ID7S210

High Side&Low Side Gate Drive IC

General Description

The ID7S210 is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels based on P_SUB P_EPI process. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. It has two versions ID7S210A & ID7S210B, and ID7S210AD & ID7S210BD are the versions with integrated BSD structure.

Features

- Fully operational to +200 V
- 3.3 V input logic compatible
- dV/dt Immunity ±50 V/nsec
- Gate drive supply range from 5 V to 20 V
- Typically 150ns deadtime
- Typically 1A output current capability
- Typically -10V negative Vs bias capability
- Matched propagation delay for both channels
- ID7S210A (LO is in phase with LIN)
- ID7S210B (LO is out of phase with LIN)
- ID7S210AD/ ID7S210BD (with built-in BSD)

Applications

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half−Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters

Package Options

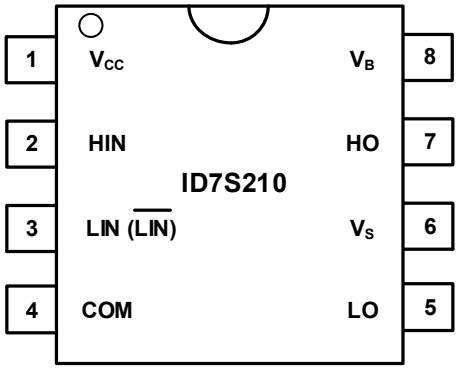
SOIC-8-

DFN8-

Order Information

Part Number	Order Code	Package	Type
ID7S210A	ID7S210ASEC-R1	SOIC8	Reel
ID7S210B	ID7S210BSEC-R1	SOIC8	Reel
ID7S210AD	ID7S210ADSEC-R1	SOIC8	Reel
ID7S210BD	ID7S210BDSEC-R1	SOIC8	Reel
ID7S210A	ID7S210ADEC-R1	DFN8	Reel
ID7S210B	ID7S210BDEC-R1	DFN8	Reel
ID7S210AD	ID7S210ADDEC-R1	DFN8	Reel
ID7S210BD	ID7S210BDDEC-R1	DFN8	Reel

Pin Configuration



Pin Definitions

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	LIN($\overline{\text{LIN}}$)	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output A version: in phase with LIN B version: out of phase with $\overline{\text{LIN}}$
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Typical Application Circuit

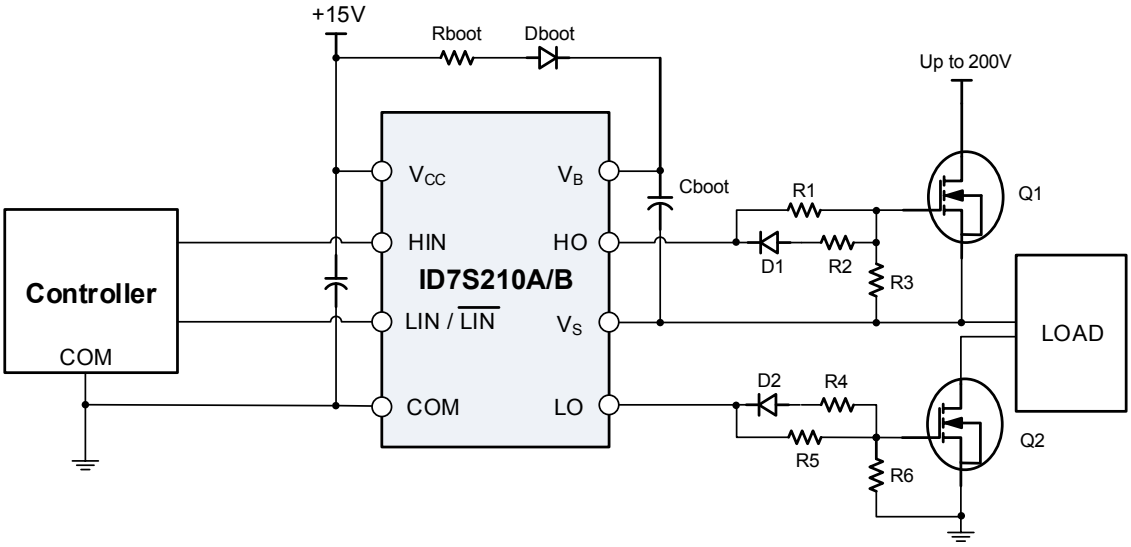


Fig.1 Typical application of ID7S210A/B

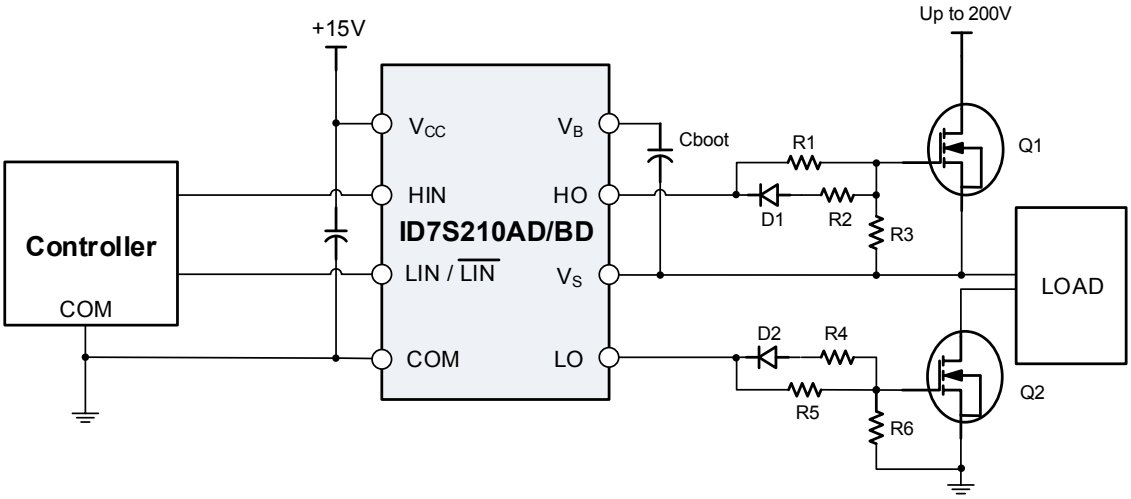


Fig.2 Typical application of ID7S210AD/ID7S210BD

Functional Block Diagram

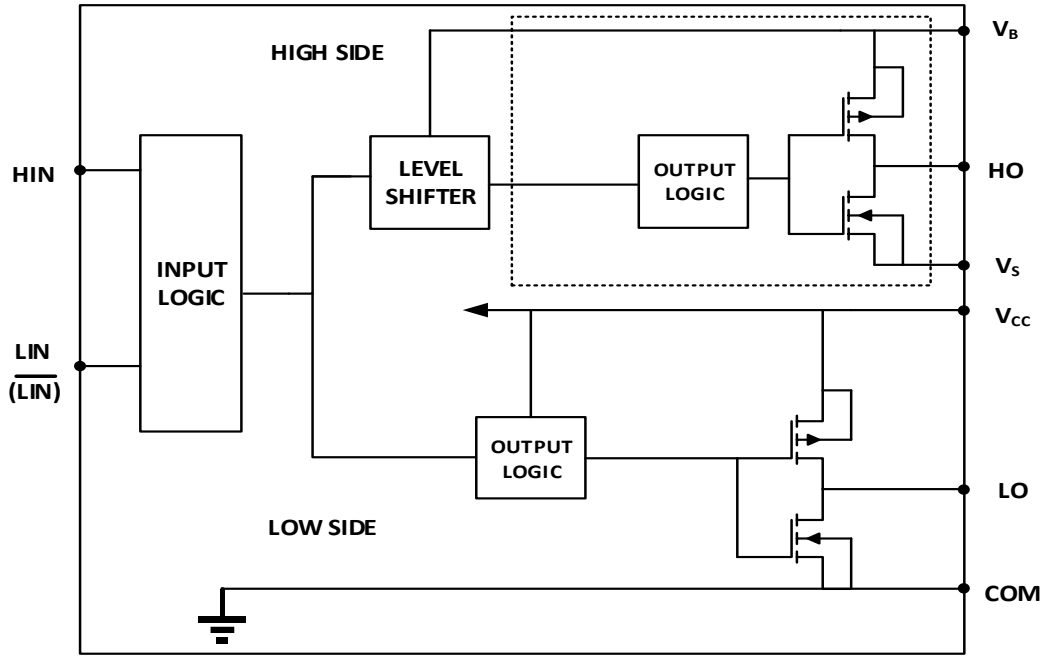


Fig.3 Function block diagram of ID7S210A/B

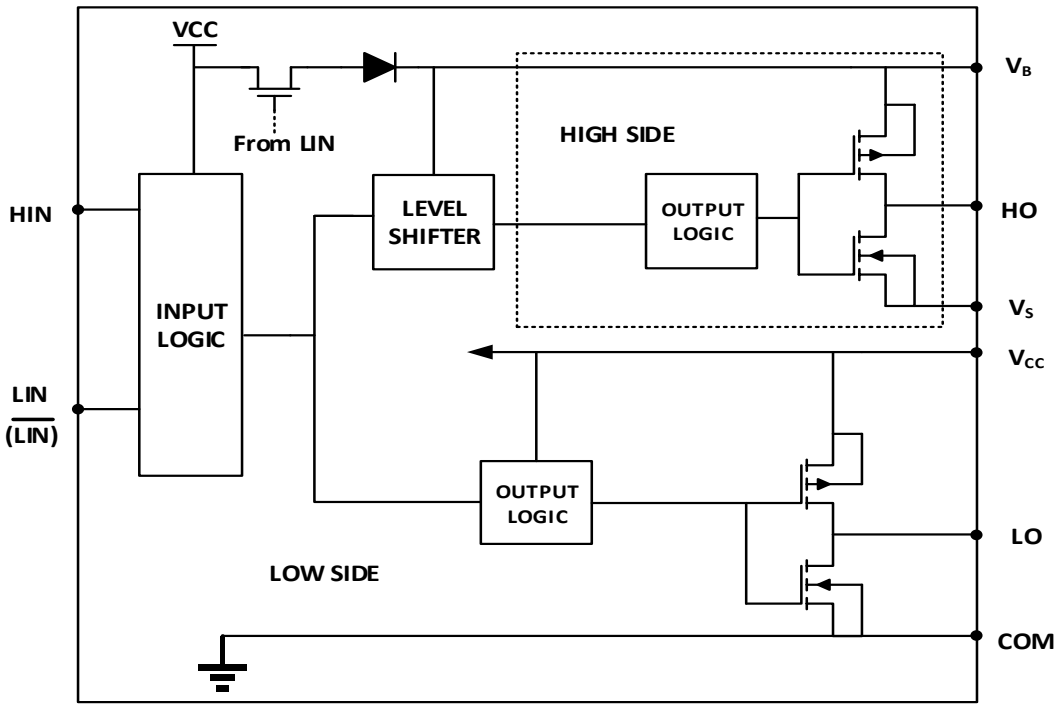


Fig.4 Function block diagram of ID7S210AD/ID7S210BD

Absolute Maximum Ratings

Exceeding these ratings may damage the device.

The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	225	V
V_S	High side floating supply return		V_B – 25	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	25	
V_{LO}	Low side gate drive output		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of $\overline{HIN}$ & $\overline{LIN}$		-0.3	V_{CC} + 0.3	
ESD	HBM Model		1.5		kV
	CDM Model		500		V
P_D	Package Power Dissipation @ TA ≤25°C	--	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	--	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S + 5	V_S + 20	V
V_S	High side floating supply return	--	200	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	5	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input of $\overline{HIN}$ & $\overline{LIN}$	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	TYP.	MAX.	Units
t_{ONH}	High side turn on propagation delay	180	240	ns
t_{OFFH}	High side turn off propagation delay	150	240	
t_{ONL}	Low side turn on propagation delay	180	240	
t_{OFFL}	Low side turn off propagation delay	150	240	
DT	Dead time	150	200	
MT	Delay matching time (t_{ON}, t_{OFF})	--	50	
t_R	Turn on rising time	50	90	
t_F	Turn off falling time	30	80	

Static Electrical Characteristics

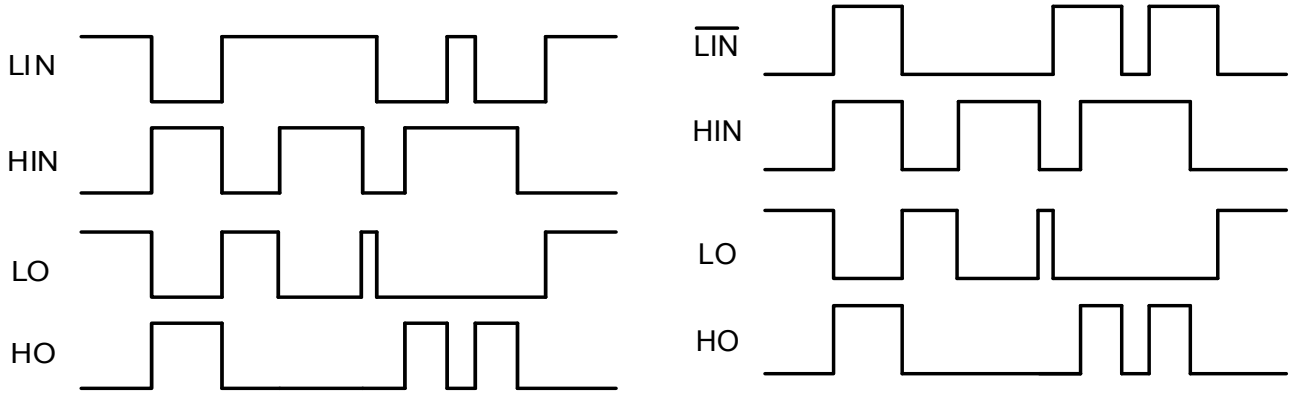
VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition		MIN.	TYP.	MAX.	Units
I_{LK}	High-side floating supply leakage current		--	--	10	µA
I_{QBS}	Quiescent V_{BS} supply current		--	80	120	
I_{QCC}	Quiescent V_{CC} supply current		--	200	320	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O		--	--	1.4	V
V_{OL}	Low level output voltage drop, V_O		--	--	0.1	
I_{O+}	Output high short circuit pulsed current		--	1000	--	mA
I_{O-}	Output low short circuit pulsed current		--	1000	--	
V_{IH}	High level input threshold voltage		2.5	--	--	V
V_{IL}	Low level input threshold voltage		--	--	0.8	
I_{IN+}	Logic “1” input bias current	ID7S210A (HIN “1” & LIN “1”)	--	1	2	µA
		ID7S210B (HIN “1” & LIN “0”)		15	20	
I_{IN-}	Logic “0” input bias current	ID7S210A (HIN “0” & LIN “0”)	--	-	1	
		ID7S210B (HIN “0” & LIN “1”)	--	10	15	
R_{BSD}	Bootstrap driver on-resistance [NOTE3]		--	200	--	Ω

Note 2: The current ability is test under the condition that VCC=15V;

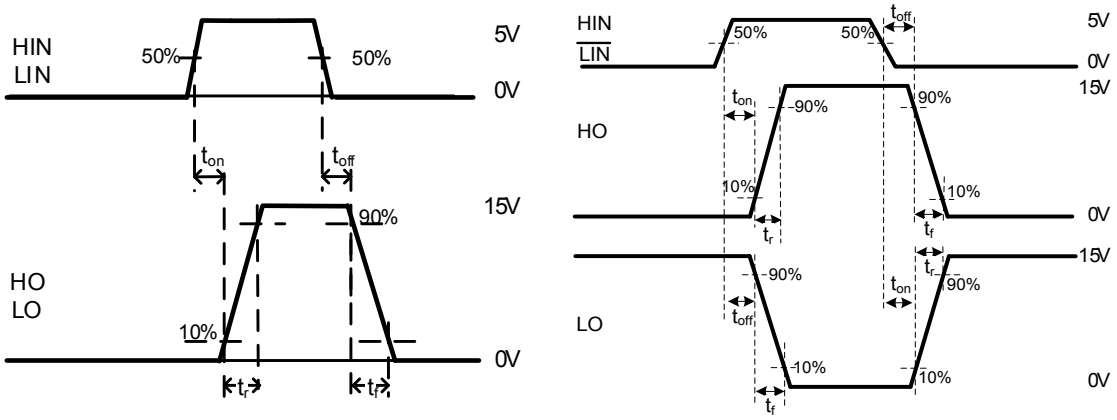
Note 3: Built in BSD is only available in ID7S210AD and ID7S210BD version.

Function Timing Diagram



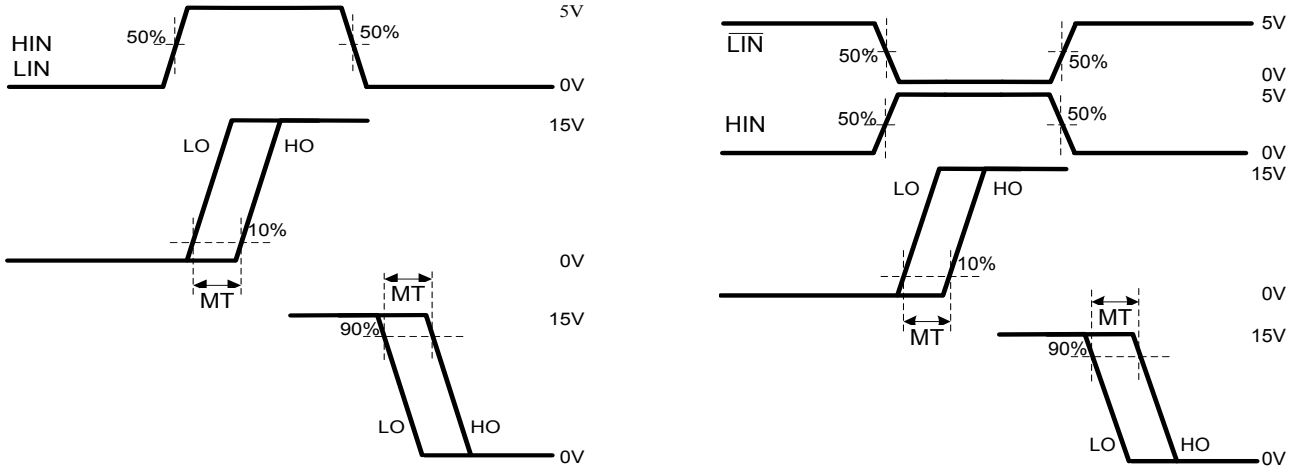
a. ID7S210A(D) b. ID7S210B(D)

Fig.5 Input and output timing waveform



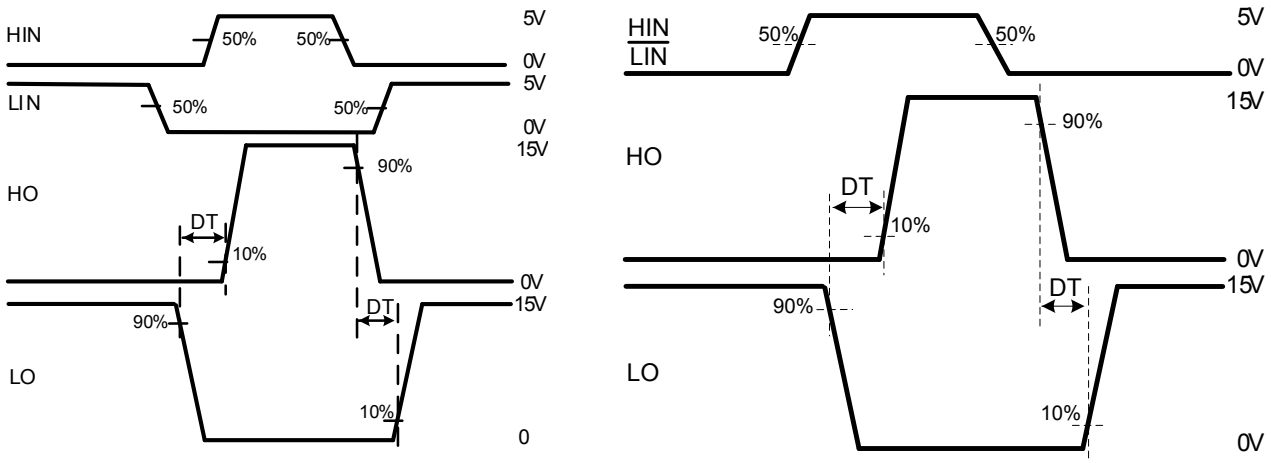
a. ID7S210A(D) b. ID7S210B(D)

Fig.6 Propagation and Rise/Fall time definition



a. ID7S210A(D) b. ID7S210B(D)

Fig.7 Delay matching definition



a. ID7S210A(D) b. ID7S210B(D)

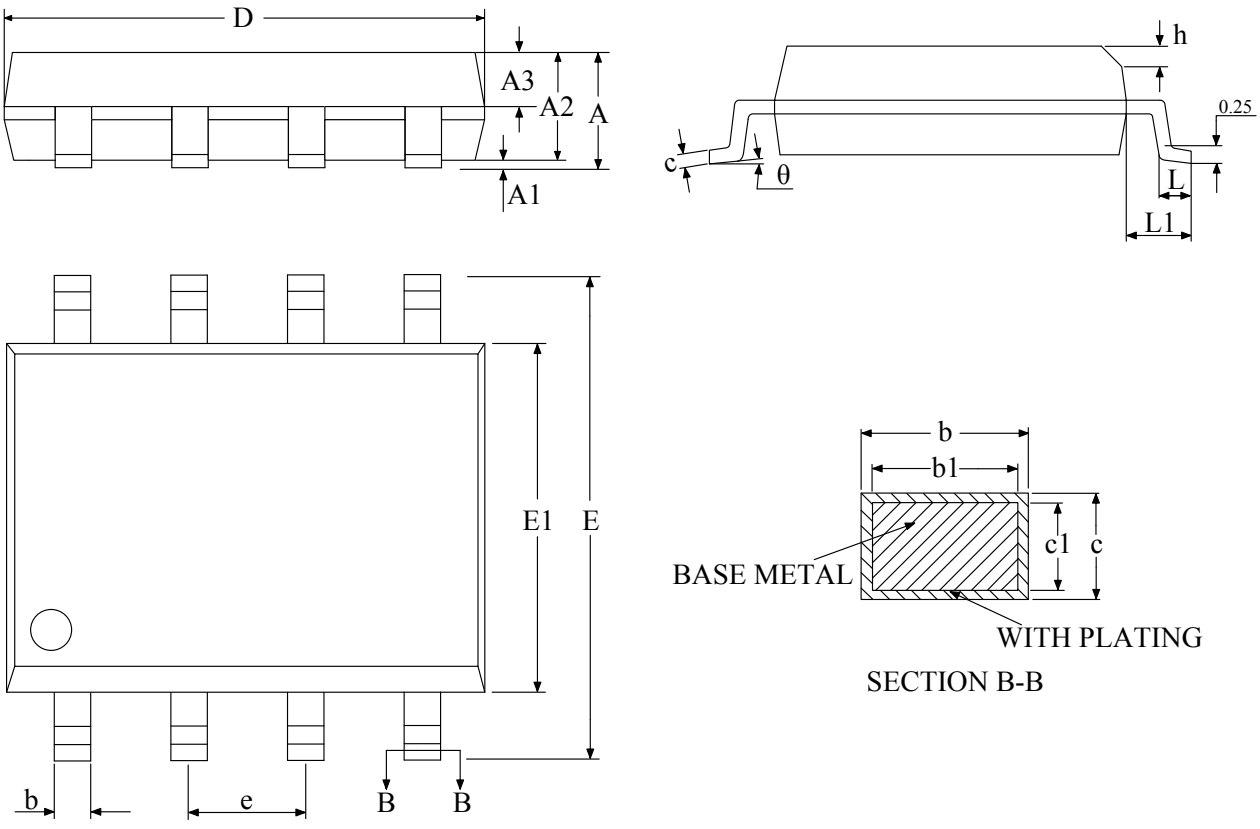
Fig.8 Dead-time waveform definitions

Package Information

SOIC8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Package Outlines



DFN8 Package Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min. (mm)	Max. (mm)	Min.(inch)	Max.(inch)
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

Package Outlines