



High-Side & Low-Side Gate Drive IC

General Description

The ID2005 is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels based on P_SUB P_EPI process. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction.

Features

- Fully operational to +200 V
- 3.3 V input logic compatible
- dV/dt Immunity ± 50 V/nsec
- Gate drive supply range from 6 V to 18 V
- Typically output Source/Sink current capability 1A/1A
- Typically -9V negative Vs bias capability

Applications

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half-Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters

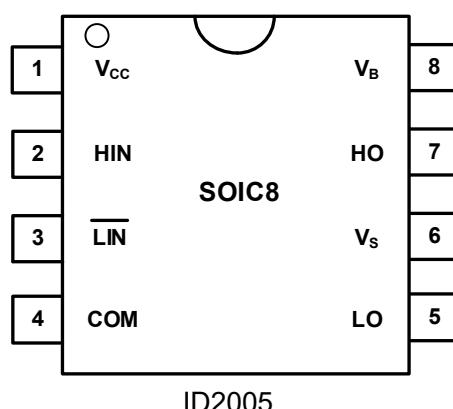
Package Options



Order Information

Part Number	Order Code	Package	Type
ID2005	ID2005SEC-R1	SOIC8	Reel

Pin Configuration



ID2005

Pin Definitions

PIN NO.	PIN NAME	PIN FUNCTION
1	V _{cc}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	LIN	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output, out of phase with LIN
6	V _s	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V _b	High side floating supply

Typical Application Circuit

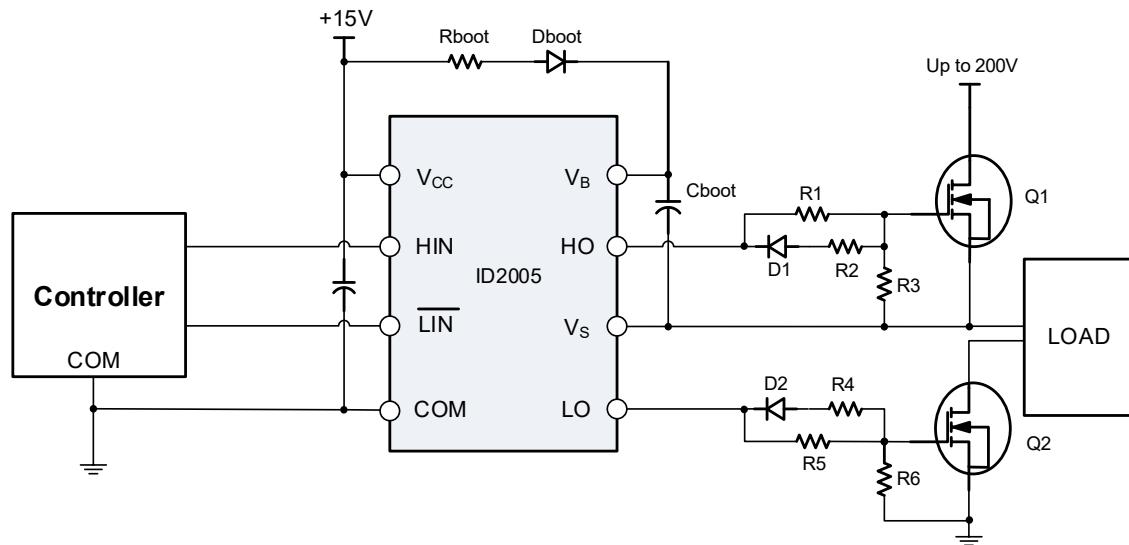


Fig.1 Typical application of ID2005

Functional Block Diagram

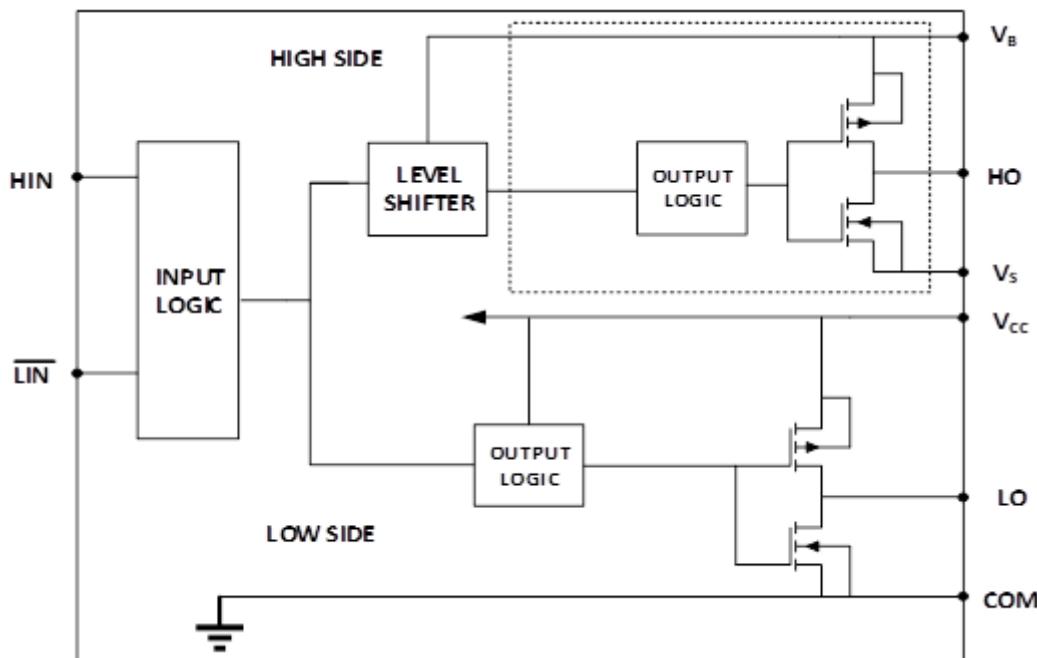


Fig.2 Function block diagram of ID2005

Absolute Maximum Ratings

Exceeding these ratings may damage the device.

The absolute maximum ratings are stress ratings only at $T_A=25^\circ\text{C}$, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	220	V
V_S	High side floating supply return	$V_B - 20$	$V_B + 0.3$	
V_{HO}	High side gate drive output	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side and main power supply	-0.3	20	
V_{LO}	Low side gate drive output	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input of HIN & LIN/ $\overline{\text{LIN}}$	-0.3	$V_{CC} + 0.3$	
ESD	HBM Model	1.5		kV
	CDM Model	500		V
P_D	Package Power Dissipation @ $TA \leq 25^\circ\text{C}$	--	--	W
R_{thJA}	Thermal Resistance Junction to Ambient	--	--	$^\circ\text{C}/\text{W}$
T_J	Junction Temperature	--	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	--	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	$V_S + 6$	$V_S + 18$	V
V_S	High side floating supply return	-9	200	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	18	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & $\overline{\text{LIN}}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	TYP.	MAX.	Units
t _{ON}	High side turn on propagation delay	150	200	ns
t _{OFF}	High side turn off propagation delay	110	200	
MT	Delay matching time (t _{ON} , t _{OFF})	--	50	
DT	Dead time	200	300	
t _R	Turn on rising time	60	100	
t _F	Turn off falling time	30	70	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
I _{LK}	High-side floating supply leakage current	--	--	50	μA
I _{QBS}	Quiescent V _{BS} supply current	--	70	120	
I _{QCC}	Quiescent V _{CC} supply current	--	200	280	
V _{OH}	High level output voltage drop, V _{BIAS} - V _O	--	--	0.2	V
V _{OL}	Low level output voltage drop, V _O	--	--	0.1	
I _{O+}	Output High short circuit pulsed current	--	1	--	A
I _{O-}	Output low short circuit pulsed current	--	1	--	
V _{IH}	High level input threshold voltage	2.5	--	--	V
V _{IL}	Low level input threshold voltage	--	--	0.8	
I _{IN+}	Logic "1" input bias current (HIN "1" & LIN "0")	--	10	20	μA
I _{IN-}	Logic "0" input bias current (HIN "0" & LIN "1")	--	15	30	

Function Timing Diagram

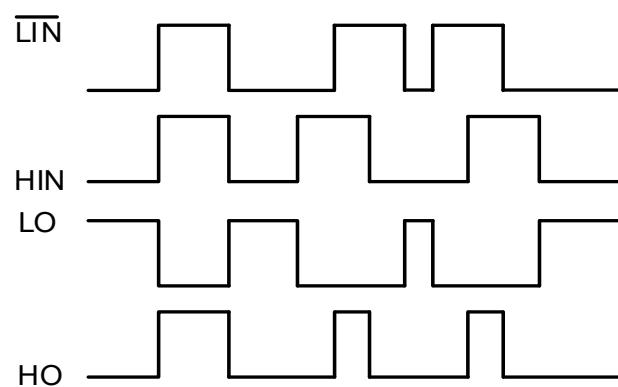


Fig.1 Input and output timing waveform (ID2005)

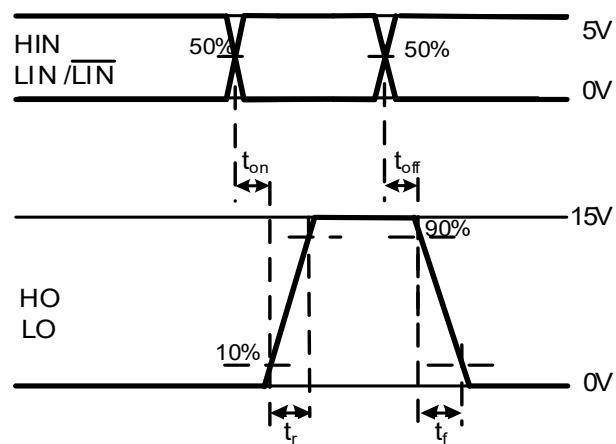


Fig.2 Propagation and Rise/Fall time definition

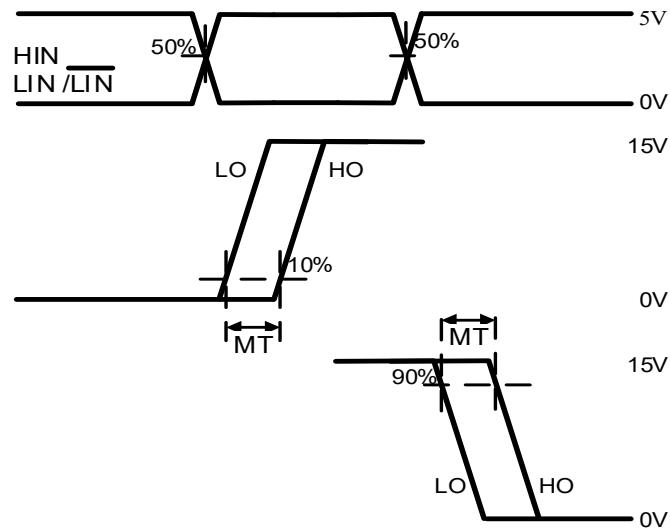


Fig.3 Delay matching definition

Package Information

SOIC8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Package Outlines

