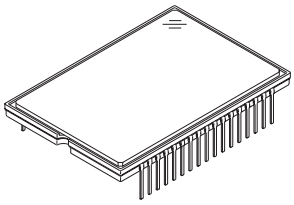
SONY

ICX413AQ

Diagonal 28.40mm (Type 1.8) Frame Readout CCD Image Sensor with Square Pixel for Color Cameras

34 pin DIP (Plastic)

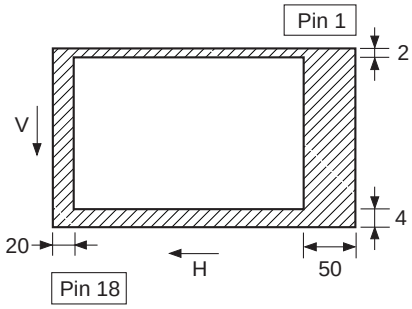


Description

The ICX413AQ is a diagonal 28.40mm (Type 1.8) interline CCD solid-state image sensor with a square pixel array and 6.15M effective pixels. Frame readout allows all pixels' signals to be output independently within approximately 1/3.08 second. Adoption of a design specially suited for frame readout ensures a high saturation signal level.

High sensitivity and low dark current are achieved through the adoption of R, G and B primary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

This chip is suitable for applications such as electronic still cameras, etc.



Optical black position (Top View)

Features

- Frame readout mode
- High horizontal and vertical resolution
- Square pixel
- Horizontal drive frequency: 25.0MHz
- R, G, B primary color mosaic filters on chip
- High sensitivity, low dark current

Device Structure

- Interline CCD image sensor
- Optical size: Diagonal 28.40mm (Type 1.8)
- Total number of pixels: 3110 (H) × 2030 (V) approx. 6.31M pixels
- Number of effective pixels: 3040 (H) × 2024 (V) approx. 6.15M pixels
- Number of active pixels: 3032 (H) × 2016 (V) approx. 6.11M pixels
- Number of recommended recording pixels: 3000 (H) × 2000 (V) approx. 6M pixels
- Chip size: 25.10mm (H) × 17.64mm (V)
- Unit cell size: 7.80µm (H) × 7.80µm (V)
- Optical black: Horizontal (H) direction: Front 20 pixels, rear 50 pixels
  Vertical (V) direction: Front 4 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 31
  Vertical 1 (even fields only)
- Substrate material: Silicon

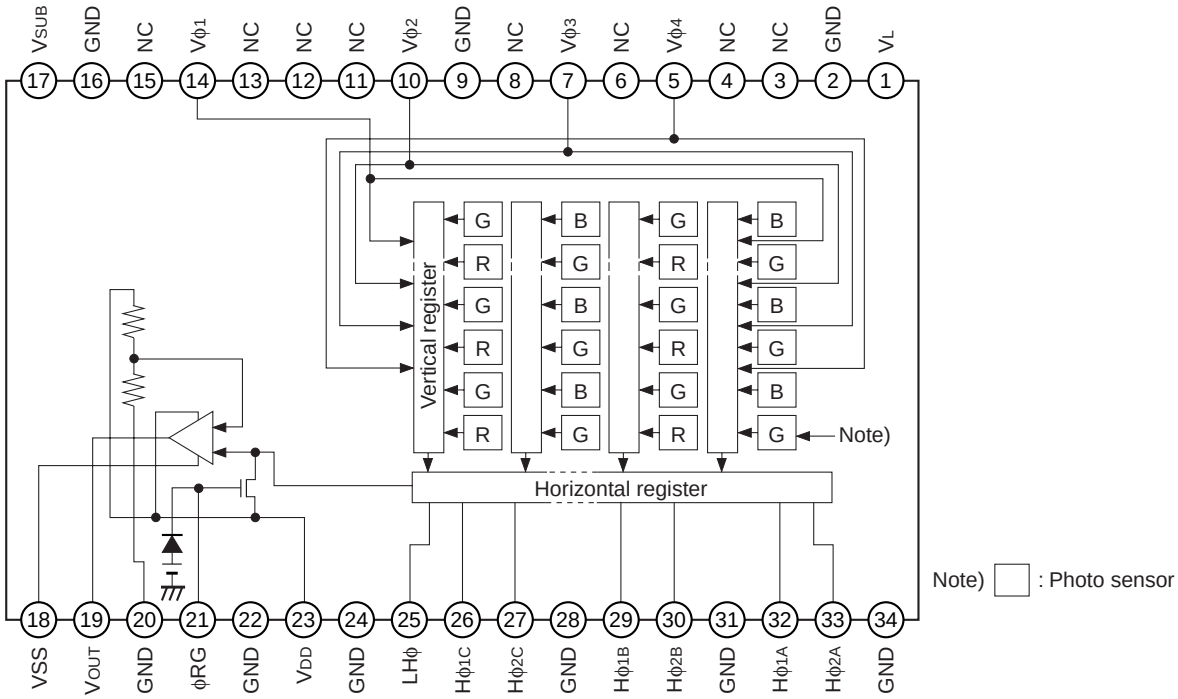
Super **HAD CCD** ™

* Super HAD CCD is a registered trademark of Sony Corporation. Super HAD CCD is a CCD that drastically improves sensitivity by introducing newly developed semiconductor technology by Sony Corporation into Sony's high-performance HAD (Hole-Accumulation Diode) sensor.

E02120B35

Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V_L	Protective transistor bias	18	VSS	Output amplifier source
2	GND	GND	19	V_{OUT}	Signal output
3	NC		20	GND	GND
4	NC		21	φRG	Reset gate clock
5	Vφ4	Vertical register transfer clock	22	GND	GND
6	NC		23	V_{DD}	Supply voltage
7	Vφ3	Vertical register transfer clock	24	GND	GND
8	NC		25	LHφ	Horizontal register final stage transfer clock
9	GND	GND	26	Hφ1C	Horizontal register transfer clock
10	Vφ2	Vertical register transfer clock	27	Hφ2C	Horizontal register transfer clock
11	NC		28	GND	GND
12	NC		29	Hφ1B	Horizontal register transfer clock
13	NC		30	Hφ2B	Horizontal register transfer clock
14	Vφ1	Vertical register transfer clock	31	GND	GND
15	NC		32	Hφ1A	Horizontal register transfer clock
16	GND	GND	33	Hφ2A	Horizontal register transfer clock
17	V_{SUB}	Substrate bias	34	GND	GND

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +10	V	
	Vφ1, Vφ3 – φSUB	–50 to +15	V	
	Vφ2, Vφ4, V_L – φSUB	–50 to +0.3	V	
	LHφ, Hφ1α, Hφ2α, GND – φSUB (α = A, B, C)	–40 to +0.3	V	
Against GND	V_{DD}, V_{OUT}, φRG – GND	–0.3 to +18	V	
	Vφ1, Vφ2, Vφ3, Vφ4 – GND	–10 to +18	V	
	LHφ, Hφ1α, Hφ2α – GND (α = A, B, C)	–10 to +7	V	
Against V_L	Vφ1, Vφ3 – V_L	–0.3 to +28	V	
	Vφ2, Vφ4, LHφ, Hφ1α, Hφ2α, GND – V_L (α = A, B, C)	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	Hφ1α – Hφ2α (α = A, B, C)	–7 to +7	V	
	Hφ1α, Hφ2α – Vφ4 (α = A, B, C)	–17 to +17	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier source	V_{SS}	Ground with resistance of 750 to 900Ω				
Substrate voltage adjustment range	V_{SUB}	8.0		15.0		
Protective transistor bias	V_L		*1			
Reset gate clock	φRG		*2			

*1 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

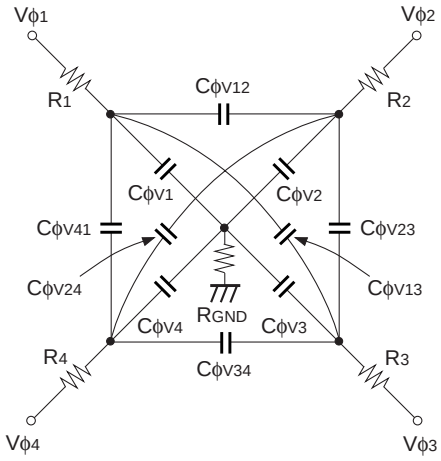
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		7.0		mA	

Clock Voltage Conditions

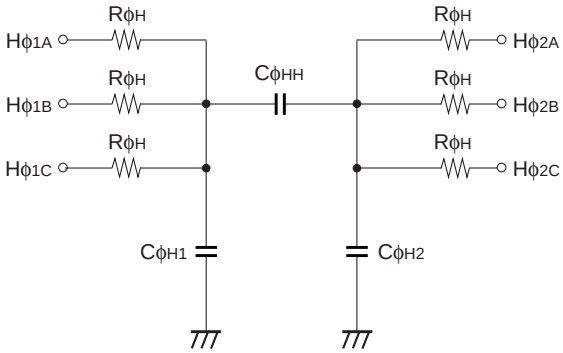
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.5	–8.0	–7.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi V$		8.0		V	2	$V\phi V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi H$	5.75	6.0	7.0	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}		3.0		V	3	Cross-point voltage
Horizontal final stage transfer clock voltage	V_{LHH}	5.75	6.0	7.0	V	4	
	V_{LHL}	–0.05	0	0.05	V	4	
Reset gate clock voltage	$V\phi RG$	4.75	5.0	5.25	V	5	
	$V_{RGLH} – V_{RGLL}$			0.4	V	5	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	5	Low-level coupling
Substrate clock voltage	$V\phi SUB$	22.0	23.0	24.0	V	6	

Clock Equivalent Circuit Constant

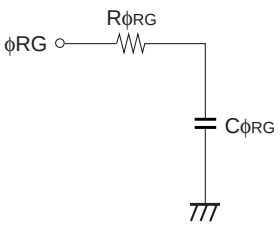
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		18000		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		15000		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		18000		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		10000		pF	
	$C_{\phi V13}$		6800		pF	
	$C_{\phi V24}$		8200		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		18		pF	
	$C_{\phi H2}$		27		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		221		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH}$		8		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		6		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		2700		pF	
Vertical transfer clock series resistor	R_1, R_2, R_3, R_4		18		Ω	
Vertical transfer clock ground resistor	R_{GND}		3.9		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		2.2		Ω	
Horizontal final stage transfer clock series resistor	$R_{\phi LH}$		39		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		39		Ω	



Vertical transfer clock equivalent circuit



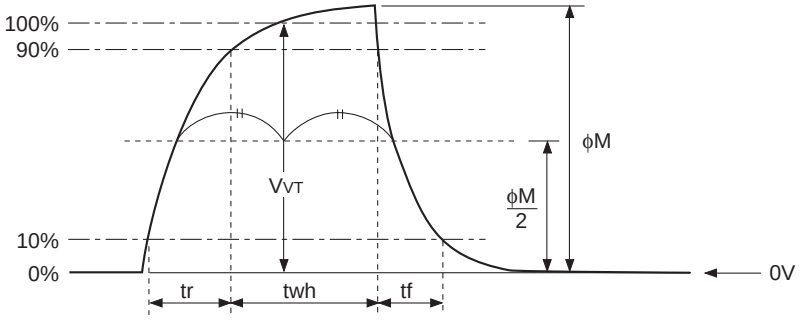
Horizontal transfer clock equivalent circuit



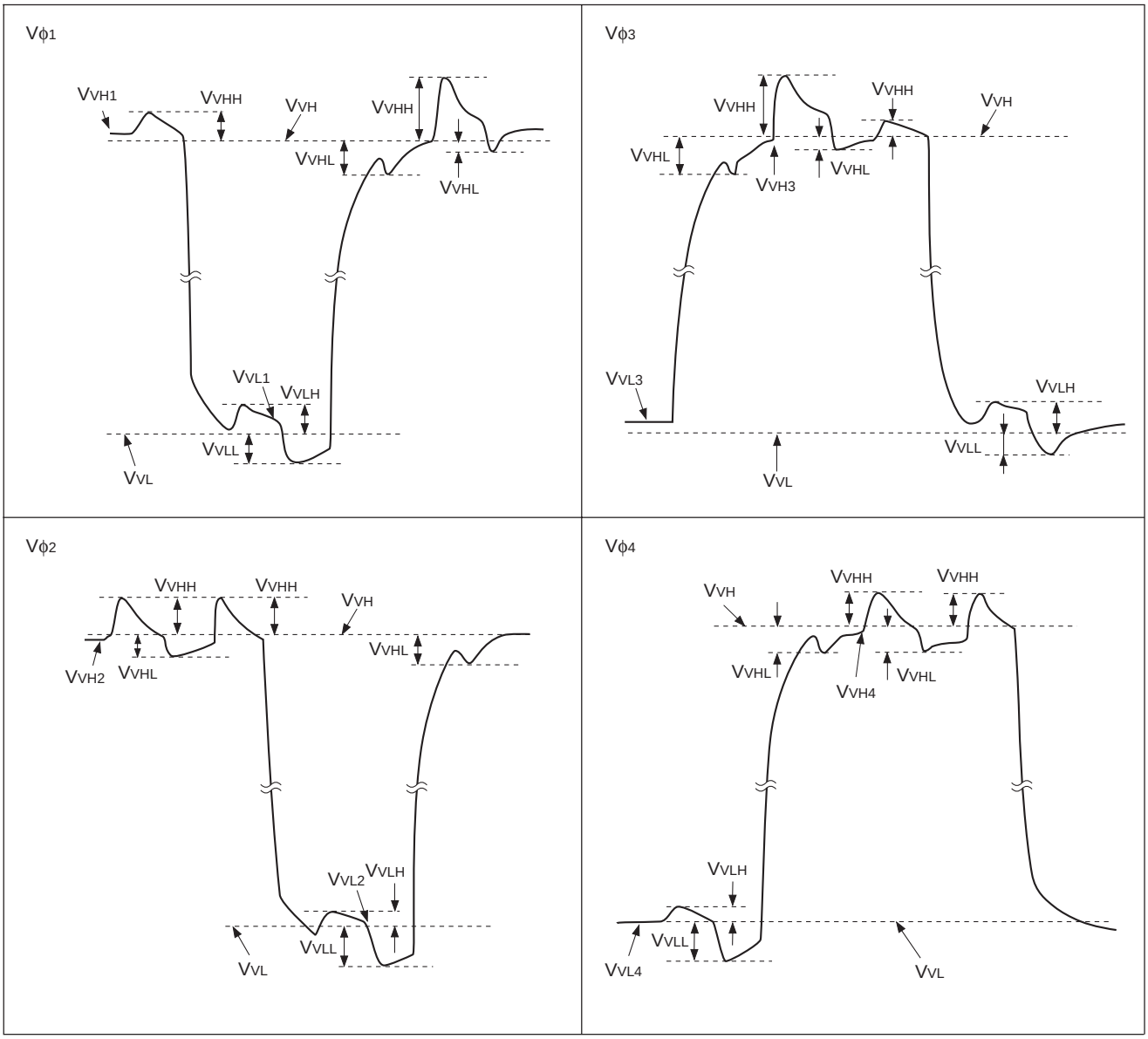
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform

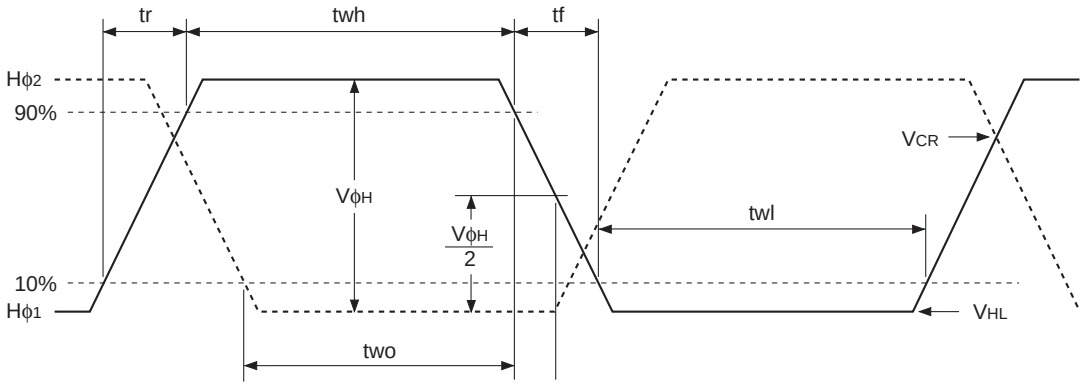


(2) Vertical transfer clock waveform



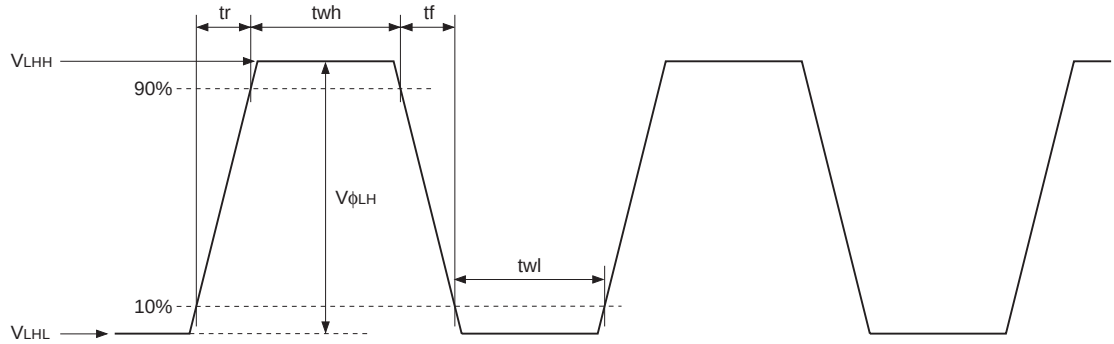
$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform

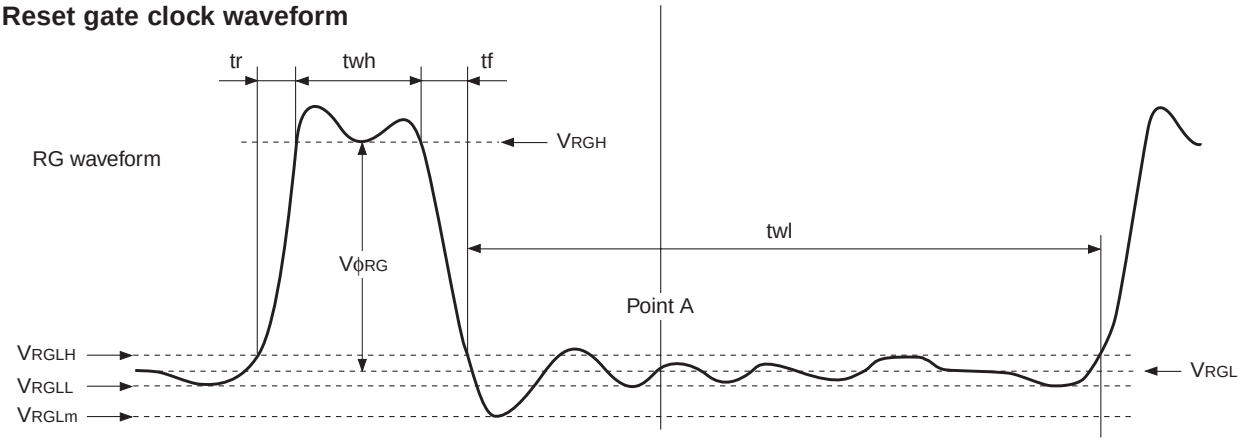


Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

(4) Horizontal final stage transfer clock waveform



(5) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

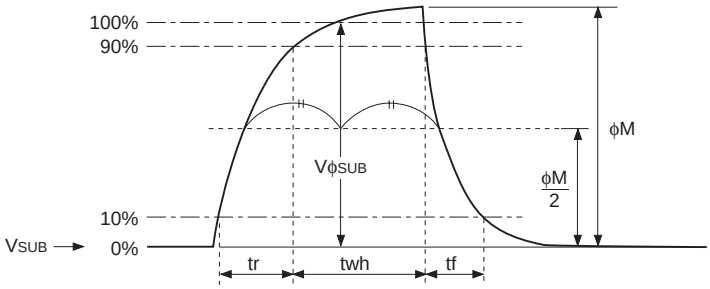
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval with twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(6) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 25MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	VT		7.5						1.5			1.5		μs	During readout
Vertical transfer clock	Vφ1, Vφ2, Vφ3, Vφ4								2			2		μs	When using CXD1268M
Horizontal transfer clock	Hφ1		15			15			5			5		ns	
	Hφ2		15			15			5			5			
Horizontal final stage transfer clock	LHφ		17			17			3			3		ns	*1
Reset gate clock	φRG		7						2			2		ns	
Substrate clock	φSUB		6											μs	When draining charge

*1 The phase of horizontal final stage transfer clock amplitude level 50% and horizontal transfer clock Hφ2 amplitude level 50% must be matched.

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	Hφ1, Hφ2		17		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

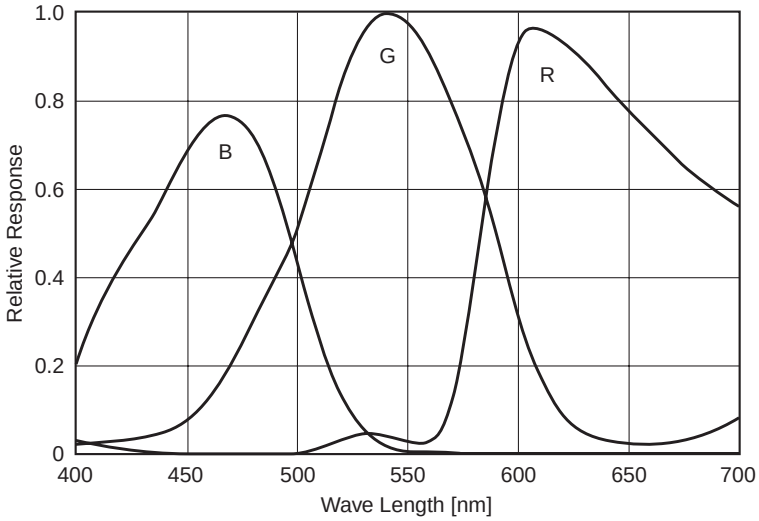


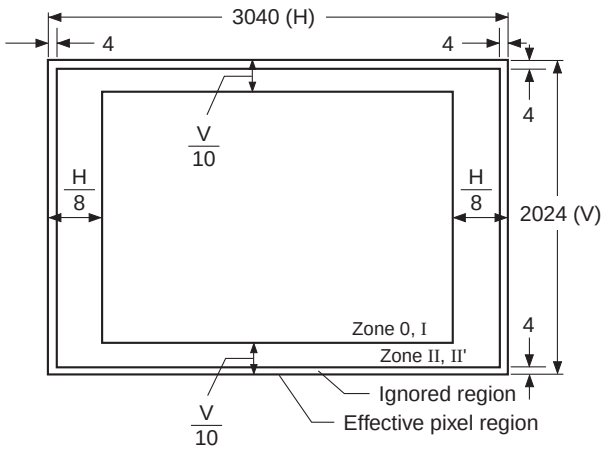
Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity	Sg	800	1000	1200	mV	1	1/30s accumulation
Sensitivity comparison	Rr	0.42	0.57	0.72		1	
	Rb	0.23	0.38	0.53			
Saturation signal	Vsat	900			mV	2	Ta = 60°C
Smear	Sm		–110	–90	dB	3	Frame readout mode, *1
Video signal shading	SHg			20	%	4	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			4	mV	5	Ta = 60°C, 3.08 frame/s
Dark signal shading	ΔVdt			2	mV	6	Ta = 60°C, 3.08 frame/s, *2
Line crawl G	Lcg			10	%	7	
Line crawl R	Lcr			10	%	7	
Line crawl B	Lcb			10	%	7	
Lag	Lag			0.5	%	8	

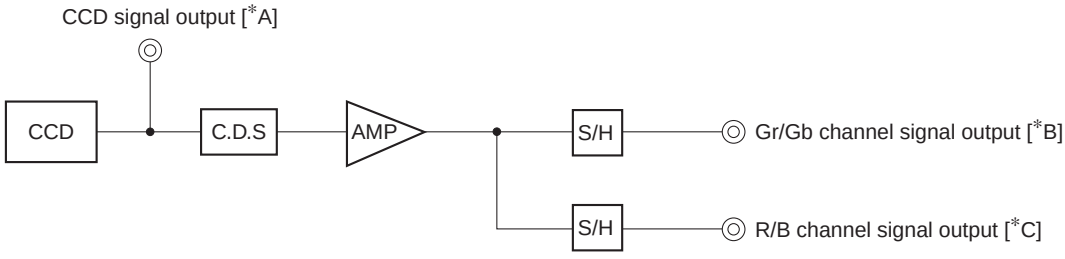
*1 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation.

*2 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

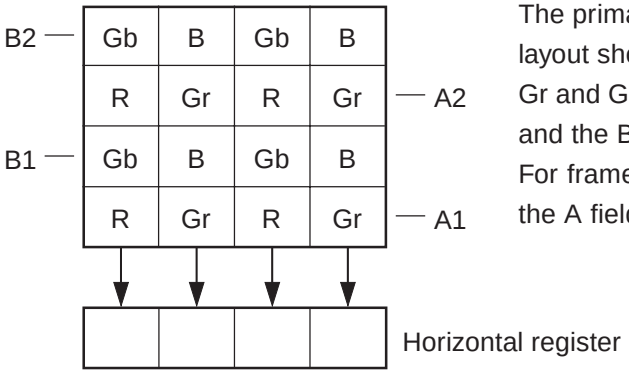
Image Sensor Characteristics Measurement Method

◎ Measurement conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

◎ Color coding of this image sensor & Readout



Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement).
Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.
For frame readout, the A1 and A2 lines are output as signals in the A field, and the B1 and B2 lines in the B field.

◎ Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity comparison
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{Gr}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$$V_G = (V_{Gr} + V_{Gb})/2$$
$$Sg = V_G \times \frac{100}{30} \text{ [mV]}$$
$$Rr = V_R/V_G$$
$$Rb = V_B/V_G$$

2. Saturation signal
Set to the standard imaging condition II: After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV.
After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = 20 \times \log\left(Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10}\right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Grmax [mV]) and minimum value (Grmin [mV]) of the Gr signal output and substitute the values into the following formula.

$$SHg = (Grmax - Grmin)/150 \times 100 \text{ [\%]}$$

5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

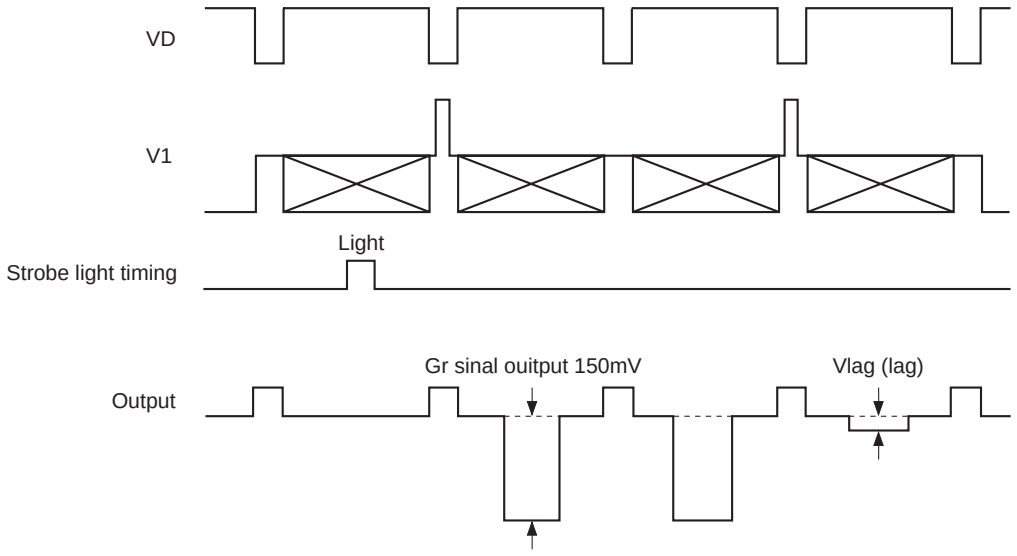
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

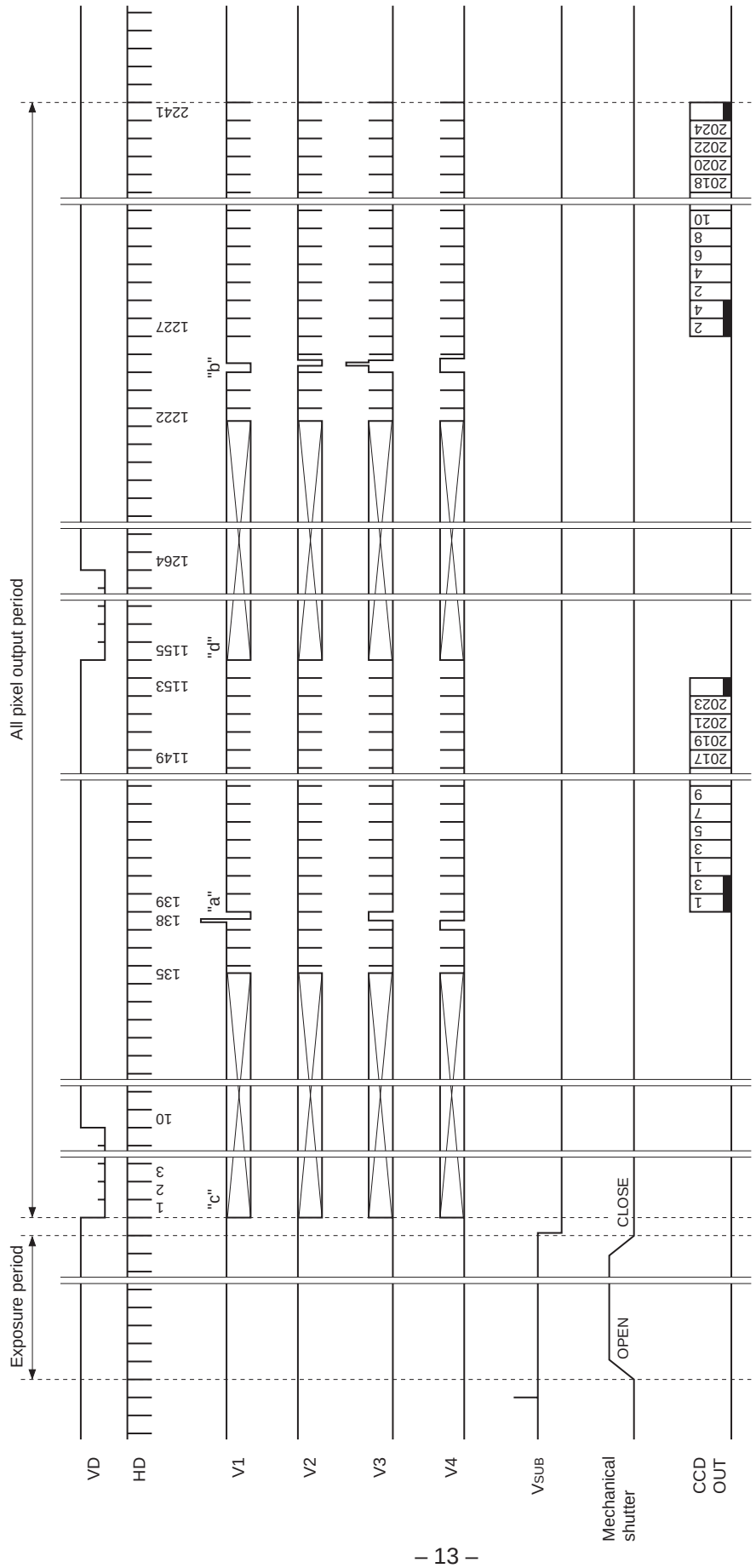
   $$Lci = \frac{\Delta Gli}{Gai} \times 100 \text{ [\%]} \quad (i = r, g, b)$$

8. Lag
   Adjust the Gr channel output generated by the strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]

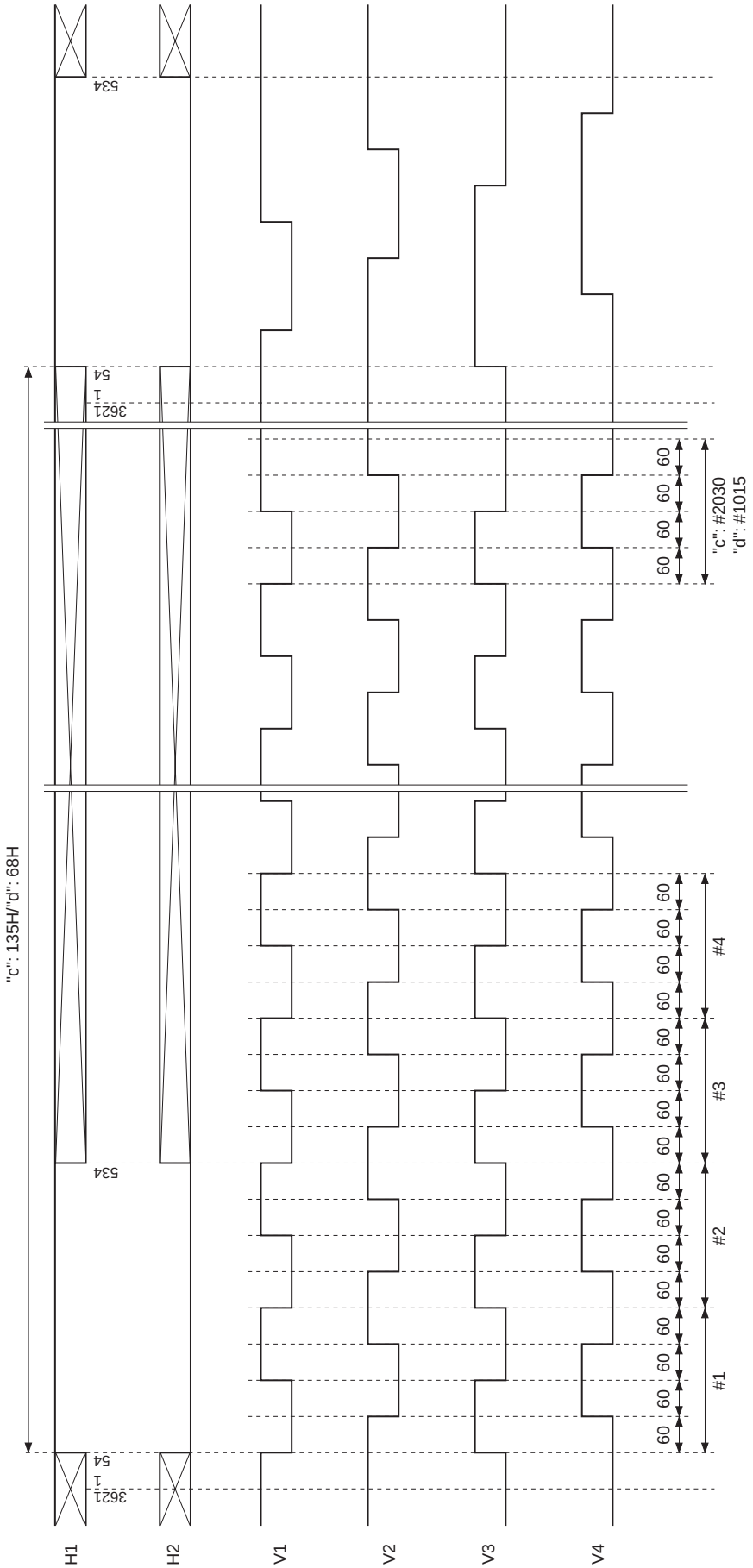


Drive Timing Chart (Vertical Sync Accumulation Time Control by Mechanical Shutter) Frame Readout Mode

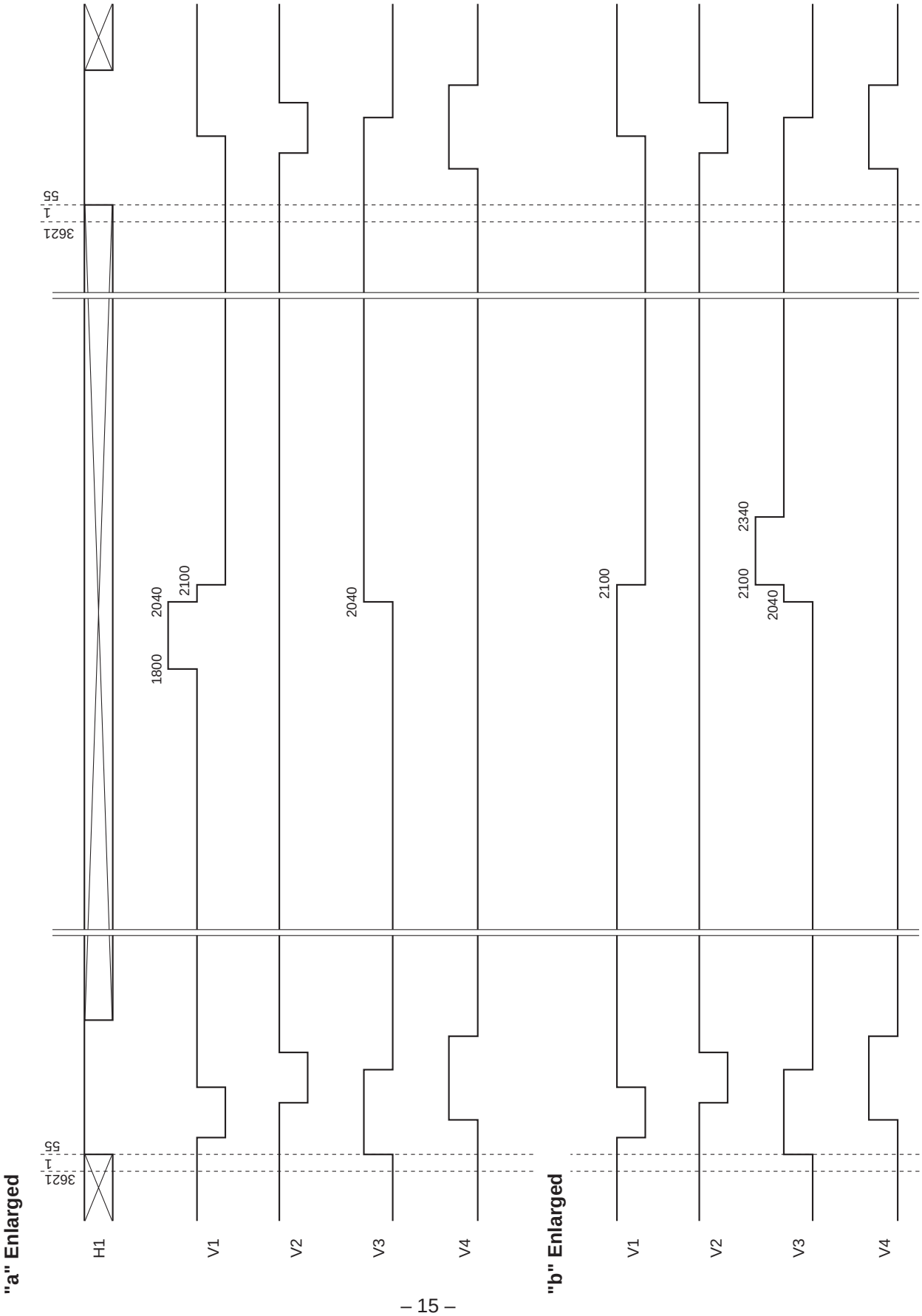


Drive Timing Chart (Vertical Sync) Frame Readout Mode

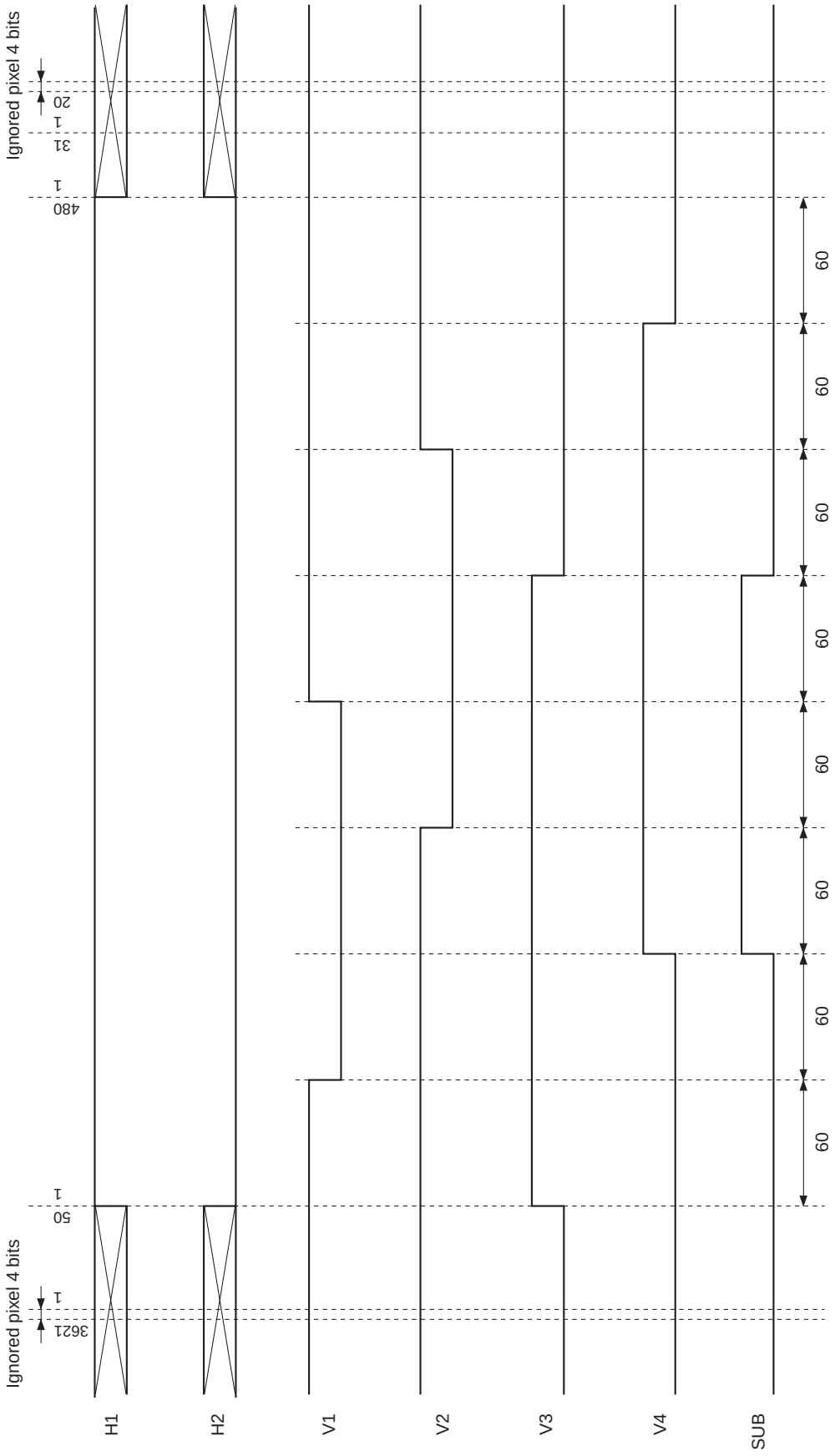
Vertical Sync "c" Enlarged, "d" Enlarged



Drive Timing Chart (Vertical Sync "a" Enlarged, "b" Enlarged)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Operate in clean environments (around class 1000 is appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

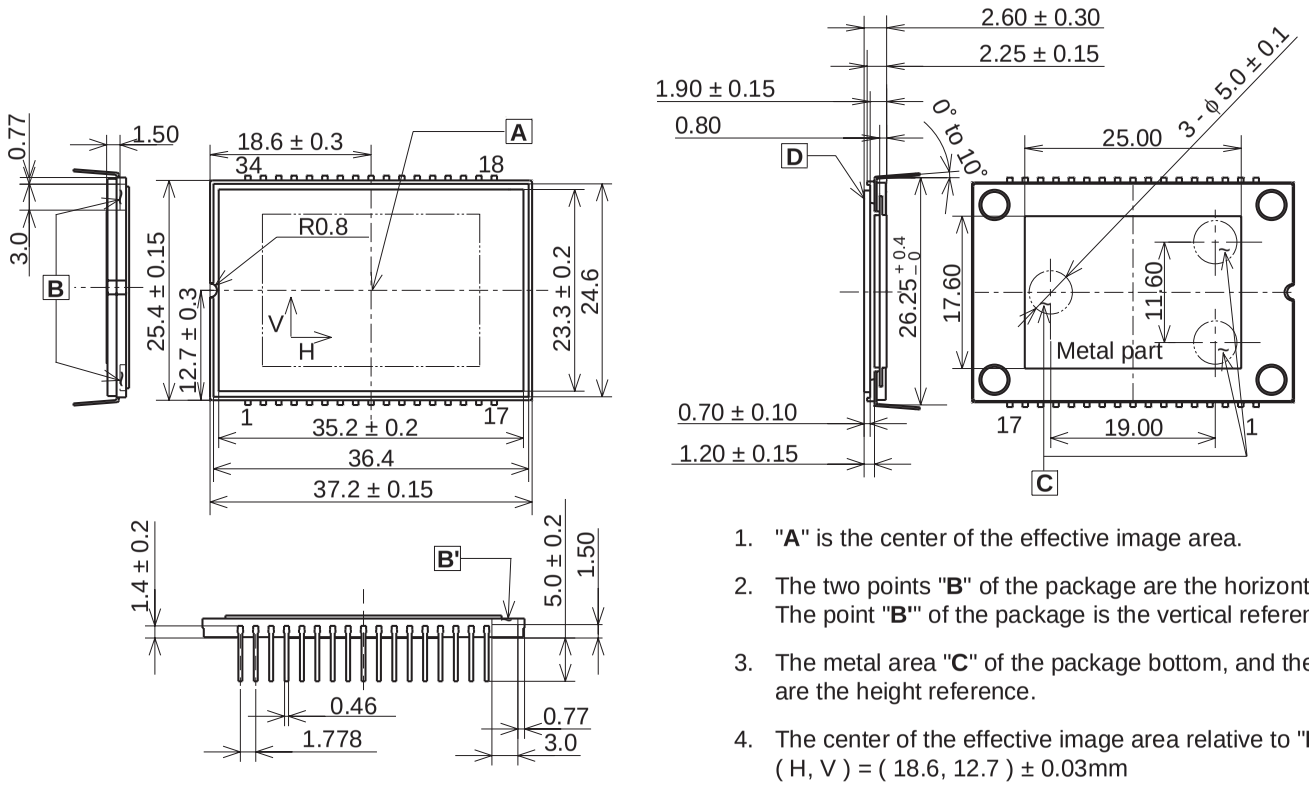
4) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

34 Pin DIP



PACKAGE MATERIAL	Plastic, Metal
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	7.00g
DRAWING NUMBER	AS-Z4(E)

1. "**A**" is the center of the effective image area.
2. The two points "**B**" of the package are the horizontal reference.
   The point "**B'**" of the package is the vertical reference.
3. The metal area "**C**" of the package bottom, and the top of the cover glass "**D**" are the height reference.
4. The center of the effective image area relative to "**B**" and "**B'**" is (H, V) = (18.6, 12.7) ± 0.03mm
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom "**C**" to the effective image area is 1.40 ± 0.15mm.
   The height from the top of the cover glass "**D**" to the effective image area is 1.20 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom "**C**" is less than 150µm.
8. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.
10. Metal part at the bottom of a package is sticking out 0.1mm. from the surrounding plastic part.