

## Two Output Differential Buffer for PCIe Gen1 & Gen2

ICS9DB102

### Description

The **ICS9DB102** zero-delay buffer supports PCI Express clocking requirements. The **ICS9DB102** is driven by a differential SRC output pair from an ICS CK410/CK505-compliant main clock. It attenuates jitter on the input clock and has a selectable PLL Band Width to maximize performance in systems with or without Spread-Spectrum clocking.

### Output Features

- 2 - 0.7V current mode differential output pairs (HCSL)

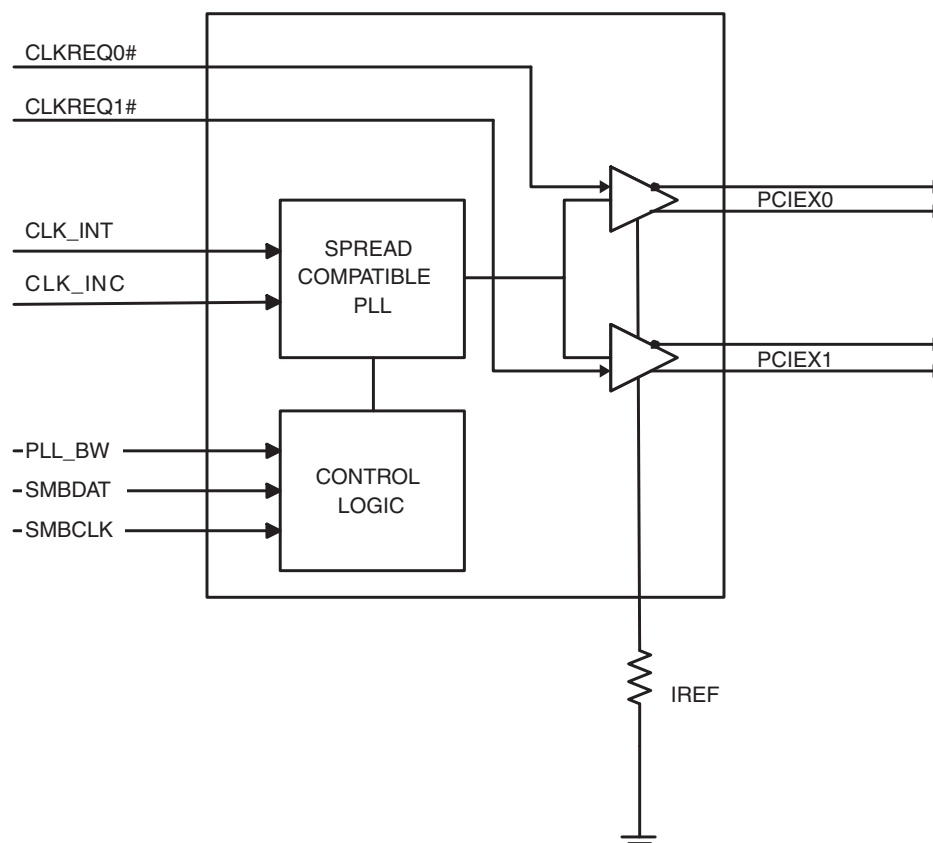
### Features/Benefits

- CLKREQ# pin for outputs 1 and 4/output enable for Express Card applications
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled
- Industrial temperature range available

### Key Specifications

- Cycle-to-cycle jitter < 35ps
- Output-to-output skew < 25ps

### Functional Block Diagram



## Pin Configuration

|           |    |                  |    |           |
|-----------|----|------------------|----|-----------|
| PLL_BW    | 1  | <b>ICS9DB102</b> | 20 | VDDA      |
| CLK_INT   | 2  |                  | 19 | GNDA      |
| CLK_INC   | 3  |                  | 18 | IREF      |
| vCLKREQ0# | 4  |                  | 17 | vCLKREQ1# |
| VDD       | 5  |                  | 16 | VDD       |
| GND       | 6  |                  | 15 | GND       |
| PCIEXT0   | 7  |                  | 14 | PCIEXT1   |
| PCIEXC0   | 8  |                  | 13 | PCIEXC1   |
| VDD       | 9  |                  | 12 | VDD       |
| SMBDAT    | 10 |                  | 11 | SMBCLK    |

**Note:** Pins preceded by 'v' have internal 120K ohm pull down resistors

## Power Groups

| Pin Number |      | Description                   |
|------------|------|-------------------------------|
| VDD        | GND  |                               |
| 5,9,12,16  | 6,15 | PCI Express Outputs           |
| 9          | 6    | SMBUS                         |
| 20         | 19   | IREF                          |
| 20         | 19   | Analog VDD & GND for PLL core |

## 20-pin SSOP & TSSOP

## Pin Description

| PIN # | PIN NAME  | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                                                     |
|-------|-----------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | PLL_BW    | IN       | 3.3V input for selecting PLL Band Width<br>0 = low, 1= high                                                                                                                                                                                                     |
| 2     | CLK_INT   | IN       | True Input for differential reference clock.                                                                                                                                                                                                                    |
| 3     | CLK_INC   | IN       | Complementary Input for differential reference clock.                                                                                                                                                                                                           |
| 4     | vCLKREQ0# | IN       | Output enable for PCI Express output pair 0.<br>0 = enabled, 1 =disabled                                                                                                                                                                                        |
| 5     | VDD       | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                                                      |
| 6     | GND       | PWR      | Ground pin.                                                                                                                                                                                                                                                     |
| 7     | PCIEXT0   | OUT      | True clock of differential PCI_Express pair.                                                                                                                                                                                                                    |
| 8     | PCIEXC0   | OUT      | Complementary clock of differential PCI_Express pair.                                                                                                                                                                                                           |
| 9     | VDD       | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                                                      |
| 10    | SMBDAT    | I/O      | Data pin of SMBUS circuitry, 5V tolerant                                                                                                                                                                                                                        |
| 11    | SMBCLK    | IN       | Clock pin of SMBUS circuitry, 5V tolerant                                                                                                                                                                                                                       |
| 12    | VDD       | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                                                      |
| 13    | PCIEXC1   | OUT      | Complementary clock of differential PCI_Express pair.                                                                                                                                                                                                           |
| 14    | PCIEXT1   | OUT      | True clock of differential PCI_Express pair.                                                                                                                                                                                                                    |
| 15    | GND       | PWR      | Ground pin.                                                                                                                                                                                                                                                     |
| 16    | VDD       | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                                                      |
| 17    | vCLKREQ1# | IN       | Output enable for PCI Express output pair 1.<br>0 = enabled, 1 =disabled                                                                                                                                                                                        |
| 18    | IREF      | OUT      | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 19    | GNDA      | PWR      | Ground pin for the PLL core.                                                                                                                                                                                                                                    |
| 20    | VDDA      | PWR      | 3.3V power for the PLL core.                                                                                                                                                                                                                                    |

### Note:

Pins preceded by 'v' have internal 120K ohm pull down resistors

## Absolute Max

| Symbol   | Parameter                                | Min       | Max             | Units |
|----------|------------------------------------------|-----------|-----------------|-------|
| VDDA     | 3.3V Core Supply Voltage                 |           | $V_{DD} + 0.5V$ | V     |
| VDD      | 3.3V Output Supply Voltage               | GND - 0.5 | $V_{DD} + 0.5V$ | V     |
| Ts       | Storage Temperature                      | -65       | 150             | °C    |
| Tcase    | Case Temperature                         |           | 115             | °C    |
| ESD prot | Input ESD protection<br>human body model | 2000      |                 | V     |

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = Tambient; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%

| PARAMETER                                  | SYMBOL                | CONDITIONS                                                      | MIN            | TYP | MAX            | UNITS  | NOTES |
|--------------------------------------------|-----------------------|-----------------------------------------------------------------|----------------|-----|----------------|--------|-------|
| Tambient                                   | Tambcom               | Commercial range                                                | 0              |     | 70             | °C     | 1     |
|                                            | Tambind               | Industrial range                                                | -40            |     | 85             | °C     | 1     |
| Input High Voltage                         | V <sub>IH</sub>       | 3.3 V +/-5%                                                     | 2              |     | $V_{DD} + 0.3$ | V      | 1     |
| Input Low Voltage                          | V <sub>IL</sub>       | 3.3 V +/-5%                                                     | $V_{SS} - 0.3$ |     | 0.8            | V      | 1     |
| Input High Current                         | I <sub>IH</sub>       | V <sub>IN</sub> = V <sub>DD</sub>                               | -5             |     | 5              | uA     | 1     |
| Input Low Current                          | I <sub>IL1</sub>      | V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors         | -5             |     |                | uA     | 1     |
|                                            | I <sub>IL2</sub>      | V <sub>IN</sub> = 0 V; Inputs with pull-up resistors            | -200           |     |                | uA     | 1     |
| Operating Supply Current                   | I <sub>DD3.3OP</sub>  | Full Active, C <sub>L</sub> = Full load;                        |                | 75  | 100            | mA     | 1     |
|                                            |                       | all differential pairs tri-stated                               |                | 27  | 50             | mA     | 1     |
| Input Frequency <sup>3</sup>               | F <sub>i</sub>        | V <sub>DD</sub> = 3.3 V                                         | 99             | 100 | 101            | MHz    | 1     |
| Pin Inductance <sup>1</sup>                | L <sub>pin</sub>      |                                                                 |                |     | 7              | nH     | 1     |
| Input Capacitance <sup>1</sup>             | C <sub>IN</sub>       | Logic Inputs                                                    |                |     | 5              | pF     | 1     |
|                                            | C <sub>OUT</sub>      | Output pin capacitance                                          |                |     | 4.5            | pF     | 1     |
| Clk Stabilization <sup>1,2</sup>           | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up to 1st clock                      |                |     | 1.8            | ms     | 1     |
| Modulation Frequency                       |                       | Triangular Modulation                                           | 30             |     | 33             | KHz    | 1     |
| Spread Spectrum Modulation Frequency       | f <sub>MOD</sub>      | Lexmark Modulation                                              | 25             |     | 45             | KHz    | 1     |
| OE# Latency                                | t <sub>LATOE#</sub>   | DIF start after OE# assertion<br>DIF stop after OE# deassertion | 1              |     | 3              | cycles | 1,2   |
| PLL Bandwidth                              | BW                    | PLL Bandwidth when PLL_BW=0                                     | 400            | 500 | 1000           | KHz    | 1     |
|                                            |                       | PLL Bandwidth when PLL_BW=1                                     | 2              | 2.5 | 3              | MHz    | 1     |
| SMBus Voltage                              | V <sub>DD</sub>       |                                                                 | 2.7            |     | 5.5            | V      | 1     |
| Low-level Output Voltage                   | V <sub>OL</sub> SMBUS | @ I <sub>PULLUP</sub>                                           |                |     | 0.4            | V      | 1     |
| Current sinking at V <sub>OL</sub> = 0.4 V | I <sub>PULLUP</sub>   | SMBus SDATA pin                                                 | 4              |     |                | mA     | 1     |
| SCLK/SDATA Clock/Data Rise Time            | T <sub>RI2C</sub>     | (Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15)    |                |     | 1000           | ns     | 1     |
| SCLK/SDATA Clock/Data Fall Time            | T <sub>FI2C</sub>     | (Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15)    |                |     | 300            | ns     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Time from deassertion until outputs are >200mV

## Electrical Characteristics - PCIEX 0.7V Current Mode Differential Pair

$T_A = T_{\text{ambient}}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\Omega$

| PARAMETER                       | SYMBOL                   | CONDITIONS                                               | MIN    | TYP | MAX     | UNITS    | NOTES |
|---------------------------------|--------------------------|----------------------------------------------------------|--------|-----|---------|----------|-------|
| Current Source Output Impedance | $Z_O$                    | $V_O = V_x$                                              | 3000   |     |         | $\Omega$ | 1     |
| Voltage High                    | VHigh                    | Statistical measurement on single ended signal using     | 660    |     | 850     | mV       | 1,3   |
| Voltage Low                     | VLow                     |                                                          | -150   |     | 150     |          | 1,3   |
| Max Voltage                     | Vovs                     | Measurement on single ended signal using absolute value. |        |     | 1150    | mV       | 1,3   |
| Min Voltage                     | Vuds                     |                                                          | -300   |     |         |          | 1,3   |
| Crossing Voltage (abs)          | Vcross(abs)              |                                                          | 250    | 350 | 550     | mV       | 1,3   |
| Crossing Voltage (var)          | d-Vcross                 | Variation of crossing over all edges                     |        | 12  | 140     | mV       | 1,3   |
| Long Accuracy                   | ppm                      | see Tperiod min-max values                               |        |     | 0       | ppm      | 1,2   |
| Average period                  | Tperiod                  | 100.00MHz nominal                                        | 9.9970 |     | 10.0030 | ns       | 2     |
|                                 |                          | 100.00MHz spread                                         | 9.9970 |     | 10.0533 | ns       | 2     |
| Absolute min period             | Tabsmin                  | 100.00MHz nominal/spread                                 | 9.8720 |     |         | ns       | 1,2   |
| Rise Time                       | $t_r$                    | $V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$      | 175    |     | 700     | ps       | 1     |
| Fall Time                       | $t_f$                    | $V_{OH} = 0.525\text{V}$ , $V_{OL} = 0.175\text{V}$      | 175    |     | 700     | ps       | 1     |
| Rise Time Variation             | d- $t_r$                 |                                                          |        | 30  | 125     | ps       | 1     |
| Fall Time Variation             | d- $t_f$                 |                                                          |        | 30  | 125     | ps       | 1     |
| Input to Output Delay           | $t_{pd}$                 | PLL Mode.                                                | 0      |     | 150     | ps       | 1     |
|                                 | $t_{pdbyp}$              | Bypass mode                                              | 3.7    |     | 4.2     | ns       | 1     |
| Duty Cycle                      | $d_{t3}$                 | Measurement from differential waveform                   | 45     |     | 55      | %        | 1     |
| Output-to-Output Skew           | $t_{sk3}$                | $V_T = 50\%$                                             |        |     | 25      | ps       | 1     |
| Jitter, Cycle to cycle          | $t_{j\text{cyc-cyc}}$    | PLL mode. Measurement from differential waveform         |        |     | 35      | ps       | 1     |
|                                 | $t_{j\text{cyc-cycbyp}}$ | Additive Jitter in Bypass Mode                           |        |     | 30      | ps       | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup> The 9DB102 does not add a ppm error to the input clock

<sup>3</sup> $I_{REF} = V_{DD}/(3 \times R_R)$ . For  $R_R = 475\Omega$  (1%),  $I_{REF} = 2.32\text{mA}$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7\text{V}$  @  $Z_O = 50\Omega$ .

## Electrical Characteristics - PLL Parameters

$T_A$  = Tambient; Supply Voltage  $V_{DD} = 3.3\text{ V} \pm 5\%$

| Group              | Parameter              | Description                                                             | Min | Typ | Max | Units  | Notes |
|--------------------|------------------------|-------------------------------------------------------------------------|-----|-----|-----|--------|-------|
| PLL Jitter Peaking | $j_{\text{peak-hibw}}$ | (PLL_BW = 1)                                                            | 0   | 1   | 2.5 | dB     | 1,4   |
| PLL Jitter Peaking | $j_{\text{peak-lobw}}$ | (PLL_BW = 0)                                                            | 0   | 1   | 2   | dB     | 1,4   |
| PLL Bandwidth      | $p_{\text{ll\_HIBW}}$  | (PLL_BW = 1)                                                            | 2   | 2.5 | 3   | MHz    | 1,5   |
| PLL Bandwidth      | $p_{\text{ll\_LOBW}}$  | (PLL_BW = 0)                                                            | 0.4 | 0.5 | 1   | MHz    | 1,5   |
| Jitter, Phase      | $t_{\text{jphasePLL}}$ | PCIe Gen 1 phase jitter<br>(1.5 - 22 MHz)                               |     | 40  | 108 | ps     | 1,2,3 |
|                    |                        | PCIe Gen 2 jitter<br>(8-16 MHz, 5-16 MHz) Hi-Band >1.5MHz<br>(PLL_BW=1) |     | 2.7 | 3.1 | ps rms | 1,2,3 |
|                    |                        | PCIe Gen 2 jitter<br>(8-16 MHz, 5-16 MHz) Hi-Band >1.5MHz<br>(PLL_BW=0) |     | 2.2 | 3.1 | ps rms | 1,2,3 |
|                    |                        | PCIe Gen 2 jitter<br>(8-16 MHz, 5-16 MHz) Lo-Band <1.5MHz               |     | 1.3 | 3   | ps rms | 1,2,3 |

### NOTES:

1. Guaranteed by design and characterization, not 100% tested in production.
2. See <http://www.pcisig.com> for complete specs
3. Device driven by 932S421BGLF or equivalent
4. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
5. Measured at 3 db down or half power point.

| SRC Reference Clock                             |  |                    |             |
|-------------------------------------------------|--|--------------------|-------------|
| Common Recommendations for Differential Routing |  | Dimension or Value | Unit Figure |
| L1 length, route as non-coupled 50ohm trace     |  | 0.5 max            | inch 1      |
| L2 length, route as non-coupled 50ohm trace     |  | 0.2 max            | inch 1      |
| L3 length, route as non-coupled 50ohm trace     |  | 0.2 max            | inch 1      |
| Rs                                              |  | 33                 | ohm 1       |
| Rt                                              |  | 49.9               | ohm 1       |

| Down Device Differential Routing                                 |  |                     |        |
|------------------------------------------------------------------|--|---------------------|--------|
| L4 length, route as coupled microstrip 100ohm differential trace |  | 2 min to 16 max     | inch 1 |
| L4 length, route as coupled stripline 100ohm differential trace  |  | 1.8 min to 14.4 max | inch 1 |

| Differential Routing to PCI Express Connector                    |  |                       |        |
|------------------------------------------------------------------|--|-----------------------|--------|
| L4 length, route as coupled microstrip 100ohm differential trace |  | 0.25 to 14 max        | inch 2 |
| L4 length, route as coupled stripline 100ohm differential trace  |  | 0.225 min to 12.6 max | inch 2 |

Figure 1: Down Device Routing

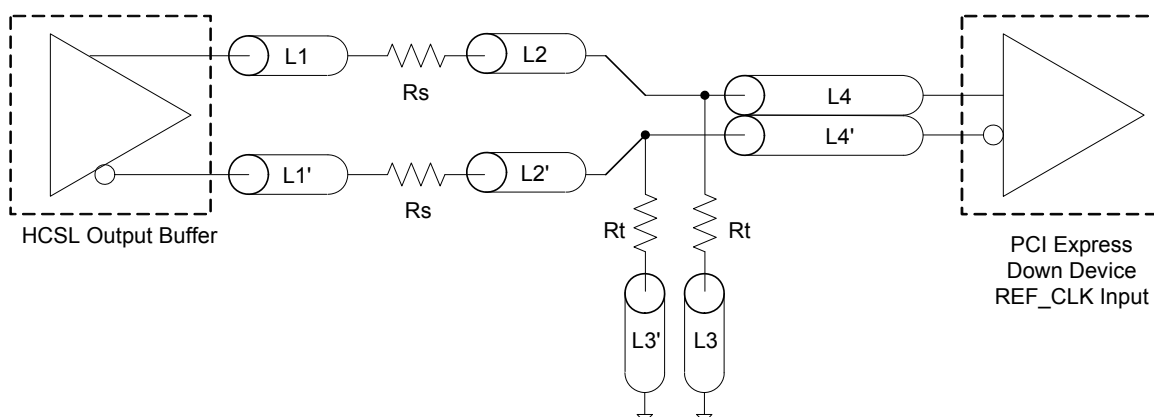
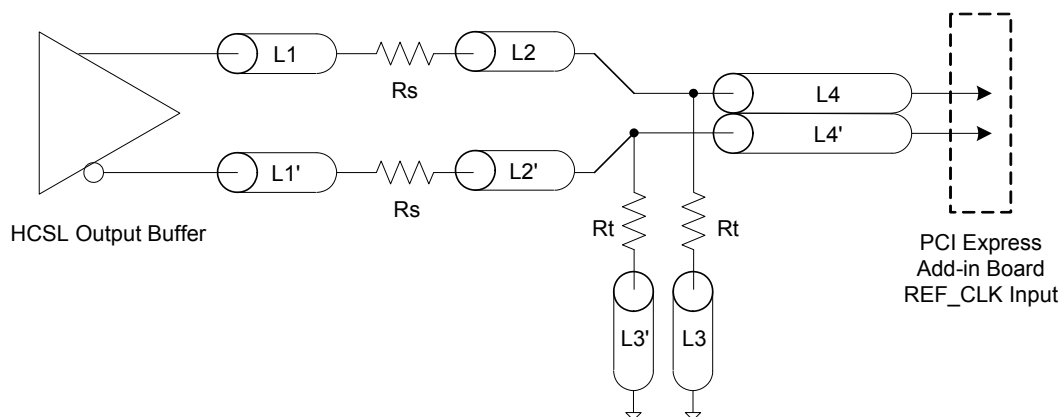


Figure 2: PCI Express Connector Routing



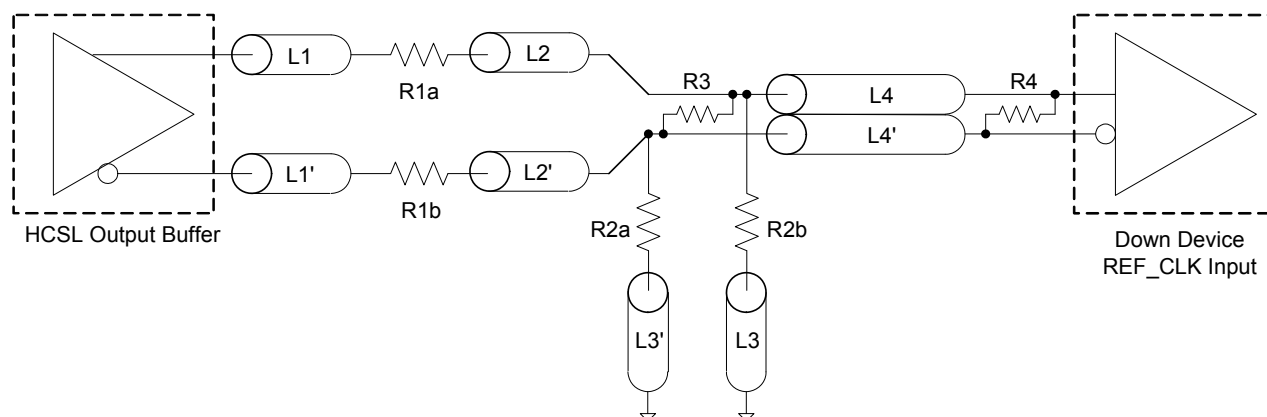
**Alternative Termination for LVDS and other Common Differential Signals (figure 3)**

| V <sub>diff</sub> | V <sub>p-p</sub> | V <sub>cm</sub> | R1 | R2   | R3   | R4  | Note                           |
|-------------------|------------------|-----------------|----|------|------|-----|--------------------------------|
| 0.45v             | 0.22v            | 1.08            | 33 | 150  | 100  | 100 |                                |
| 0.58              | 0.28             | 0.6             | 33 | 78.7 | 137  | 100 |                                |
| 0.80              | 0.40             | 0.6             | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60              | 0.3              | 1.2             | 33 | 174  | 140  | 100 | Standard LVDS                  |

R1a = R1b = R1

R2a = R2b = R2

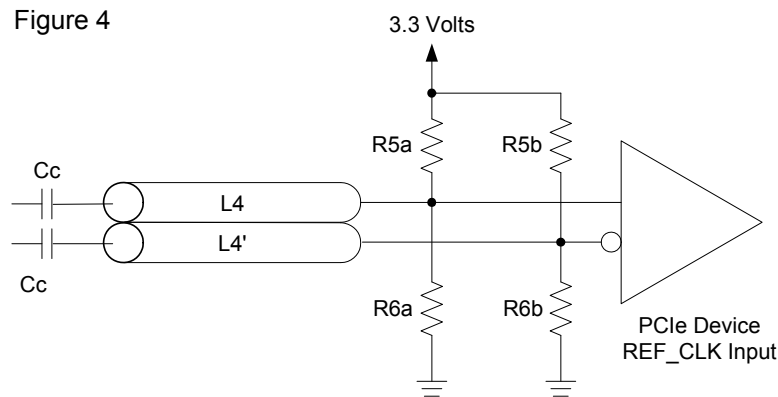
**Figure 3**



**Cable Connected AC Coupled Application (figure 4)**

| Component       | Value       | Note |
|-----------------|-------------|------|
| R5a, R5b        | 8.2K 5%     |      |
| R6a, R6b        | 1K 5%       |      |
| Cc              | 0.1 $\mu$ F |      |
| V <sub>cm</sub> | 0.350 volts |      |

**Figure 4**



## General SMBus serial interface information for the ICS9DB102

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $D4_{(h)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $D4_{(h)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $D5_{(h)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if  $X_{(h)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation     |           |                      |
|---------------------------------|-----------|----------------------|
| Controller (Host)               |           | IDT (Slave/Receiver) |
| T                               | starT bit |                      |
| Slave Address D4 <sub>(h)</sub> |           |                      |
| WR                              | WRite     |                      |
|                                 |           | ACK                  |
| Beginning Byte = N              |           |                      |
|                                 |           | ACK                  |
| Data Byte Count = X             |           |                      |
|                                 |           | ACK                  |
| Beginning Byte N                | X Byte    |                      |
|                                 |           | ACK                  |
| ◊                               |           |                      |
| ◊                               |           | ◊                    |
| ◊                               |           | ◊                    |
|                                 |           | ◊                    |
|                                 |           | ◊                    |
| Byte N + X - 1                  |           |                      |
|                                 |           | ACK                  |
| P                               | stoP bit  |                      |

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address $D4_{(h)}$   |                 |                      |
| WR                         | WRite           |                      |
|                            |                 | ACK                  |
| Beginning Byte = N         |                 |                      |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address $D5_{(h)}$   |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
|                            |                 | Data Byte Count = X  |
| ACK                        |                 |                      |
|                            |                 | Beginning Byte N     |
| ACK                        |                 |                      |
| ◊                          | X Byte          | ◊                    |
| ◊                          |                 | ◊                    |
| ◊                          |                 | ◊                    |
| ◊                          |                 |                      |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

**SMBus Table: Device Control Register, READ/WRITE ADDRESS (D4/D5)**

| Byte 0 | Pin # | Name           | Control Function            | Type | 0                                       | 1                                   | PWD |
|--------|-------|----------------|-----------------------------|------|-----------------------------------------|-------------------------------------|-----|
| Bit 7  | -     | SW_EN          | Enables SMBus Control       | RW   | Functions controlled by SMBus registers | Functions controlled by device pins | 1   |
| Bit 6  | -     | RESERVED       |                             | RW   | -                                       | -                                   | X   |
| Bit 5  | -     | RESERVED       |                             | RW   | -                                       | -                                   | X   |
| Bit 4  | -     | RESERVED       |                             | RW   | -                                       | -                                   | X   |
| Bit 3  | -     | RESERVED       |                             | RW   | -                                       | -                                   | X   |
| Bit 2  | -     | RESERVED       |                             | RW   | -                                       | -                                   | X   |
| Bit 1  | -     | PLL BW #adjust | Selects PLL Bandwidth       | RW   | Low BW                                  | High BW                             | 1   |
| Bit 0  | -     | PLL Enable     | Bypasses PLL for board test | RW   | PLL bypassed (fan out mode)             | PLL enabled (ZDB mode)              | 1   |

**SMBus Table: Output Enable Register**

| Byte 1 | Pin # | Name     | Control Function | Type | 0 | 1 | PWD |
|--------|-------|----------|------------------|------|---|---|-----|
| Bit 7  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 6  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 5  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 4  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 3  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 2  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 1  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 0  | -     | RESERVED |                  | RW   | - | - | X   |

**SMBus Table: Function Select Register**

| Byte 2 | Pin # | Name     | Control Function | Type | 0 | 1 | PWD |
|--------|-------|----------|------------------|------|---|---|-----|
| Bit 7  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 6  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 5  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 4  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 3  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 2  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 1  | -     | RESERVED |                  | RW   | - | - | X   |
| Bit 0  | -     | RESERVED |                  | RW   | - | - | X   |

**SMBus Table: Vendor & Revision ID Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7  | -     | RID3 | REVISION ID      | R    | - | - | 0   |
| Bit 6  | -     | RID2 |                  | R    | - | - | 0   |
| Bit 5  | -     | RID1 |                  | R    | - | - | 0   |
| Bit 4  | -     | RID0 |                  | R    | - | - | 1   |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | - | - | 0   |
| Bit 2  | -     | VID2 |                  | R    | - | - | 0   |
| Bit 1  | -     | VID1 |                  | R    | - | - | 0   |
| Bit 0  | -     | VID0 |                  | R    | - | - | 1   |

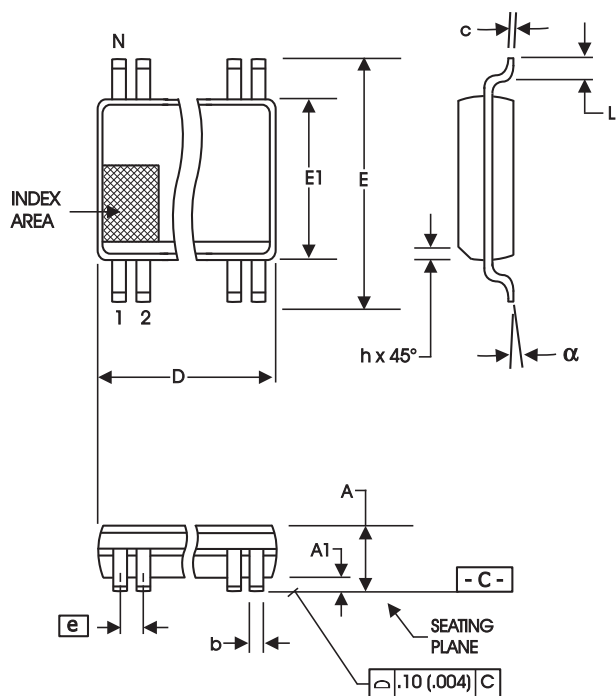
**SMBus Table: DEVICE ID**

| Byte 4 | Pin # | Name                  | Control Function | Type | 0 | 1 | PWD |
|--------|-------|-----------------------|------------------|------|---|---|-----|
| Bit 7  | -     | Device ID<br>= 06 Hex |                  | R    | - | - | 0   |
| Bit 6  | -     |                       |                  | R    | - | - | 0   |
| Bit 5  | -     |                       |                  | R    | - | - | 0   |
| Bit 4  | -     |                       |                  | R    | - | - | 0   |
| Bit 3  | -     |                       |                  | R    | - | - | 0   |
| Bit 2  | -     |                       |                  | R    | - | - | 1   |
| Bit 1  | -     |                       |                  | R    | - | - | 1   |
| Bit 0  | -     |                       |                  | R    | - | - | 0   |

**SMBus Table: Byte Count Register**

| Byte 5 | Pin # | Name | Control Function                                                                                   | Type | 0 | 1 | PWD |
|--------|-------|------|----------------------------------------------------------------------------------------------------|------|---|---|-----|
| Bit 7  | -     | BC7  | Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes. | RW   | - | - | 0   |
| Bit 6  | -     | BC6  |                                                                                                    | RW   | - | - | 0   |
| Bit 5  | -     | BC5  |                                                                                                    | RW   | - | - | 0   |
| Bit 4  | -     | BC4  |                                                                                                    | RW   | - | - | 0   |
| Bit 3  | -     | BC3  |                                                                                                    | RW   | - | - | 0   |
| Bit 2  | -     | BC2  |                                                                                                    | RW   | - | - | 1   |
| Bit 1  | -     | BC1  |                                                                                                    | RW   | - | - | 1   |
| Bit 0  | -     | BC0  |                                                                                                    | RW   | - | - | 0   |

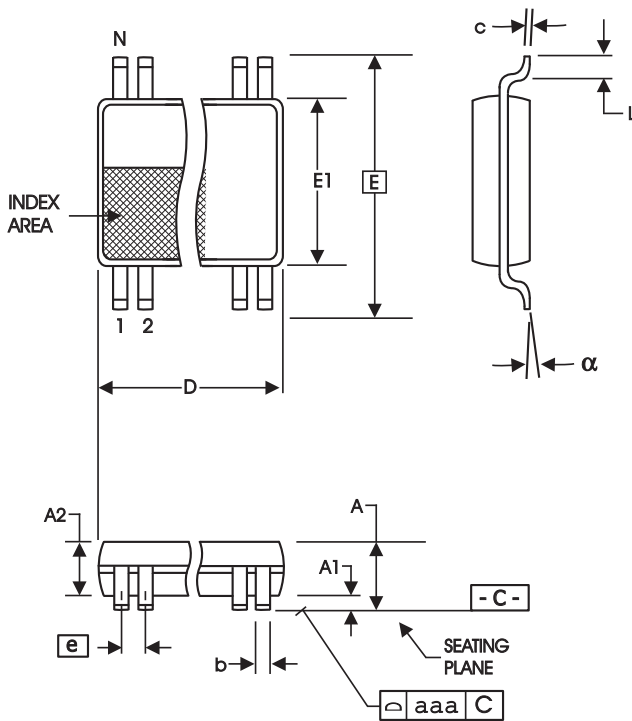
## 20-Pin SSOP Package Drawing and Dimensions



20-Lead, 150 mil SSOP (QSOP)

| SYMBOL | In Millimeters    |      | In Inches         |      |
|--------|-------------------|------|-------------------|------|
|        | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|        | MIN               | MAX  | MIN               | MAX  |
| A      | 1.35              | 1.75 | .053              | .069 |
| A1     | 0.10              | 0.25 | .004              | .010 |
| A2     | --                | 1.50 | --                | .059 |
| b      | 0.20              | 0.30 | .008              | .012 |
| c      | 0.18              | 0.25 | .007              | .010 |
| D      | 8.55              | 8.75 | .337              | .344 |
| E      | 5.80              | 6.20 | .228              | .244 |
| E1     | 3.80              | 4.00 | .150              | .157 |
| e      | 0.635 BASIC       |      | 0.025 BASIC       |      |
| L      | 0.40              | 1.27 | .016              | .050 |
| N      | 20                |      | 20                |      |
| a      | 0°                | 8°   | 0°                | 8°   |
| ZD     | 1.47              |      | .058              |      |

## 20-Pin TSSOP Package Drawing and Dimensions



20-Lead, 4.40 mm. Body, 0.65 mm. Pitch TSSOP  
(173 mil) (25.6 mil)

| SYMBOL | In Millimeters    |      | In Inches         |      |
|--------|-------------------|------|-------------------|------|
|        | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|        | MIN               | MAX  | MIN               | MAX  |
| A      | --                | 1.20 | --                | .047 |
| A1     | 0.05              | 0.15 | .002              | .006 |
| A2     | 0.80              | 1.05 | .032              | .041 |
| b      | 0.19              | 0.30 | .007              | .012 |
| c      | 0.09              | 0.20 | .0035             | .008 |
| D      | 6.40              | 6.60 | .252              | .260 |
| E      | 6.40 BASIC        |      | 0.252 BASIC       |      |
| E1     | 4.30              | 4.50 | .169              | .177 |
| e      | 0.65 BASIC        |      | 0.0256 BASIC      |      |
| L      | 0.45              | 0.75 | .018              | .030 |
| N      | 20                |      | 20                |      |
| a      | 0°                | 8°   | 0°                | 8°   |
| aaa    | --                | 0.10 | --                | .004 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

## Ordering Information

| Part / Order Number | Shipping Packaging | Package      | Temperature  |
|---------------------|--------------------|--------------|--------------|
| 9DB102BFLF          | Tubes              | 20-pin SSOP  | 0 to +70°C   |
| 9DB102BFLFT         | Tape and Reel      | 20-pin SSOP  | 0 to +70°C   |
| 9DB102BFILF         | Tubes              | 20-pin SSOP  | -40 to +85°C |
| 9DB102BFILFT        | Tape and Reel      | 20-pin SSOP  | -40 to +85°C |
| 9DB102BGLF          | Tubes              | 20-pin TSSOP | 0 to +70°C   |
| 9DB102BGLFT         | Tape and Reel      | 20-pin TSSOP | 0 to +70°C   |
| 9DB102BGILF         | Tubes              | 20-pin TSSOP | -40 to +85°C |
| 9DB102BGILFT        | Tape and Reel      | 20-pin TSSOP | -40 to +85°C |

"LF" after the package code are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate to the datasheet revision).

## Revision History

| Rev. | Originator | Issue Date | Description                                                                                                                                         | Page #  |
|------|------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| F    |            | 8/6/2007   | 1. Added Phase Noise Parameters, Updated input to output delay values.<br>2. PLL BW moved to PLL parameters table.<br>3. Added terminations tables. | Various |
| G    |            | 12/14/2007 | Updated General SMBus Interface Information.                                                                                                        | 8       |
| H    |            | 10/29/2008 | Corrected "HCSL" typos.                                                                                                                             | 1, 6, 7 |
| J    |            | 1/15/2010  | 1. Added I-temp electricals<br>2. Changed datasheet title<br>3. Updated Input Frequency parameter<br>4. Updated ordering information                | Various |
| K    | RW         | 4/1/2010   | Updated ordering info for Rev B                                                                                                                     |         |
| L    | DC         | 9/28/2010  | Updated package dimension tables                                                                                                                    | 11, 12  |
| M    | RDW        | 1/27/2011  | Updated Termination Figure 4.                                                                                                                       | 7       |
| N    | RDW        | 4/20/2011  | Changed pulldown indicator on CLKREQ# pins to correct pin description of those pins.                                                                |         |
| P    | AT         | 5/24/2012  | Added OE# Latency spec to Common Input/Output Parameters table                                                                                      | 3       |
| Q    | J. Chao    | 8/27/2013  | Updated PLL Bandwidth specs per latest characterization data,                                                                                       | 3       |

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