



Programmable System Frequency Generator for PII/III™

Recommended Application:

BX, Appollo Pro 133 type of chip set.

Output Features:

- 3 - CPUs @ 2.5V, up to 166MHz.
- 17 - SDRAM @ 3.3V, up to 166MHz.
- 7 - PCI @ 3.3V
- 2 - IOAPIC @ 2.5V
- 1 - 48MHz, @ 3.3V fixed.
- 1 - 24MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz.

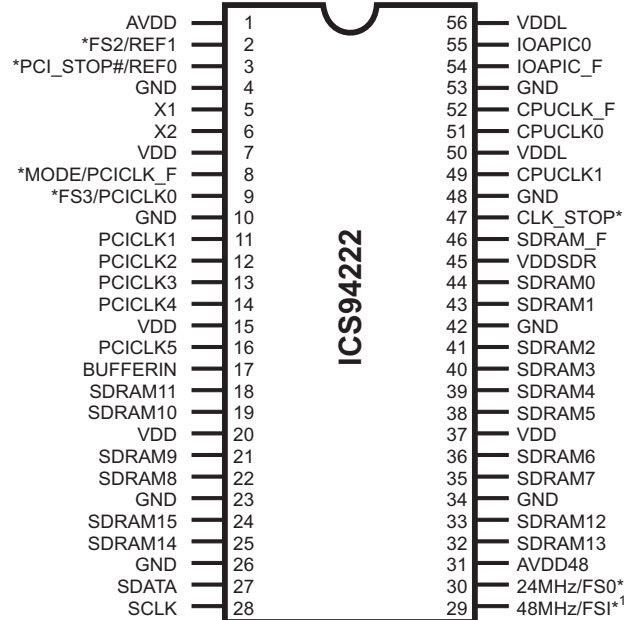
Features:

- Programmable output frequency.
- Programmable output rise/fall time.
- Programmable PCI_F and PCICLK skew.
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage.
- Watchdog timer technology to reset system if over-clocking causes malfunction.
- Uses external 14.318MHz crystal.
- FS pins for frequency select

Key Specifications:

- CPU – CPU: <175ps
- SDRAM - SDRAM: <500ps
- PCI – PCI: <500ps
- CPU-SDRAM: <500ps
- CPU(early)-PCI: Min=1.0ns, Typ=2.0ns, Max=4.0ns

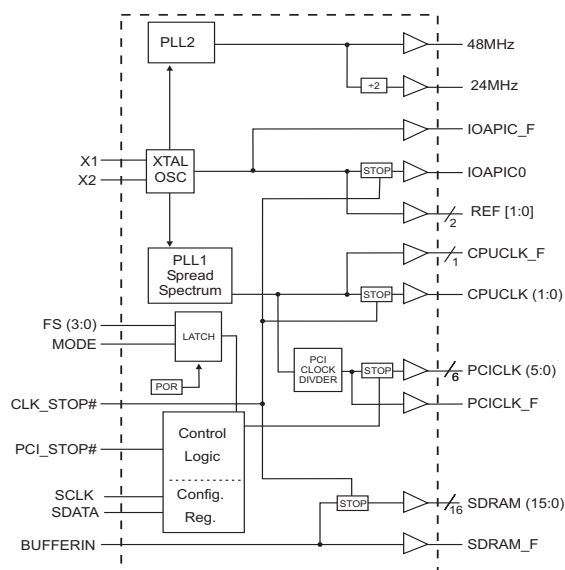
Pin Configuration



56-Pin SSOP

* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	PCICLK (MHz)
0	0	0	0	80.00	40.00
0	0	0	1	75.00	37.50
0	0	1	0	83.31	41.65
0	0	1	1	66.9	33.45
0	1	0	0	103.00	34.33
0	1	0	1	112.01	37.34
0	1	1	0	68.01	34.01
0	1	1	1	100.7	33.57
1	0	0	0	120.00	40.00
1	0	0	1	114.99	38.33
1	0	1	0	109.99	36.66
1	0	1	1	105.00	35.00
1	1	0	0	140.00	35.00
1	1	0	1	150.00	37.50
1	1	1	0	124.00	31.00
1	1	1	1	133.9	33.25



Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	AVDD	PWR	Analog power supply 3.3V
2	REF1	OUT	14.318 MHz reference clock output
	FS2 ¹	IN	Latched frequency select input. Has pull-up to VDD
3	REF0	OUT	14.318MHz reference clock output
	PCI_STOP# ¹	IN	Halts PCICLK [5:1] at logic "0" level when low. (in mobile, MODE=0)
4, 10, 23, 26, 34, 42, 48, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap, (nominal 33pF).
6	X2	OUT	Crystal output. Has internal load cap (33pF) and feedback resistor to X1
7, 15, 20, 37, 45	VDD	PWR	Nominal 3.3V power supply, see power groups for function.
8	PCICLK_F	OUT	Free running BUS clock not affected by PCI_STOP#
	MODE ¹	IN	Latched input for MODE select. Converts pin 3 to PCI_STOP# when low for power management.
9	FS3 ¹	IN	Latched frequency select input, pull-down
	PCICLK0	OUT	Free running BUS clock not affected by PCI_STOP#
16, 14, 13, 12, 11	PCICLK (5:1)	OUT	PCI Clock Outputs.
17	BUFFERIN	IN	Input for Buffers
27	SDATA	IN	Serial data in for serial config port. (I ² C)
28	SCLK	IN	Clock input for serial config port. (I ² C)
30	24MHz	OUT	24MHz clock output for Super I/O or FD.
	FS0 ¹	IN	Latched frequency select input. Has pull-up to VDD
29	48MHz	OUT	48MHz clock output for USB, 2X strength.
	FS1 ¹	IN	Latched frequency select input. Has pull-up to VDD
31	AVDD48	PWR	Analog power supply 3.3V
24, 25, 32, 33, 18, 19, 21, 22, 35, 36, 38, 39, 40, 41, 43, 44	SDRAM (15:0)	OUT	SDRAM clocks
46	SDRAM_F	OUT	Free running SDRAM clock Not affected by CPU_STOP#
47	CLK_STOP#	IN	Halts CPUCLKs, IOAPIC0, SDRAMs clocks at logic "0" level when low.
50, 56	VDDL	PWR	CPU and IOAPIC clock buffer power supply, 2.5V nominal.
55	IOAPIC0	OUT	IOAPIC clock output. (14.318 MHz) Poweredby VDDL
49, 51	CPUCLK (1:0)	OUT	CPU Output clocks. Powered by VDDL (60 or 66.6MHz)
52	CPUCLK_F	OUT	Free running CPU output clock. Not affected ty the CLK_STOP#.
54	IOAPIC_F	OUT	Freerunning IOAPIC clock output. Not affected by the CLK_STOP# (14.31818 MHz) Powered by VDDL

Notes:

- 1: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



General Description

The **ICS94222** is a single chip clock solution for desktop designs using the BX/Apollo Pro133/ALI 1631 style chipset. It provides all necessary clock signals for such a system.

The **ICS94222** belongs to ICS new generation of programmable system clock generators. It employs serial programming I²C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

Mode Pin - Power Management Input Control

MODE (Latched Input)	Pin 3
0	PCI_STOP# (Input)
1	REF0 (Output)

Power Groups

AVDD48 = 48MHz, Fixed PLL

AVDD = CPU PLL, XTAL



General I²C serial interface information for the ICS94222

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte 0 through Byte 20** (see Note)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 _(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends **Byte 0 through byte 8 (default)**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 _(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7 _H has been written to B6	Byte 7
ACK	
○	○
○	○
○	○
If 12 _H has been written to B6	Byte 18
ACK	
If 13 _H has been written to B6	Byte 19
ACK	
If 14 _H has been written to B6	Byte 20
ACK	
Stop Bit	



Brief I²C registers description for ICS94222 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I ² C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00 _H to this byte.	08 _H
Watchdog Control Registers	9 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	9 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
Watchdog Timer Count Register	10	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10 _H
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.



Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description							PWD
Bit 2,7, 6:4	Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK MHz	PCICLK MHz	XXXX Note1
	0	0	0	0	0	80.00	40.00	
	0	0	0	0	1	75.00	37.50	
	0	0	0	1	0	83.31	41.65	
	0	0	0	1	1	66.9	33.45	
	0	0	1	0	0	103.00	34.33	
	0	0	1	0	1	112.01	37.34	
	0	0	1	1	0	68.01	34.01	
	0	0	1	1	1	100.7	33.57	
	0	1	0	0	0	120.00	40.00	
	0	1	0	0	1	114.99	38.33	
	0	1	0	1	0	109.99	36.66	
	0	1	0	1	1	105.00	35.00	
	0	1	1	0	0	140.00	35.00	
	0	1	1	0	1	150.00	37.50	
	0	1	1	1	0	124.00	31.00	
	0	1	1	1	1	133.9	33.25	
	1	0	0	0	0	135.00	33.75	
	1	0	0	0	1	129.99	32.50	
	1	0	0	1	0	126.00	31.50	
	1	0	0	1	1	118.00	39.33	
	1	0	1	0	0	115.98	38.66	
	1	0	1	0	1	95.00	31.67	
	1	0	1	1	0	90.00	30.00	
	1	0	1	1	1	85.01	28.34	
	1	1	0	0	0	166.00	41.50	
	1	1	0	0	1	160.01	40.00	
	1	1	0	1	0	154.99	38.75	
	1	1	0	1	1	147.95	36.99	
	1	1	1	0	0	145.98	36.50	
	1	1	1	0	1	143.98	35.99	
	1	1	1	1	0	141.99	35.50	
	1	1	1	1	1	138.01	34.50	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2, 7:4							0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled $\pm 0.25\%$ (Center Spread)							1
Bit 0	0 - Running 1- Tristate all outputs							0

Note 1. Default at Power-up will be for latched logic inputs to define frequency as displayed by Bit 3.

Note: PWD = Power-Up Default

**Byte 1: CPU, Active/Inactive Register**
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	46	1	SDRAM_F (Act/Inact)
Bit 2	49	1	CPUCLK1 (Act/Inact)
Bit 1	51	1	CPUCLK0 (Act/Inact)
Bit 0	52	1	CPUCLK_F (Act/Inact)

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	29	1	48MHz (Act/Inact)
Bit 4	30	1	24MHz (Act/Inact)
Bit 3	33, 32, 25, 24	1	SDRAM (15:12) (Act/Inact)
Bit 2	22, 21, 19, 18	1	SDRAM (11:8) (Act/Inact)
Bit 1	39, 38, 36, 35	1	SDRAM (7:4) (Act/Inact)
Bit 0	44, 43, 41, 40	1	SDRAM (3:0) (Act/Inact)

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	X	Latched FS2#
Bit 5	54	1	IOAPIC_F (Act/Inact)
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	2	1	REF1 (Act/Inact)
Bit 0	3	1	REF0 (Act/Inact)

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLK_F (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Latched FS0#
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	X	Latched FS1#
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	X	Latched FS3#
Bit 0	-	1	Reserved

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: This is an unused register writing to this register will not affect device performance or functionality.

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.



Byte 7: Vendor ID and Revision ID Register

Bit	PWD	Description
Bit 7	0	Vendor ID
Bit 6	0	Vendor ID
Bit 5	1	Vendor ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

Byte 8: Byte Count and Read Back Register

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	1	Reserved
Bit 2	0	Reserved
Bit 1	0	Reserved
Bit 0	0	Reserved

Byte 9: VCO Control Selection Bit & Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B14&15 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	0	WD Safe Frequency, Byte 0 bit 2
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit [0:4] will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 10: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to 290ms or 1ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16X 290ms = 4.6 seconds.
Bit 6	0	
Bit 5	0	
Bit 4	1	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

Byte 11: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 [6:0]) + 2 is equal to the REF divider value .

Notes:

1. PWD = Power on Default

Byte 12: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit [7:0] & Byte 11 bit [7]) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program $36 - 8 = 28$, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.



Byte 13: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 14: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bit9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7	0	PCICLK (5:0) Skew Control
Bit 6	1	
Bit 5	1	
Bit 4	0	
Bit 3	0	PCICLK_F Skew Control
Bit 2	1	
Bit 1	1	
Bit 0	0	

Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	CPUCLK_F: Slew Rate Control
Bit 6	0	
Bit 5	1	CPUCLK1: Slew Rate Control
Bit 4	0	
Bit 3	1	SDRAM_F: Slew Rate Control
Bit 2	0	
Bit 1	1	SDRAM (11:0) Slew Rate Control
Bit 0	0	

Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	PCI (4:0) Slew Rate Control
Bit 6	0	
Bit 5	1	PCI_F Slew Rate Control
Bit 4	0	
Bit 3	1	48MHz: Slew Rate Control
Bit 2	0	
Bit 1	1	24MHz: Slew Rate Control
Bit 0	0	

Notes:

1. PWD = Power on Default
2. The power on default for byte 13-20 depends on the hardware (latch inputs FS[0:4]) or I²C (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 8 registers when VCO frequency change is desired for the first pass.
3. If Byte 8 bit 7 is driven to "1" meaning programming is intended, Byte 21-24 will lose their default power up value.



Byte 19: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 20: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Note: Byte 19 and 20 are reserved registers, these are unused registers writing to these registers will not affect device performance or functionality.

VCO Programming Constrains

VCO Frequency 150MHz to 500MHz

VCO Divider Range 8 to 519

REF Divider Range 2 to 129

Phase Detector Stability 0.3536 to 1.4142

Useful Formula

VCO Frequency = $14.31818 \times \text{VCO/REF divider value}$

Phase Detector Stability = $14.038 \times (\text{VCO divider value})^{-0.5}$

To program the VCO frequency for over-clocking.

- Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.
- Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.
- Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).
- Read back byte 11-20 and copy values in these registers.
- Re-initialize the write sequence.
- Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.
- Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.
- The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

- User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.
- If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.
- Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use $14.31818\text{MHz} \times \text{VCO/REF divider values}$ to calculate the VCO frequency (MHz).
- ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.
- Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spreadamount desired. See Application note for software support.



Absolute Maximum Ratings

Supply Voltage.....	7.0 V
Logic Inputs.....	GND –0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Case Temperature	115°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage V_{DD} , $V_{DDL} = 3.3\text{ V} \pm 5\%$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		$V_{SS} - 0.3$		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	μA
Input Low Current	I_{IL1}	$V_{IN} = 0\text{ V}$; Inputs with no pull-up resistors	-5			μA
Input Low Current	I_{IL2}	$V_{IN} = 0\text{ V}$; Inputs with pull-up resistors	-200			μA
Operating Supply Current	$I_{DD3.3OP66}$	$C_L = 0\text{ pF}$; Select @ 66MHz			180	mA
	$I_{DD3.3OP100}$	$C_L = 0\text{ pF}$; Select @ 100MHz				
Input frequency	F_i	$V_{DD} = 3.3\text{ V}$;	12		16	MHz
Input Capacitance ¹	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization ¹	T_{STAB}	From $V_{DD} = 3.3\text{ V}$ to 1% target Freq.			3	ms

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	$C_L = 0\text{ pF}$; Select @ 66.8 MHz			72	mA
	$I_{DD2.5OP100}$	$C_L = 0\text{ pF}$; Select @ 100 MHz			100	
Skew ¹	$t_{CPU-PCI}$	$V_T = 1.5\text{ V}$; $V_{TL} = 1.25\text{ V}$	1.5		4	ns

¹Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - CPUCLK** $T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	$I_{OH} = -12.0 \text{ mA}$	2			V
Output Low Voltage	V_{OL2B}	$I_{OL} = 12 \text{ mA}$			0.4	V
Output High Current	I_{OH2B}	$V_{OH} = 1.7 \text{ V}$			-19	mA
Output Low Current	I_{OL2B}	$V_{OL} = 0.7 \text{ V}$	19			mA
Rise Time	t_{r2B}^1	$V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.0 \text{ V}$			1.6	ns
Fall Time	t_{f2B}^1	$V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.4 \text{ V}$			1.6	ns
Duty Cycle	d_{t2B}^1	$V_T = 1.25 \text{ V}$	45		55	%
Skew	t_{sk2B}^1	$V_T = 1.25 \text{ V}$			175	ps
Jitter, Cycle-to-cycle	$t_{jcy-cyc2B}^1$	$V_T = 1.25 \text{ V}$			250	ps
Jitter, One Sigma	t_{j1s2B}^1	$V_T = 1.25 \text{ V}$			150	ps
Jitter, Absolute	t_{jabs2B}^1	$V_T = 1.25 \text{ V}$	-250		+250	ps

¹Guaranteed by design, not 100% tested in production.**Electrical Characteristics - PCICLK** $T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 30 \text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	$I_{OH} = -11 \text{ mA}$	2.4			V
Output Low Voltage	V_{OL1}	$I_{OL} = 9.4 \text{ mA}$			0.4	V
Output High Current	I_{OH1}	$V_{OH} = 2.0 \text{ V}$			-22	mA
Output Low Current	I_{OL1}	$V_{OL} = 0.8 \text{ V}$	25			mA
Rise Time ¹	t_{r1}	$V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$			2	ns
Fall Time ¹	t_{f1}	$V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$			2	ns
Duty Cycle ¹	d_{t1}	$V_T = 1.5 \text{ V}$	45		55	%
Skew ¹	t_{sk1}	$V_T = 1.5 \text{ V}$			500	ps
Jitter, Cycle-to-cycle	$t_{jcy-cyc2B}^1$	$V_T = 1.5 \text{ V}$			250	ps
Jitter, One Sigma ¹	t_{j1s1}	$V_T = 1.5 \text{ V}$			150	ps
Jitter, Absolute ¹	t_{jabs1}	$V_T = 1.5 \text{ V}$	-500		500	ps

¹Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - SDRAM** $T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	$I_{OH} = -28\text{ mA}$	2.4			V
Output Low Voltage	V_{OL3}	$I_{OL} = 23\text{ mA}$			0.4	V
Output High Current	I_{OH3}	$V_{OH} = 2.0\text{ V}$			-54	mA
Output Low Current	I_{OL3}	$V_{OL} = 0.8\text{ V}$	41			mA
Rise Time	T_{r3}^1	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$			2	ns
Fall Time	T_{f3}^1	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$			2	ns
Duty Cycle	D_{i3}^1	$V_T = 1.5\text{ V}$	45		55	%
Skew ¹	T_{sk1}	$V_T = 1.5\text{ V}$			500	ps
Propagation Delay	T_{prop}	$V_T = 1.5\text{ V}$			5	ns

¹Guaranteed by design, not 100% tested in production.**Electrical Characteristics - IOAPIC** $T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	$I_{OH} = -12\text{ mA}$	2			V
Output Low Voltage	V_{OL4B}	$I_{OL} = 12\text{ mA}$			0.4	V
Output High Current	I_{OH4B}	$V_{OH} = 1.7\text{ V}$			-19	mA
Output Low Current	I_{OL4B}	$V_{OL} = 0.7\text{ V}$	19			mA
Rise Time ¹	T_{r4B}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$			2	ns
Fall Time ¹	T_{f4B}	$V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$			2	ns
Duty Cycle ¹	D_{i4B}	$V_T = 1.25\text{ V}$	45		55	%
Jitter, One Sigma ¹	T_{j1s4B}	$V_T = 1.25\text{ V}$			0.5	ns
Jitter, Absolute ¹	T_{jabs4B}	$V_T = 1.25\text{ V}$	-1		1	ns

¹Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - 24MHz, 48MHz, REF**

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	$I_{OH} = -16\text{ mA}$	2.4			V
Output Low Voltage	V_{OL5}	$I_{OL} = 9\text{ mA}$			0.4	V
Output High Current	I_{OH5}	$V_{OH} = 2.0\text{ V}$			-22	mA
Output Low Current	I_{OL5}	$V_{OL} = 0.8\text{ V}$	16			mA
Rise Time ¹	t_{r5}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$			4	ns
Fall Time ¹	t_{f5}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$			4	ns
Duty Cycle ¹	d_{t5}	$V_T = 1.5\text{ V}$	45		55	%
Jitter, One Sigma ¹	t_{j1s5}	$V_T = 1.5\text{ V}$			0.5	ns
Jitter, Absolute ¹	t_{jab5}	$V_T = 1.5\text{ V}$	-1		1	ns

¹Guaranteed by design, not 100% tested in production.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS94222 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

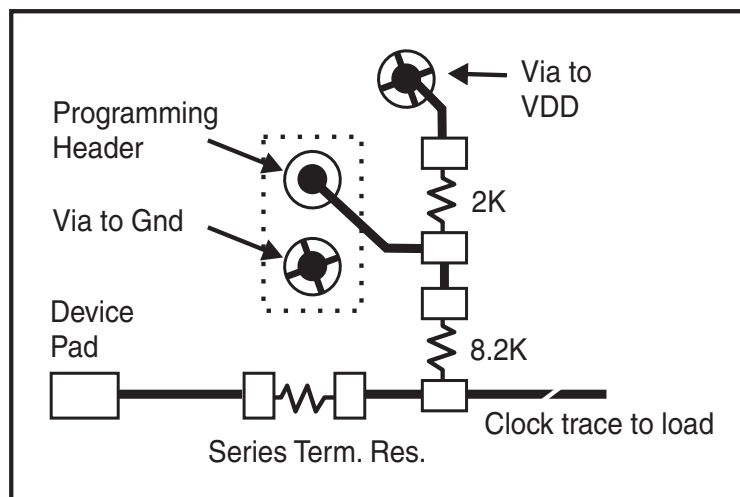
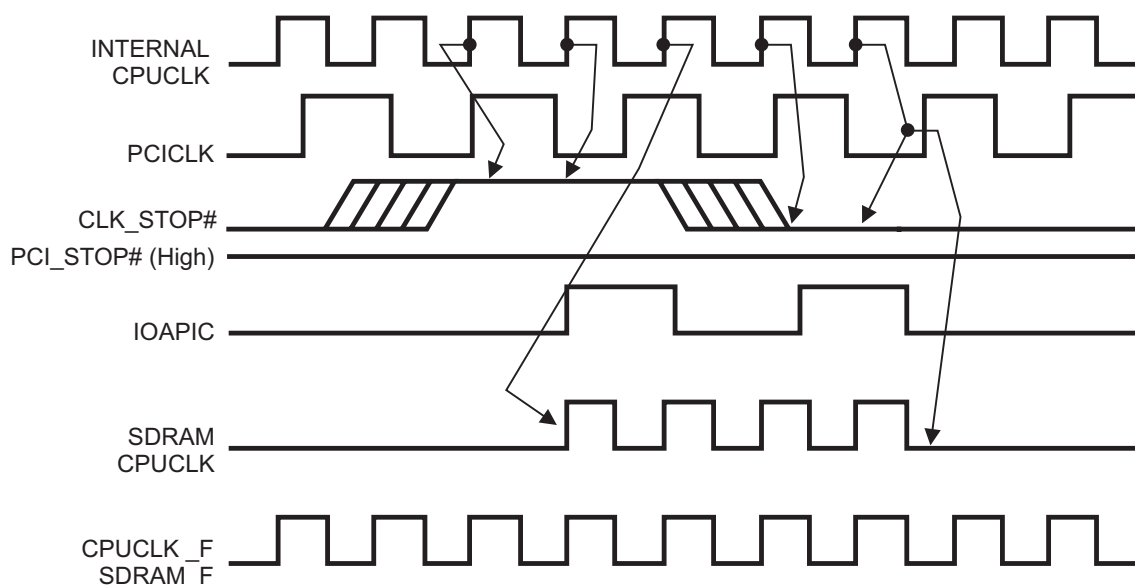


Fig. 1



CLK_STOP# Timing Diagram

CLK_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the ICS94222. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



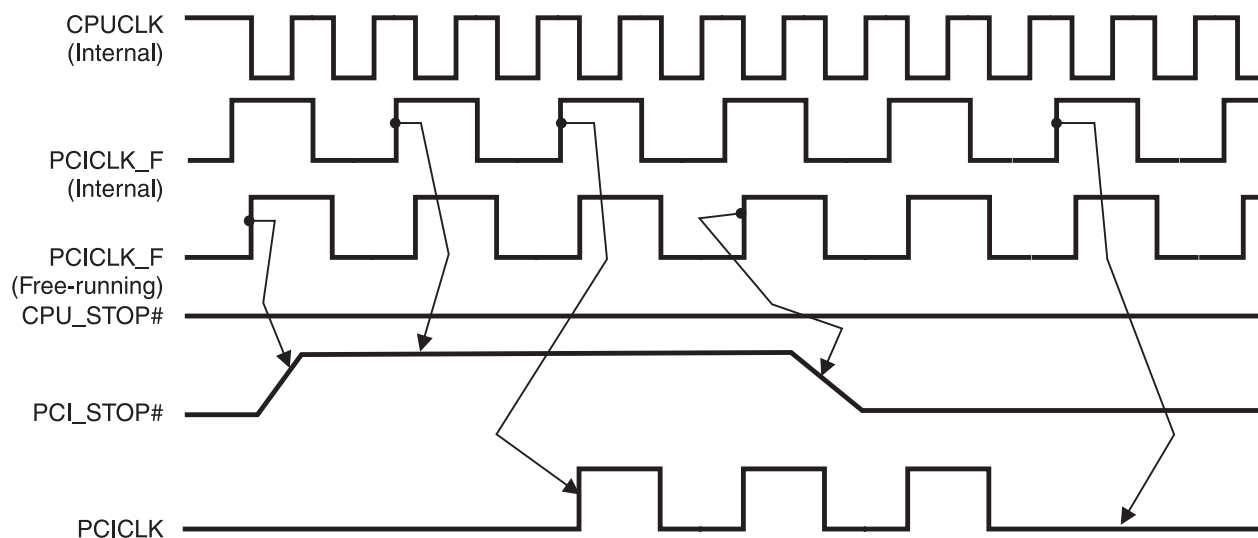
Notes:

1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS94222.
3. IOAPIC output is Stopped Glitch Free by CLK_STOP# going low.
4. SDRAM-F output is controlled by Buffer in signal, not affected by the ICS94222 CLK_STOP# signal. SDRAM's are controlled as shown.
5. All other clocks continue to run undisturbed.



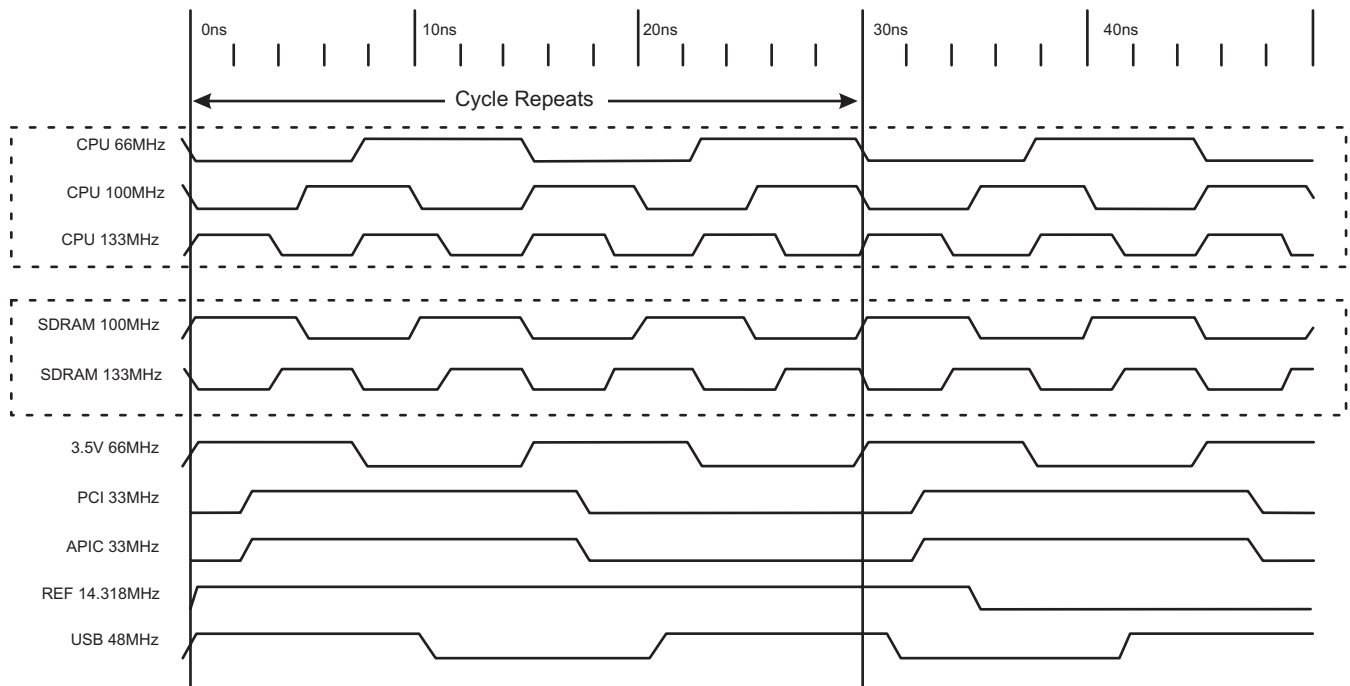
PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS94222**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS94222** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

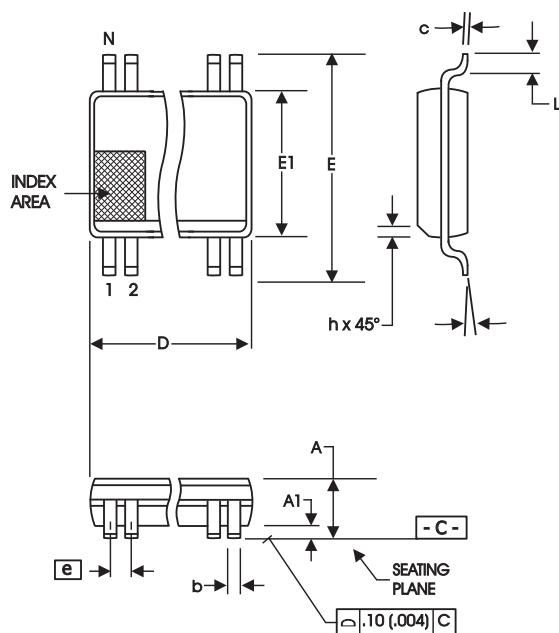


Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94222 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94222.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.



Group Offset Waveforms



300 mil SSOP Package

SYMBOL	In Millimeters		In Inches	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS94222yFT

Example:

ICS XXXX y F - PPP - T

- Prefix
 - Device Type
 - Revision Designator (will not correlate with datasheet revision)
 - Package Type
F=SSOP
 - Pattern Number (2 or 3 digit number for parts with ROM code patterns)
 - Designation for tape and reel packaging
- ICS, AV = Standard Device