Integrated Circuit Systems, Inc.

ICS9250-30

Preliminary Product Preview

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

810/810E and Solano type chipset

Output Features:

- 2 - CPUs @ 2.5V, up to 200MHz.
- 13 - SDRAM @ 3.3V, up to 200MHz.
- 3 - 3V66 @ 3.3V, 2x PCI MHz.
- 8 - PCI @3.3V.
- 1 - 48MHz, @3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 1 - REF @3.3V, 14.318MHz.

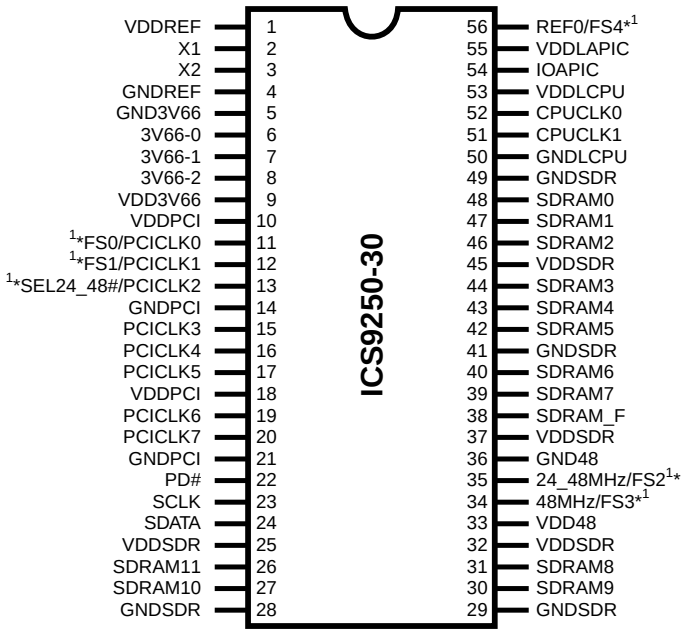
Features:

- Support PC133 SDRAM.
- Up to 200MHz frequency support
- Support power management through PD#.
- Spread spectrum for EMI control (± 0.25% Center Spread or 0 to -0.5% down spread)
- Uses external 14.318MHz crystal
- FS pins for frequency select

Key Specifications:

- CPU Output Jitter: <250ps
- CPU Output Skew: <175ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <175ps
- For group skew timing, please refer to the Group Timing Relationship Table.

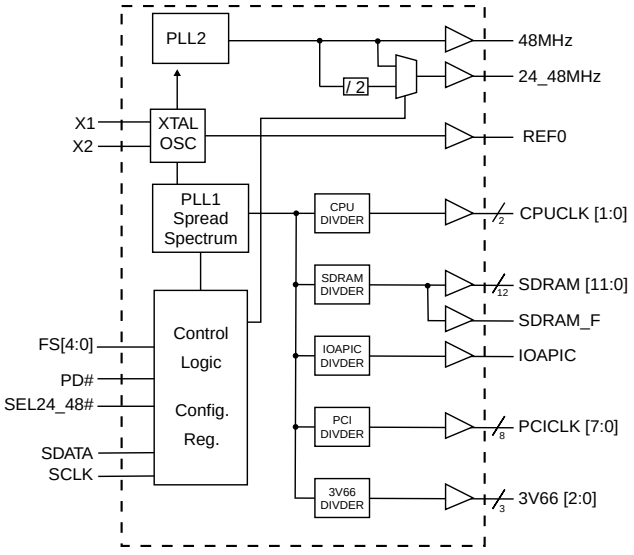
Pin Configuration



56-Pin 300 mil SSOP

1. These pins will have 1.5 to 2X drive strength.
* 120K ohm pull-up to VDD on indicated inputs.

Block Diagram



Functionality

FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	3V66	PCI
0	0	0	0	0	66.67	100.00	66.67	33.33
0	0	0	1	1	68.33	102.50	68.33	34.17
0	0	1	1	0	80.00	120.00	80.00	40.00
0	0	1	1	1	83.00	124.50	83.00	41.50
0	1	0	0	0	100.00	100.00	66.67	33.33
0	1	0	1	1	103.00	103.00	68.67	34.33
0	1	1	1	0	115.00	115.00	76.67	38.33
0	1	1	1	1	200.00	200.00	66.67	33.33
1	0	0	0	0	133.33	133.33	66.67	33.33
1	0	0	0	1	166.67	166.67	83.34	41.67
1	0	0	1	1	137.00	137.00	68.50	34.25
1	0	1	1	1	160.00	160.00	80.00	40.00
1	1	0	0	0	133.33	100.00	66.67	33.33
1	1	0	0	1	166.67	125.00	83.34	41.67
1	1	0	1	1	137.00	102.75	68.50	34.25
1	1	1	1	1	160.00	120.00	80.00	40.00

For other hardware/I^2C selectable frequencies please refer to Byte 0 frequency select register.

General Description

The **ICS9250-30** is a single chip clock solution for desktop designs using the 810/810E and Solano style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-30 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 9, 10, 18, 25, 32, 33, 37, 45	VDD	PWR	3.3V power supply
2	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
3	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
4, 5, 14, 21, 28, 29, 36, 41, 49	GND	PWR	Ground pins for 3.3V supply
8, 7, 6	3V66 [2:0]	OUT	3.3V Fixed 66MHz clock outputs for HUB
11	PCICLK0	OUT	3.3V PCI clock outputs
	FS0	IN	Logic input frequency select bit. Input latched at power on.
12	PCICLK1	IN	3.3V PCI clock outputs.
	FS1	IN	Logic input frequency select bit. Input latched at power on.
20, 19, 17, 16, 15	PCICLK [7:3]	OUT	3.3V PCI clock outputs.
13	PCICLK2	OUT	3.3V PCI clock output.
	SEL24_48#	IN	Input logic select. When logic "0" is selected pin 35 = 48MHz When logic "1" is selected pin 35 = 24MHz.
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	SCLK	IN	Clock input of I^2C input.
24	SDATA	IN	Data input for I^2C serial input.
34	48MHz	OUT	3.3V Fixed 48MHz clock output for USB.
	FS3	IN	Logic input frequency select bit. Input latched at power on.
35	FS2	IN	Logic input frequency select bit. Input latched at power on.
	24_48MHz	OUT	3.3V 24 or 48MHz output.
38	SDRAM_F	OUT	3.3V free running 100MHz SDRAM not affected by I^2C
48, 47, 44, 43, 42, 40, 39, 31, 30, 30, 27, 26	SDRAM [11:0]	OUT	3.3V output running 100MHz. All SDRAM outputs can be turned off through I^2C.
50	GNDL	PWR	Ground for 2.5V power supply for CPU & APIC.
51, 52	CPUCLK [1:0]	OUT	2.5V Host bus clock output. Output frequency derived from FS pins.
53, 55	VDDL	PWR	2.5V power suypply for CPU, IOAPIC.
54	IOAPIC	OUT	2.5V clock outputs running at 16.67MHz.
56	FS4	IN	Logic input frequency select bit. Input latched at power on.
	REF0	OUT	3.3V, 14.318MHz reference clock output.

Byte 0: Functionality and frequency select register (Default=0)
(1 = enable, 0 = disable)

Bit	Description											PWD
Bit (2, 7:4)	Bit 2	Bit 7	Bit 6	Bit 5	Bit 4	CPUCLK MHz	SDRAM MHz	3V66 MHz	PCICLK	IOAPIC MHz	Spread Precentage	00001 Note 1
	FS4	FS3	FS2	FS1	FS0							
	0	0	0	0	0	66.67	100.00	66.67	33.33	16.67	0 to -0.5% Down Spread	
	0	0	0	0	1	60.00	90.00	60.00	30.00	15.00	+/- 0.25% Center Spread	
	0	0	0	1	0	66.80	100.20	66.80	33.40	16.70	+/- 0.25% Center Spread	
	0	0	0	1	1	68.33	102.50	68.33	34.17	17.08	+/- 0.25% Center Spread	
	0	0	1	0	0	70.00	105.00	70.00	35.00	17.50	+/- 0.25% Center Spread	
	0	0	1	0	1	75.00	112.50	75.00	37.50	18.75	+/- 0.25% Center Spread	
	0	0	1	1	0	80.00	120.00	80.00	40.00	20.00	+/- 0.25% Center Spread	
	0	0	1	1	1	83.00	124.50	83.00	41.50	20.75	+/- 0.25% Center Spread	
	0	1	0	0	0	100.00	100.00	66.67	33.33	16.67	0 to -0.5% Down Spread	
	0	1	0	0	1	90.00	90.00	60.00	30.00	15.00	+/- 0.25% Center Spread	
	0	1	0	1	0	100.30	100.30	66.87	33.43	16.72	+/- 0.25% Center Spread	
	0	1	0	1	1	103.00	103.00	68.67	34.33	17.17	+/- 0.25% Center Spread	
	0	1	1	0	0	105.00	105.00	70.00	35.00	17.50	+/- 0.25% Center Spread	
	0	1	1	0	1	110.00	110.00	73.33	36.67	18.33	+/- 0.25% Center Spread	
	0	1	1	1	0	115.00	115.00	76.67	38.33	19.17	+/- 0.25% Center Spread	
	0	1	1	1	1	200.00	200.00	66.67	33.33	16.67	+/- 0.25% Center Spread	
	1	0	0	0	0	133.33	133.33	66.67	33.33	16.67	0 to -0.5% Down Spread	
	1	0	0	0	1	166.67	166.67	83.34	41.67	20.83	+/- 0.25% Center Spread	
	1	0	0	1	0	133.70	133.70	66.85	33.43	16.71	+/- 0.25% Center Spread	
	1	0	0	1	1	137.00	137.00	68.50	34.25	17.13	+/- 0.25% Center Spread	
	1	0	1	0	0	140.00	140.00	70.00	35.00	17.50	+/- 0.25% Center Spread	
	1	0	1	0	1	145.00	145.00	72.50	36.25	18.13	+/- 0.25% Center Spread	
	1	0	1	1	0	150.00	150.00	75.00	37.50	18.75	+/- 0.25% Center Spread	
	1	0	1	1	1	160.00	160.00	80.00	40.00	20.00	+/- 0.25% Center Spread	
	1	1	0	0	0	133.33	100.00	66.67	33.33	16.67	0 to -0.5% Down Spread	
	1	1	0	0	1	166.67	125.00	83.34	41.67	20.83	+/- 0.25% Center Spread	
	1	1	0	1	0	133.70	100.28	66.85	33.43	16.71	+/- 0.25% Center Spread	
	1	1	0	1	1	137.00	102.75	68.50	34.25	17.13	+/- 0.25% Center Spread	
	1	1	1	0	0	140.00	105.00	70.00	35.00	17.50	+/- 0.25% Center Spread	
	1	1	1	0	1	145.00	108.75	72.50	36.25	18.13	+/- 0.25% Center Spread	
	1	1	1	1	0	150.00	112.50	75.00	37.50	18.75	+/- 0.25% Center Spread	
	1	1	1	1	1	160.00	120.00	80.00	40.00	20.00	+/- 0.25% Center Spread	
Bit 3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,7:4											0
Bit 1	0- Normal 1- Spread spectrum enable											1
Bit 0	0- Running 1- Tristate all outputs											0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
2. The I^2C readback for Bit 2, 7:4 indicate the revision code.

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	FS3#
Bit 6	-	X	FS0#
Bit 5	-	X	FS2#
Bit 4	35	0	24_48MHz #
Bit 3	-	1	(Reserved)
Bit 2	34	1	48MHz
Bit 1	-	1	(Reserved)
Bit 0	38	1	SDRAM_F

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	39	1	SDRAM7
Bit 6	40	1	SDRAM6
Bit 5	42	1	SDRAM5
Bit 4	43	1	SDRAM4
Bit 3	44	1	SDRAM3
Bit 2	46	1	SDRAM2
Bit 1	47	1	SDRAM1
Bit 0	48	1	SDRAM0

Byte 3: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	20	1	PCICLK7
Bit 6	19	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 4: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	8	1	3V66_2
Bit 6	6	1	3V66_0
Bit 5	7	1	3V66_1
Bit 4	-	X	FS4#
Bit 3	54	1	IOAPIC
Bit 2	-	X	FS1#
Bit 1	51	1	CPUCLK1
Bit 0	52	1	CPUCLK0

Byte 5: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	26	1	SDRAM11
Bit 2	27	1	SDRAM10
Bit 1	30	1	SDRAM9
Bit 0	31	1	SDRAM8

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table[1]

Group	CPU 66MHz SDRAM 100MHz		CPU 100MHz SDRAM 100MHz		CPU 133MHz SDRAM 100MHz		CPU 133MHz SDRAM 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps	3.75ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps	3.75ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5 -3.5ns	500ps
PCI to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A	Asynch	N/A

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND			600	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		1.6	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			175	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -5.5 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH@min}$ = 1.4 V, $V_{OH@MAX}$ = 2.5 V	-36		-21	mA
Output Low Current	I_{OL4B}	$V_{OL@MIN}$ = 1.0 V, $V_{OL@MAX=}$ 0.2	36		31	mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	nS
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	nS
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45		55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.25 V			500	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH@MIN}$= 2.0 V, $V_{OH@MAX}$=3.135 V	-54		-46	mA
Output Low Current	I_{OL3}	$V_{OL@MIN}$= 1.0 V, $V_{OL@MAX}$=0.4 V	54		53	mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		1.6	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45		55	%
Skew	T_{sk3}[1]	V_T = 1.5 V			250	ps
Jitter	$t_j$cyc-cyc	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 48M, REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = 1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = -1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH@MIN}$=1 V, $V_{OH@MAX}$= 3.135 V	-29		-23	mA
Output Low Current	I_{OL5}	$V_{OL@MIN}$=1.95 V, $V_{OL@MIN}$=0.4 V	29		27	mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	4	nS
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.7	4	nS
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Fixed Clocks			500	pS
	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Ref Clocks			1000	pS

[1]Guarenteed by design, not 100% tested in production.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9250-30 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

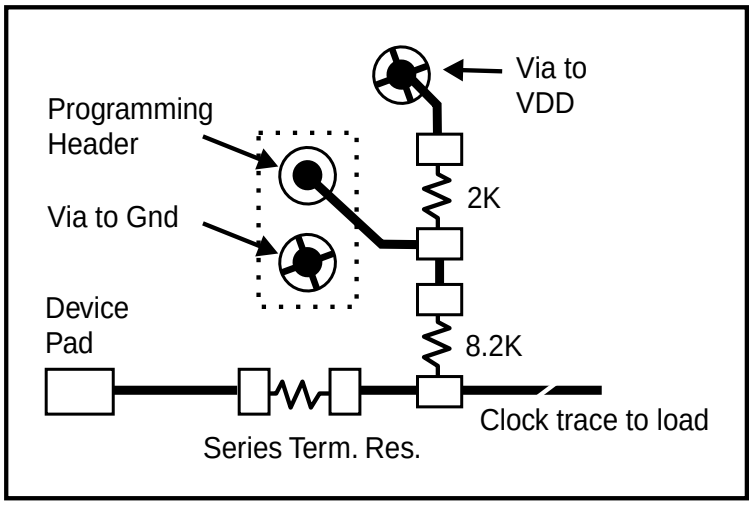
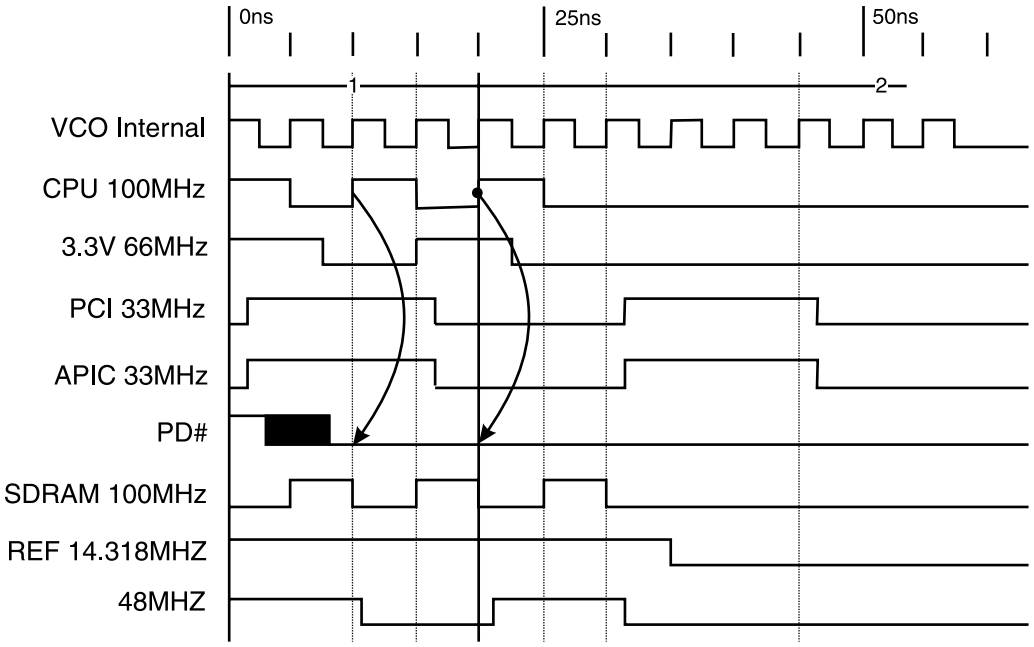


Fig. 1

Power Down Waveform

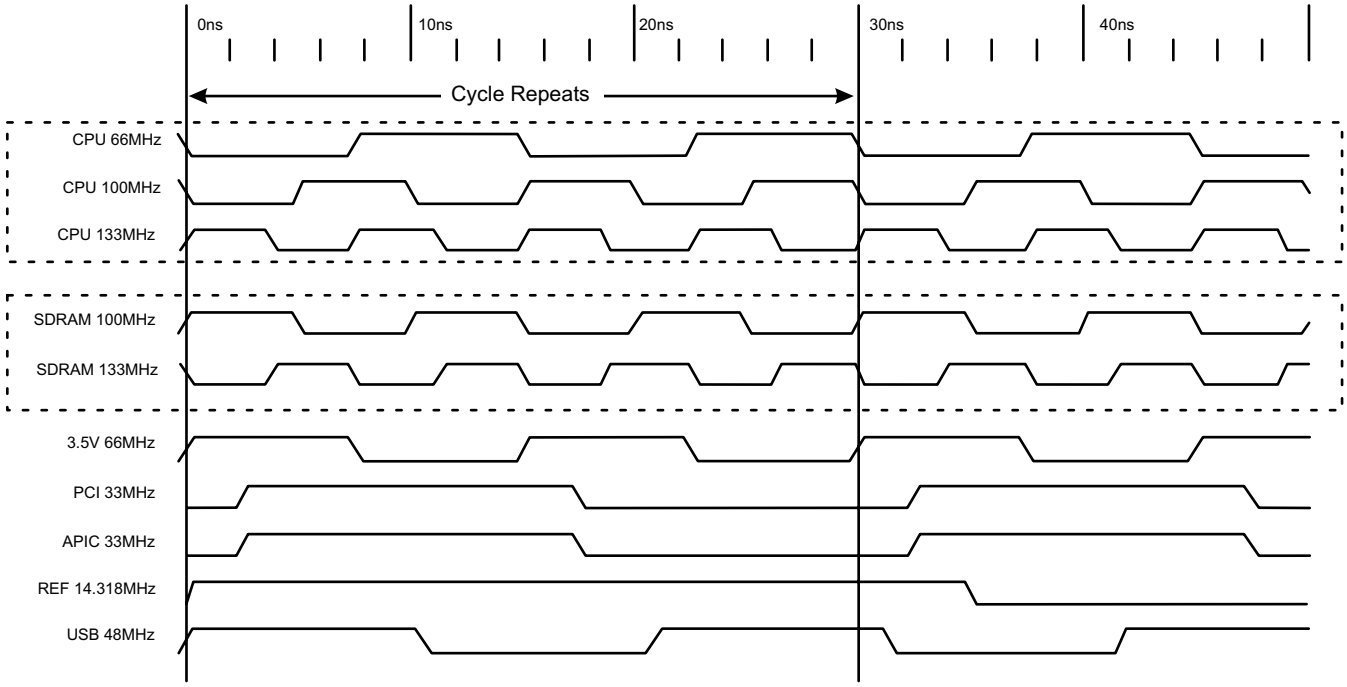


Note

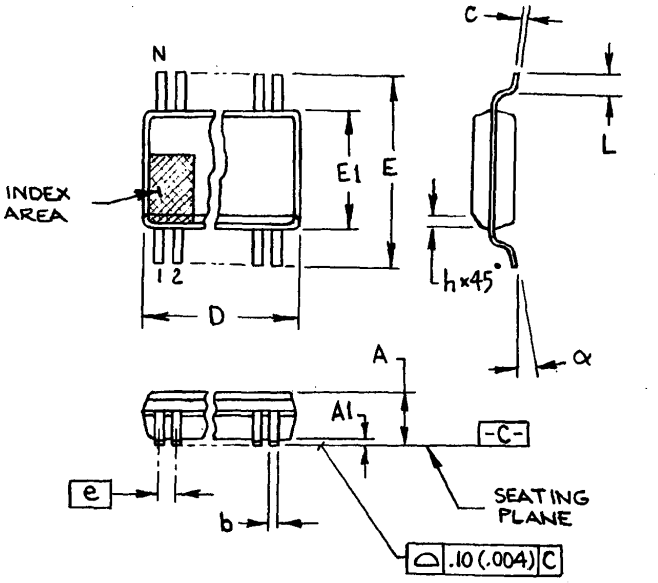
1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz



Group Offset Waveforms



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.288	18.542	.720	.730

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS9250yF-30-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device