Frequency Generator & Integrated Buffers for PENTIUM/Pro™

General Description

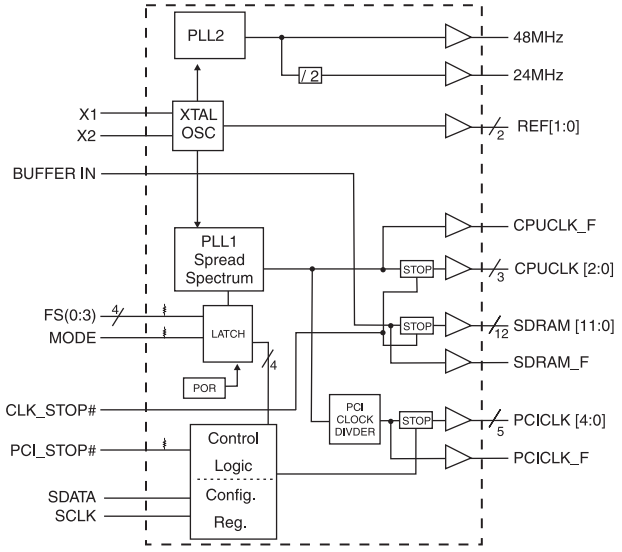
The **ICS9248-95** is the single chip clock solution for Desktop designs using the VIA MVP4 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-95** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

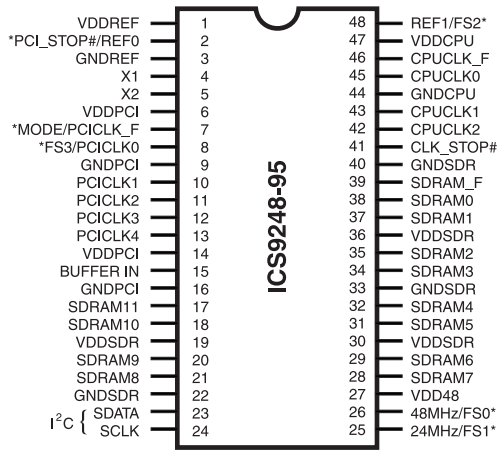
Features

- Up to 124MHz frequency support.
- Spread Spectrum for EMI control ±0.5% center spread and ±0.25% center spread
- Serial I²C interface for Power Management, Frequency Select, Spread Spectrum.
- Provides the following system clocks
  - 4-CPUs @ 3.3V, up to 124MHz.
  - 13-SDRAMs @3.3V, up to 124MHz (including SDRAM_F)
  - 6-PCI @3.3V, CPU/2 or CPU/3 (including PCICLK_F) (including 1 free running).
  - 1-24MHz @3.3V fixed.
  - 1-48MHz @3.3V fixed.
  - 2-REF @3.3V, 14.318MHz.
- Efficient Power management scheme through PCI and STOP CLOCKS.
- Spread Spectrum ±.25%, & ±.5% center spread

Block Diagram



Pin Configuration



48-Pin SSOP

* Internal Pull-up Resistor of 240K to VDD

Power Groups

VDDCPU, GNDCPU = CPUCLK [2:0], CPUCLK_F
VDDSDR, GNDSDR = SDRAMCLKS [11:0], SDRAM_F
VDDPCI, GNDPCI = PCICLKS [4:0], PCICLK_F
VDD48 = 48MHz, 24MHz
VDDREF, GNDREF = REF, X1, X2

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 Mhz reference clock.This REF output is the STRONGER buffer for ISA BUS loads
	PCI_STOP#[1]	IN	Halts PCICLK [4:1]clocks at logic 0 level, when input low (In mobile mode, MODE=0)
3,9,16,22, 33,40,44	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz.
6,14	VDDPCI	PWR	Supply for PCICLK_F and PCICLK [4:0], nominal 3.3V
7	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
	MODE[1, 2]	IN	Pin 17, pin 2 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
8	FS3[1]	IN	Frequency select pin. Latched Input.
	PCICLK0	OUT	PCI clock outputs. Syncheronous to CPU clocks with 1-4ns skew (CPU early)
13, 12, 11, 10	PCICLK [4:1]	OUT	PCI clock outputs. Syncheronous to CPU clocks with 1-4ns skew (CPU early)
15	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
17	SDRAM11	OUT	SDRAM clock output Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38	SDRAM [10:0]	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
19,30,36	VDDSDR	PWR	Supply for SDRAM [11:0] and CPU PLL Core, nominal 3.3V.
23	SDATA	IN	Data input for I^2C serial input, 5V tolerant input
24	SCLK	IN	Clock input of I^2C input, 5V tolerant input
25	24MHz	OUT	24MHz output clock
	FS1[1, 2]	IN	Frequency select pin. Latched Input.
26	48MHz	OUT	48MHz output clock
	FS0[1, 2]	IN	Frequency select pin. Latched Input
27	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
39	SDRAM_F	OUT	Free running SDRAM clock output. Not affected by CPU_STOP#
41	CLK_STOP#	IN	This asynchronous input halts CPUCLK & SDRAM (0:11) at logic "0" level when driven low.
42, 43, 45	CPUCLK [2:0]	OUT	CPU clock outputs, powered by VDDCPU
46	CPUCLK_F	OUT	Free running CPU clock. Not affected by the CPU_STOP#
47	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
48	REF1	OUT	14.318 MHz reference clock.
	FS2[1, 2]	IN	Frequency select pin. Latched Input

Notes:

1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

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Mode Pin - Power Management Input Control

MODE (Latched Input)	
0	PCI_STOP# (Input)
1	REF0 (Output)

Functionality

V_{DD}1,2,3 = 3.3V±5%, V_{DDL}1,2 = 2.5V±5% or 3.3±5%, TA=0 to 70°C
Crystal (X1, X2) = 14.31818MHz

FS3	FS2	FS1	FS0	CPU (MHz)	PCI (MHz)
0	0	0	0	124.00	41.33
0	0	0	1	120.00	40.00
0	0	1	0	114.99	38.33
0	0	1	1	109.99	36.66
0	1	0	0	105.00	35.00
0	1	0	1	83.31	41.65
0	1	1	0	80.00	40.00
0	1	1	1	75.00	37.50
1	0	0	0	100.00	33.33
1	0	0	1	95.19	31.73
1	0	1	0	83.31	27.77
1	0	1	1	80.00	26.67
1	1	0	0	90.00	30.00
1	1	0	1	70.00	35.00
1	1	1	0	66.82	33.41
1	1	1	1	60.00	30.00

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description			PWD
Bit 7	0 - ±0.25% Spread Spectrum Modulation 1 - ±0.5% Spread Spectrum Modulation			1
Bit [2, 6:4]	Bit [2, 6:4]	CPUCLK (MHz)	PCICLK (MHz)	Note1
	0000	124.00	41.33	
	0001	120.00	40.00	
	0010	114.99	38.33	
	0011	109.99	36.66	
	0100	105.00	35.00	
	0101	83.31	41.65	
	0110	80.00	40.00	
	0111	75.00	37.50	
	1000	100.00	33.33	
	1001	95.19	31.73	
	1010	83.31	27.77	
	1011	80.00	32.33	
	1100	90.00	30.00	
	1101	70.00	35.00	
	1110	66.82	33.41	
	1111	60.00	30.00	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit [2, 6:4]			0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled			1
Bit 0	0 - Running 1- Tristate all outputs			0

Note 1. Default at Power-up will be for latched logic inputs to define frequency. Bit [2, 6:4] are default to 0000.

Note: PWD = Power-Up Default

Byte 1: CPU, Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	X	Latched FS2#
Bit 6	46	1	CPUCLK_F (Act/Inact)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	39	1	SDRAM_F (Act/Inact)
Bit 2	42	1	CPUCLK2 (Act/Inact)
Bit 1	43	1	CPUCLK1 (Act/Inact)
Bit 0	45	1	CPUCLK0 (Act/Inact)

Byte 2: PCI Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	X	Latched FS0#
Bit 6	7	1	PCICLK_F (Act/Inact)
Bit 5	-	1	(Reserved)
Bit 4	13	1	PCICLK4 (Act/Inact)
Bit 3	12	1	PCICLK3 (Act/Inact)
Bit 2	11	1	PCICLK2 (Act/Inact)
Bit 1	10	1	PCICLK1 (Act/Inact)
Bit 0	8	1	PCICLK0 (Act/Inact)

Byte 3: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	17	1	SDRAM11 (Active/Inactive)
Bit 6	18	1	SDRAM10 (Active/Inactive)
Bit 5	20	1	SDRAM9 (Active/Inactive)
Bit 4	21	1	SDRAM8 (Active/Inactive)
Bit 3	28	1	SDRAM7 (Active/Inactive)
Bit 2	29	1	SDRAM6 (Active/Inactive)
Bit 1	31	1	SDRAM5 (Active/Inactive)
Bit 0	32	1	SDRAM4 (Active/Inactive)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 4: Reserved Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	X	Latched FS1#
Bit 2	-	1	(Reserved)
Bit 1	-	X	Latched FS3#
Bit 0	-	1	(Reserved)

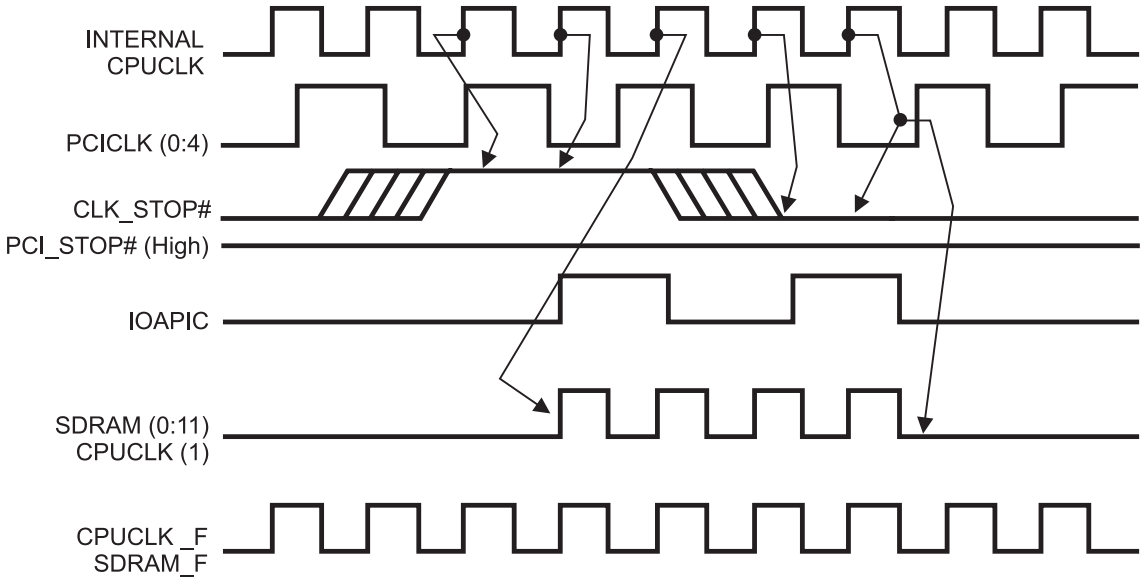
Byte 5: Peripheral Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	34	1	SDRAM3 (Act/Inact)
Bit 6	35	1	SDRAM2 (Act/Inact)
Bit 5	37	1	SDRAM1 (Act/Inact)
Bit 4	38	1	SDRAM0 (Act/Inact)
Bit 3	26	1	48MHz (Act/Inact)
Bit 2	25	1	24MHz (Act/Inact)
Bit 1	48	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

CLK_STOP# Timing Diagram

CLK_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the **ICS9248-95**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

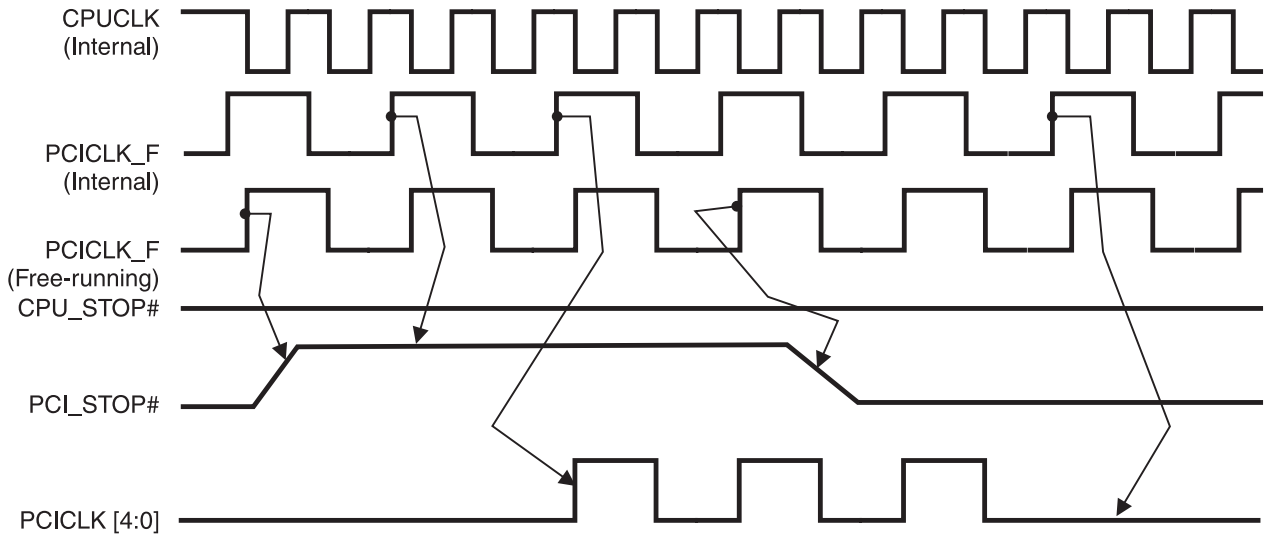


Notes:

1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-95.
3. IOAPIC output is Stopped Glitch Free by CPUSTOP# going low.
4. SDRAM-F output is controlled by Buffer in signal, not affected by the **ICS9248-95** CLK_STOP# signal. SDRAM (0:11) are controlled as shown.
5. All other clocks continue to run undisturbed.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-95**. It is used to turn off the PCICLK [4:0] clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-95** internally. The minimum that the PCICLK [4:0] clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK [4:0] clocks. PCICLK [4:0] clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK [4:0] clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9248-95** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

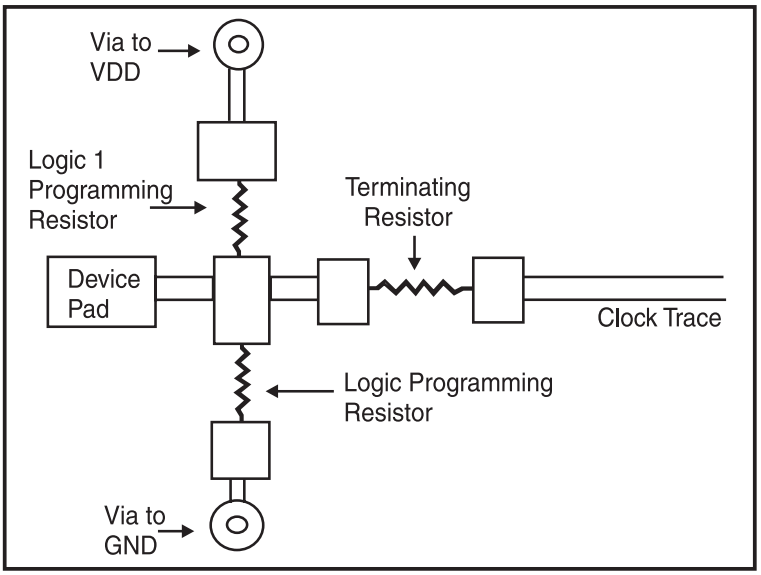


Fig. 1

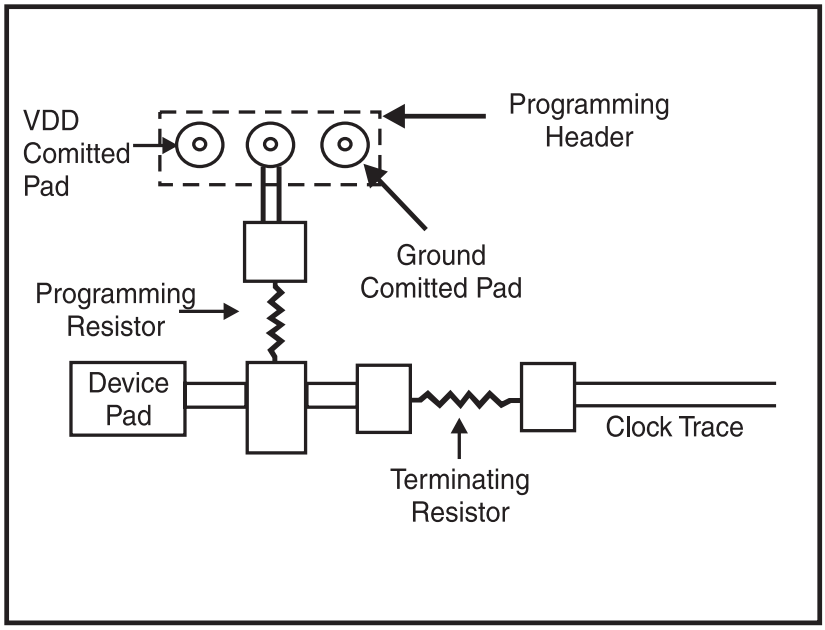


Fig. 2a

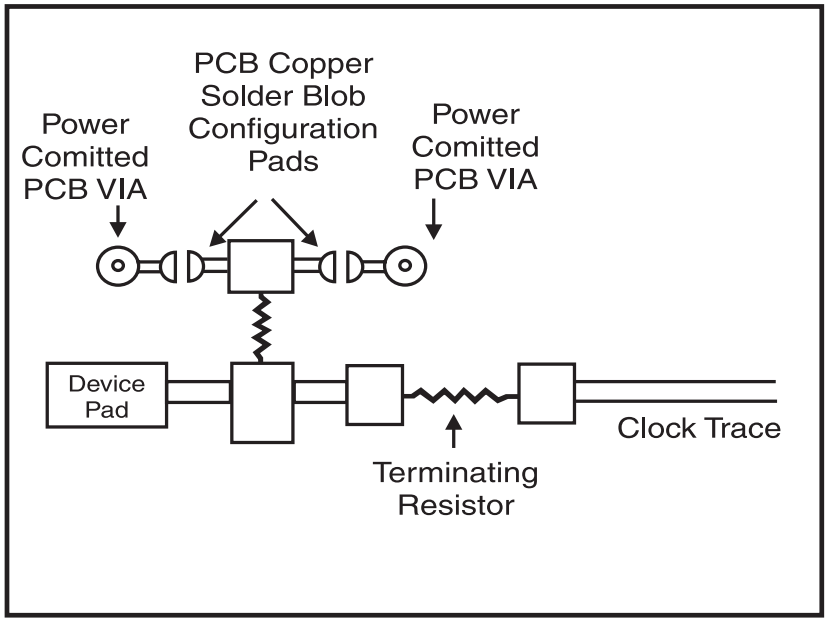


Fig. 2b

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Supply Current	I_{DD}	C_L = 0 pF; Select @ 66M		77	180	mA
	I_{DDL}			6.0	30	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pS
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.		1.5	3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Skew[1]	$T_{CPU-BUS}$	V_T = 1.5 V;	1.0	2.2	4.0	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$ Output P	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$ Output N	10		20	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.2	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-41	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	37		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		2.0	nS
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.0	2.0	nS
Duty Cycle	d_{t2A}[1]	V_T = 1.25 V	45.0	51.0	55.0	%
Skew (Window)	t_{sk2A}[1]	V_T = 1.25 V		120	250	pS
Jitter	t_{c-c}[1]	V_T = 1.25 V		250	300	pS
	t_{j1s}[1]	V_T = 1.25 V			150	pS
	t_{jabs}[1]	V_T = 1.25 V		208	250	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF 1

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 6.0 mA		0.25	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-42	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10	18		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4.0	nS
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4.0	nS
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45.0	50.0	55.0	%
Jitter	t_{j1s5}[1]	V_T = 1.5 V		100	250	pS
	t_{jabs5}[1]	V_T = 1.5 V		250	800	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	23	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	20	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4	2.9		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-58	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	52		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2.0	nS
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2.0	nS
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45.0	50.0	55.0	%
Skew Window	t_{sk1}[1]	V_T = 1.5 V		80	500	pS
Jitter	t_{j1s1}[1]	V_T = 1.5 V		50	150	pS
	t_{jabs1}[1]	V_T = 1.5 V		200	500	pS

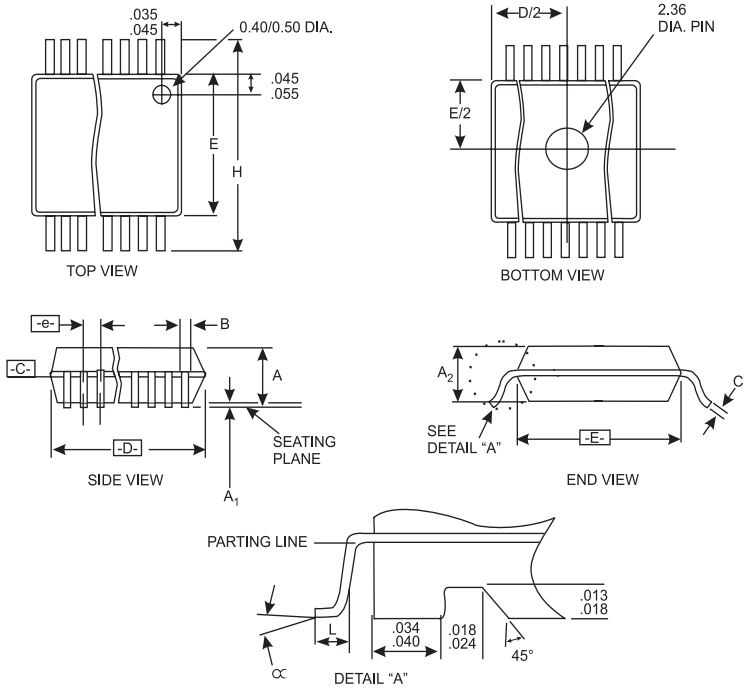
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} =V_{DDL} 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4	2.8		V
Output Low Voltage	V_{OL2A}	I_{OL} = 19 mA		0.3	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-72	-42	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33	50		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.0	nS
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	nS
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45	50	55	%
Skew Window (output to output)	t_{sk2A}[1]	V_T = 1.5 V		200	250	pS
Skew (Bufferin to output)	t_{sk2A}[1]	V_T = 1.5 V			5	nS

[1]Guarenteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

SSOP Package

Ordering Information

9248yF-95LF

Example:

XXXX y F - PPP LF

- **Annealed Lead Free (optional)**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator**
- **Device Type (consists of 3 or 4 digit numbers)**

310D—04/12/05

Revision History

Rev.	Issue Date	Description	Page #
C	4/4/2005	1. Updated CPU,PCI, and SDRAM Electrical Characteristics.	13-14
D	4/12/2005	1. Updated Electrical Characteristics for Input/Output Parameters, CPU and SDRAM. 2. Added Lead Free option. 3. Datasheet Release.	12-15

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