Integrated Circuit Systems, Inc.

ICS9248-65

Frequency Timing Generator for PENTIUM II™ Systems

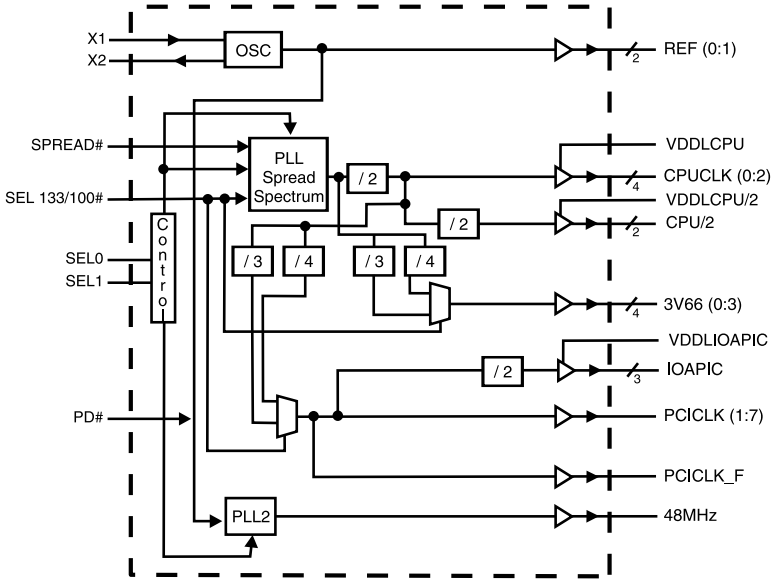
Features

- Generates the following system clocks:
  - 3 CPU clocks (2.5V, 100/133MHz)
  - 10 PCI clocks, including 1 free-running (3.3V, 33.3MHz)
  - 1 CPU/2 clocks (2.5V, 50/66.6MHz)
  - 1 IOAPIC clocks (2.5V, 16.67MHz)
  - 3 Fixed frequency 66MHz clocks(3.3V, 66.6MHz)
  - 2 REF clocks(3.3V, 14.318MHz)
  - 1 USB clock (3.3V, 48MHz)
- Efficient power management through PD#.
- 0 to -0.5% typical down spread modulation on CPU, PCI, IOAPIC, 3V66 and CPU/2 output clocks.
- Uses external 14.318MHz crystal.

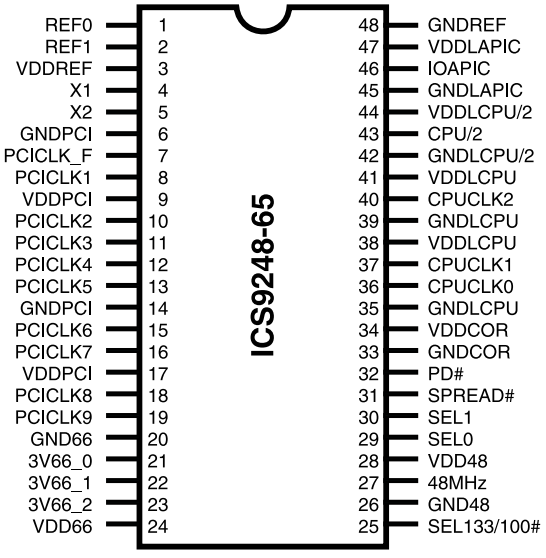
Key Specification

- CPU Output Jitter: <250ps
- CPU/2 Output Jitter. <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- PCI Output Jitter. <500ps
- Ref Output Jitter. <1000ps
- CPU 0:2 Output Skew: <175ps
- PCI_F, PCI 1:7 Output Skew: <500ps
- 3V66_0:2 Output Skew <250ps
- CPU to 3V66_0:2 Output Offset: 0.0 - 1.5ns (CPU leads)
- 3V66 to PCI Output Offset: 1.5 - 4ns (CPU leads)
- CPU to IOAPIC Output Offset 1.5 - 4.0ns (CPU leads)

Block Diagram



Pin Configuration



48-pin SSOP

General Description

The **ICS9248-65** is a main clock synthesizer chip for Pentium II based systems using Rambus Interface DRAMs. This chip provides all the clocks required for such a system when used with a Direct Rambus Clock Generator(DRCG) chip such as the ICS9211-01.

Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-65** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

The CPU/2 clocks are inputs to the DRCG.

Power Groups:

VDDREF, GNDREF = REF, X1, X2
GNDPCI, VDDPCI = PCICLK
VDD66, GND66 = 3V66
VDD48, GND48 = 48MHz
VDDCOR, GNDCOR = PLL Core
VDDLCPU/2 , GNDLCPU/2 = CPU/2
VDDLIOAPIC, GNDIOAPIC = IOAPIC

Pin Descriptions

Pin number	Pin name	Type	Description
1,2	REF	Output	3.3V, 14.318 MHz reference clock output.
3, 9, 17, 24, 28, 34	VDD	Power	3.3 V power for clock outputs.
4	X1	Input	14.318 MHz crystal input
5	X2	Output	14.318 MHz crystal output
6,14, 20, 26, 33, 45, 48	GND	Power	Ground for clock outputs
7	PCICLK_F	Output	3.3 V free running PCI clock output, will not be stopped by the PCI_STOP#
8,10,11,12,13, 15,16,18,19	PCICLK (1:9)	Output	3.3 V PCI clock outputs, generating timing requirements for
21,22,23	3V66	Output	3.3 V 66 MHz clock output, fixed frequency clock typically used with AGP
25	SEL 133/100#	Input	Control for the frequency of clocks at the CPU output pins. If logic "0" is used the 100 MHz frequency is selected. If Logic "1" is used, the 133 MHz frequency is selected. The PCI clock is multiplexed to run at 33.3 MHz for both selected cases.
27	48 MHz	Output	3.3 V 48 MHz clock output, fixed frequency clock typically used with USB devices
29,30	SEL (0:1)	Input	Frequency select pin , logic input.
31	SPREAD#	Output	Power-on spread spectrum enable option. Active low = spread spectrum clocking enable. Active high = spread spectrum clocking disable.
32	PD#	Input	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped.
35,39	GNDLCPU	Power	Ground for the CPU and Host clock outputs
36,37,40	CPUCLK (0:2)	0utput	2.5 V CPU and Host clock outputs
38,41	VDDLCPU	Power	2.5 V power for the CPU and Host clock outputs
42	GNDLCPU/2	Power	Ground for the CPU and Host clock outputs
43	CPU/2	Output	Output running at 1/2 CPU clock frequency.Synchronous to the CPU outputs.
44	VDDLCPU/2	Power	2.5 V power for the CPU/2 clock outputs
46	IOAPIC(0:1)	Output	2.5V fixed 16.6 MHz IOAPIC clock outputs
47	VDDIOAPIC	Power	2.5V power for IOAPIC clock

Frequency Select:

SEL 133/100#	SEL1	SEL0	CPU MHz	CPU/2 MHz	3V66 MHz	PCI MHz	48 MHz	REF MHz	IOAPIC MHz	Comments
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Tri-state
0	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
0	1	0	100	50	66.6	33.3	Hi-Z	14.318	16.67	48MHz PLL disabled
0	1	1	100	50	66.6	33.3	48	14.318	16.67	
1	0	0	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	Test mode (1)
1	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
1	1	0	133.3	66	66	33	Hi-Z	14.318	16.67	
1	1	1	133.3	66	66	33	48	14.318	16.67	

Note:
1. TCLK is a test clock driven on the x1 input during test mode.

ICS9248-65 Power Management Features:

PD#	CPUCLK	CPU/2	IOAPIC	3V66	PCI	PCI_F	REF. 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON	ON

Note:
1. LOW means outputs held static LOW as per latency requirement next page.
2. On means active.
3. PD# pulled Low, impacts all outputs including REF and 48 MHz outputs.

Power Management Requirements:

Singal	Singal State	Latency
		No. of rising edges of PCICLK
PD#	1 (normal operation)	3mS
	0 (power down)	2max.

Note:
1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/ high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high to when the first valid clocks are dirven from the device.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Offset

Group	Offset	Measurement Loads	Measure Points
CPU to 3V66	0.0-1.5ns CPU leads	CPU @ 20pF, 3V66 @ 30pF	CPU @1.25V, 3V66 @ 1.5V
3V66 to PCI	1.5-4.0ns 3V66 leads	3V66 @ 30pF, PCI @ 30pF	3V66 @ 1.5V, PCI @ 1.5V
CPU to IOAPIC	1.5-4.0ns CPU leads	CPU @ 20pF, IOAPIC @ 20pF	CPU @1.25V, IOAPIC @ 1.5V

Note: 1. All offsets are to be measured at rising edges.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = VDDL = 3.3 V +/-5%, (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100 MHz		65	160	mA
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133.3 MHz		71		
	$I_{DD3.3OP144}$	C_L = 0 pF; Select @ 144 MHz		75		
	$I_{DD3.3OP154}$	C_L = 0 pF; Select @ 154 MHz		78		
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; PWRDWN# = 0		64	200	µA
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.		1	3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		0.5		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{CPU-PCI}$	V_T = 1.5 V; V_{TL} = 1.25 V	1.5	2.4	4	ns
Skew[1]	$t_{CPU-3V66}$	V_T = 1.5 V; V_{TL} = 1.25 V		1.4	1.5	ns
Skew[1]	$t_{3V66-PCI}$	V_T = 1.5 V		1.4	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		14	30	mA
	$I_{DD2.5OP133}$	C_L = 0 pF; Select @ 133.3 MHz		18	30	
	$I_{DD2.5OP144}$	C_L = 0 pF; Select @ 144 MHz		19	30	
	$I_{DD2.5OP154}$	C_L = 0 pF; Select @ 154 MHz		20	30	
Power Down Supply Current	$I_{DD2.5PD}$	C_L = 0 pF; PWRDWN# = 0		0.3	100	µA
Skew[1]	$t_{CPU-PCI}$	V_T = 1.5 V; V_{TL} = 1.25 V	1.5	2.4	4	ns
Skew[1]	$t_{CPU-3V66}$	V_T = 1.5 V; V_{TL} = 1.25 V		1.4	1.5	ns
Skew[1]	$t_{CPU-IOAPIC}$	V_{TL} = 1.25 V		1.4	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-39	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	27		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		0.95	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V, Freq. < 124 MHz	45	50	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		22	175	ps
Jitter, One Sigma	$t_{j1\sigma 2B}$[1]	V_T = 1.25 V		21	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	55	+250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		110	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU/2

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.31	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-33	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	27		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.1	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V, Freq. < 124 MHz	45	48	55	%
Jitter, One Sigma	$t_{j1\sigma 2B}$[1]	V_T = 1.25 V		13	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	42	+250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		100	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-61	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	45		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.8	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.7	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		37	500	ps
Jitter, One Sigma[1]	$t_{j1\sigma 1}$	V_T = 1.5 V		16	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-250	50	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		130	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	45		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		310	500	ps
Jitter, One Sigma[1]	$t_{j1\sigma1}$	V_T = 1.5 V		11	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-250	45	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		105	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -12 mA	2	2.4		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA		0.17	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-61	-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	53		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		0.75	2.2	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		0.675	2	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45	49.5	55	%
Jitter, One Sigma[1]	$T_{j1\sigma4B}$	V_T = 1.25 V		26	150	ps
Jitter, Absolute[1]	T_{jabs4B}	V_T = 1.25 V	-500	137	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		200	500	ps

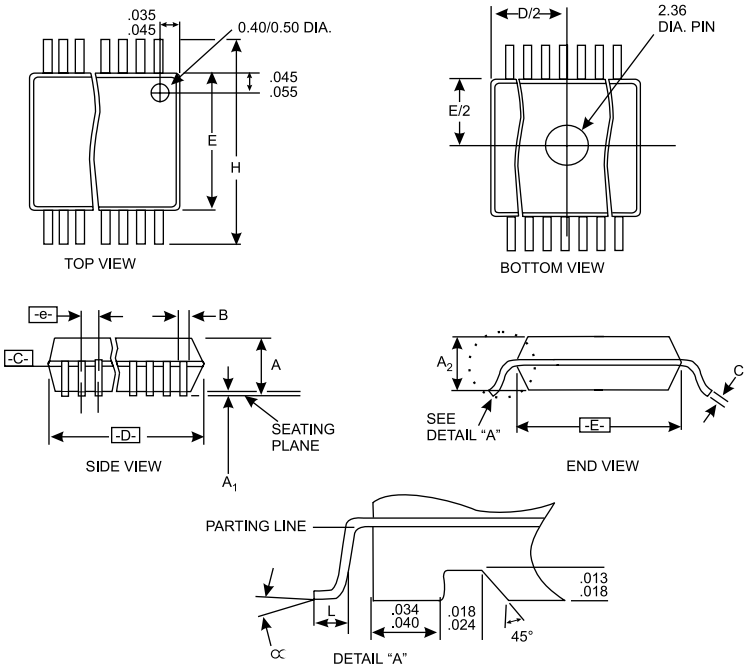
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 10 mA		0.33	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-31	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	23		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.1	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52	55	%
Jitter, One Sigma[1]	$t_{j1\sigma5}$	V_T = 1.5 V, REF		85	150	ps
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V, REF	-500	285	500	ps
Jitter, One Sigma[1]	$t_{j1\sigma5}$	V_T = 1.5 V, 48 MHz		32	150	ps
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V, 48 MHz	-250	110	250	ps

[1]Guaranteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

48 Pin SSOP Package

Ordering Information

ICS9248yF-65

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device