Integrated Circuit Systems, Inc.

ICS9248-64

AMD-K7™ System Clock Chip

General Description

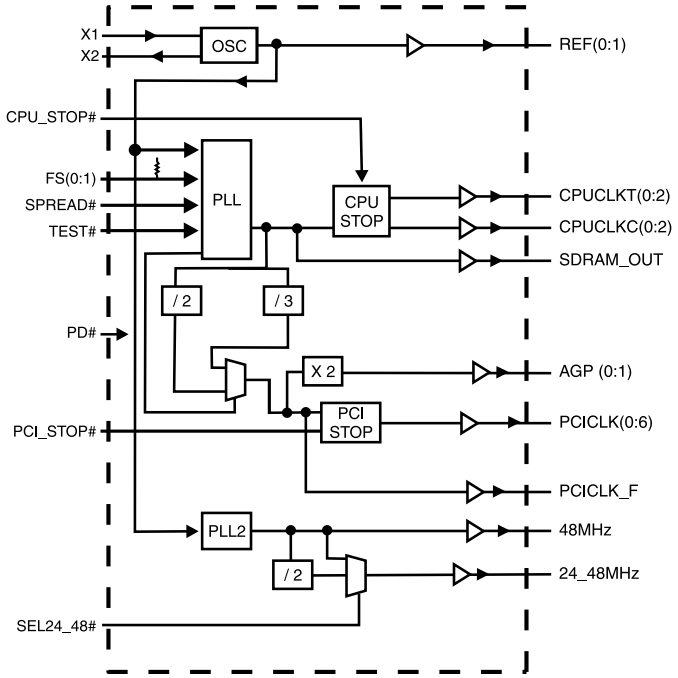
The **ICS9248-64** is a main clock synthesizer chip for AMD-K7 based systems. This provides all clocks required for such a system when used with a Zero Delay Buffer Chip such as the ICS9179-06.

Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-64** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

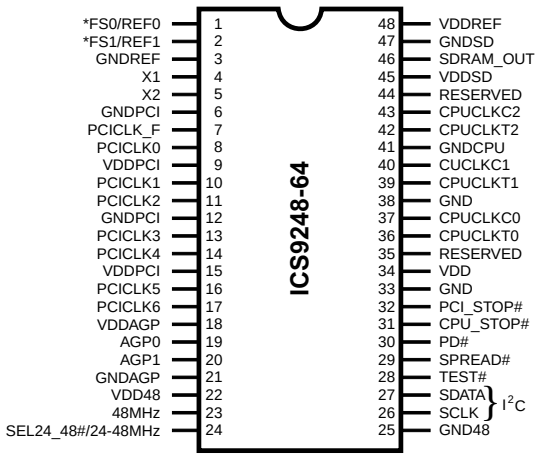
Features

- Generates the following system clocks:
  - 3 differential pair open drain CPU clocks (1.5V external pull-up; up to 133MHz).
  - 8 PCI including 1 free running (3.3V) @33.3MHz.
  - 2 AGP(3.3V) up to 66.6MHz.
  - 2 REF(3.3V)@14.318MHz
  - 1 48MHz(3.3V)
  - 24 / 48MHz(3.3V)
- Skew characteristics:
  - CPU -CPU≤250ps
  - CPUt - CPUc ≤200ps (differential pair)
  - PCI – PCI: <500ps
  - CPU – SDRAM_OUT: < 250ps
  - CPU – AGP <500ps
- Efficient Power Management through PD#, PCI_STOP# and CPU_STOP#.
- Spread Spectrum option for EMI reduction (-1.0% down spread).
- Uses external 14.318 MHz crystal

Block Diagram



Pin Configuration



48-Pin SSOP

* Internal 120K pullup resistor on indicated inputs

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 2	FS(0:1)	IN	Frequency Select pins, has pull-up to VDD
	REF(0:1)	OUT	14.318MHz clock output
3	GNDREF	PWR	Ground for REF outputs
4	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
5	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
6, 12	GNDPCI	PWR	Ground for PCI outputs
7	PCICLK_F	OUT	Free Running PCI output. Not affected by the PCI_STOP# input.
8, 10, 11, 13, 14,16,17	PCICLK (0:6)	OUT	PCI clock outputs. TTL compatible 3.3V
9, 15	VDDPCI	PWR	Power for PCICLK outputs, nominally 3.3V
18	VDDAGP	PWR	Power for AGP outputs, nominally 3.3V
19, 20	AGP (0:1)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
21	GNDAGP	PWR	Ground for AGP clock outputs
22	VDD48	PWR	Power for USB, FDC outputs nominally 3.3V
23	48MHz	OUT	48MHz output
24	SEL24-48#	IN	Selects 24 or 48MHz output for pin 24 Low = 48MHz High = 24MHz
	24-48MHz	OUT	Fixed clock out selectable through SEL24-48#
25	GND48	PWR	Ground for 48MHz outputs
26	SCLK	IN	Clock input for I^2C
27	SDATA	IN	Data input for I^2C
28	TEST#	IN	Tri State or test mode when low (please refer to frequency table)
29	SPREAD#	IN	Enables Spread Spectrum feature when LOW. Down Spread 0.5% modulation frequency =50KHz
30	PD#	IN	Powers down chip, active low. Internal PLL & all outputs are disabled.
31	CPU_STOP#	IN	Halts CPUCLKs. CPUCLKT(0:2) is driven LOW whereas CPUCLKC(0:2) is driven HIGH when this pin is asserted (Active LOW).
32	PCI_STOP#	IN	Halts PCI Bus at logic "0" level when driven low. PCICLK_F is not affected by this pin
33	GND	PWR	Isolated ground for core
34	VDD	PWR	Isolated power for core, nominally 3.3V
35, 44	RESERVED	N/C	Furture CPU power rail
36, 39, 42,	CPUCLKT (0:2)	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
37, 40, 43	CPUCLKC(0:2)	OUT	"Complementory" clocks of differental pair CPU output. These open drain outputs need an external 1.5V pull_up.
38, 41	GNDCPU	PWR	Ground for CPUCLK outputs.
45	VDDSD	PWR	Power for SDRAM_OUT pin. Norminally 3.3V
46	SDRAM_OUT	OUT	Reference clock for SDRAM zero delay buffer
47	GNDSD	PWR	Ground for SDRAM_OUT pins
48	VDDREF	PWR	Power for REF (0:1), X1, X2, nominally 3.3V

Frequency Select

TEST#	FS1	FS0	CPU, SDRAM	PCI	AGP	48MHz	REF	Comments
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Tri-state
0	0	1	50.0	25.0	50.0	48	14.318	
0	1	0	66.6	33.3	66.6	48	14.318	
0	1	1	TCLK/2	TCLK/6	TCLK/3	TCLK/4	TCLK	Test mode(1)
1	0	0	90.0	30.0	60.0	48	14.318	
1	0	1	133.3	33.3	66.6	48	14.318	
1	1	0	120.0	30.0	60.0	48	14.318	
1	1	1	100.0	33.3	66.6	48	14.318	

Notes:

1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.

I²C Command Bitmaps

Byte 0: Reserved for Buffer

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved for Buffer)
Bit 6	-	1	(Reserved for Buffer)
Bit 5	-	1	(Reserved for Buffer)
Bit 4	-	1	(Reserved for Buffer)
Bit 3	-	1	(Reserved for Buffer)
Bit 2	-	1	(Reserved for Buffer)
Bit 1	-	1	(Reserved for Buffer)
Bit 0	-	1	(Reserved for Buffer)

Byte 1: Reserved for Buffer

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved for Buffer)
Bit 6	-	1	(Reserved for Buffer)
Bit 5	-	1	(Reserved for Buffer)
Bit 4	-	1	(Reserved for Buffer)
Bit 3	-	1	(Reserved for Buffer)
Bit 2	-	1	(Reserved for Buffer)
Bit 1	-	1	(Reserved for Buffer)
Bit 0	-	1	(Reserved for Buffer)

Byte 2: Reserved for Buffer

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved for Buffer)
Bit 6	-	1	(Reserved for Buffer)
Bit 5	-	1	(Reserved for Buffer)
Bit 4	-	1	(Reserved for Buffer)
Bit 3	-	1	(Reserved for Buffer)
Bit 2	-	1	(Reserved for Buffer)
Bit 1	-	1	(Reserved for Buffer)
Bit 0	-	1	(Reserved for Buffer)

Byte 3: Reserved for Buffer

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved for Buffer)
Bit 6	-	1	(Reserved for Buffer)
Bit 5	-	1	(Reserved for Buffer)
Bit 4	-	1	(Reserved for Buffer)
Bit 3	-	1	(Reserved for Buffer)
Bit 2	-	1	(Reserved for Buffer)
Bit 1	-	1	(Reserved for Buffer)
Bit 0	-	1	(Reserved for Buffer)

Byte 4: Clock Control Register

BIT	PIN#	PWD	DESCRIPTION
7	1	1	REF0 enable
6	24	1	24MHz/48MHz enable
5	23	1	48MHz enable
4	20	1	AGP1 enable
3	19	1	AGP0 enable
2	42, 43	1	CPUCLK2 enable (both of differential pair, True" and "Complimentary"
1	39, 40	1	CPUCLK1 enable (both of differential pair, True" and "Complimentary"
0	36, 37	1	CPUCLK0 enable (both of differential pair, True" and "Complimentary"

Notes: A value of '1'b is enable, '0'b is disable

Byte 5: PCI Clock Control Register

BIT	PIN#	PWD	DESCRIPTION
7	2	1	REF1 enable
6	17	1	PCICLK6 enable
5	16	1	PCICLK5 enable
4	14	1	PCICLK4 enable
3	13	1	PCICLK3 enable
2	11	1	PCICLK2 enable
1	10	1	PCICLK1 enable
0	8	1	PCICLK0 enable

Notes: A value of '1'b is enable, '0'b is disable

Byte 6: SDRAM Clock & Generator Mode Control Register

Bit	Description				PWD
7	Spread Spectrum enable down spread				1
6:4	Bit 654	CPU	PCI	Spread Percentage	
	111	100	33.3	1% Down Spread	1
	110	120	30	1% Down Spread	
	101	133	33.3	1% Down Spread	
	100	90	30	-0.5%Down Spread	
	011	TCLK/2	TCLK/6	1% Down Spread	
	010	66	33	-0.5%Down Spread	
	001	50	25	1% Down Spread	
	000	HI-Z	HI-Z	1% Down Spread	
2:3	(Reserved)				1
1	I^2C enable				1
0	SDRAM_OUT Enable				1

Notes: A value of '1'b is enable, '0'b is disable

Absolute Maximum Ratings

Supply Voltage 5.5V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = max cap loads; Select @ 66MHz		100	180	mA
	$I_{DD3.3OP100}$	CL = max cap loads; Select @ 100MHz		110		
	$I_{DD3.3OP133}$	CL = max cap loads; Select @ 133MHz		120		
Power Down	PD			95	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew1	$t_{CPU-SDRAM}$	VT = 50%		190	250	ps
	$t_{CPU-AGP}$	VT = 50%		60	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24_48M, REF(0:1)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	2.8		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.32	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-27	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.3	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.4	4	ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45	51	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 Volts, REF		400	1000	ps
		V_T = 1.5 Volts, USB, 24_48M		260	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK (Open Drain)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$		50		Ω
Output High Voltage	V_{OH2B}	Termination to $V_{pull-up(external)}$	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to $V_{pull-up(external)}$		0.175	0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18	21		mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.3 V, V_{OH} = 1.2 V		0.85	0.9	ns
Differential voltage-AC[1]	V_{DIF}	Note 2	0.4		$V_{pullup(external)}$ + 0.6	V
Differential voltage-DC[1]	V_{DIF}	Note 2	0.2		$V_{pullup(external)}$ + 0.6	V
Differential Crossover Voltage[1]	V_X	Note 3	550	750	1100	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45	51	55	%
Skew[1], CPU to CPU	t_{sk2B}	V_T = 50%		100	250	ps
Skew[1], CPUT to CPUC	t_{sk2B}	V_T = 50%		135	200	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$		110	250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.

3 - $Vpullup_{(external)}$ = 1.5V, Min = $Vpullup_{(external)}$/2-150mV; Max=($Vpullup_{(external)}$/2)+150mV

Electrical Characteristics - PCICLK(0:6)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-54	-16	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	19	44		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.65	2	ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45	51	55	%
Skew[1](window)	T_{sk}[1]	V_T = 50%		470	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 Volts		120	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.165	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-54	-12	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12	44		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.75	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.65	2	ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45	51	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 Volts		120	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGP(0:1)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -18 mA	2	3		V
Output Low Voltage	V_{OL4B}	I_{OL} = 18 mA		0.31	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 2.0 V		-63	-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.8 V	19	30		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.3	2	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle[1]	D_{t4B}	V_T = 50%	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 Volts		290	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM_OUT

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -11 mA	2	3		V
Output Low Voltage	V_{OL3}	I_{OL} = 11 mA		0.31	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-60	-12	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	12	30		mA
Rise Time[1]	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.7	2.2	ns
Fall Time[1]	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.9	2.2	ns
Duty Cycle[1]	D_{t3}[1]	V_T = 50%	45	55	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 Volts		130	250	ps

[1]Guarenteed by design, not 100% tested in production.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-64 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

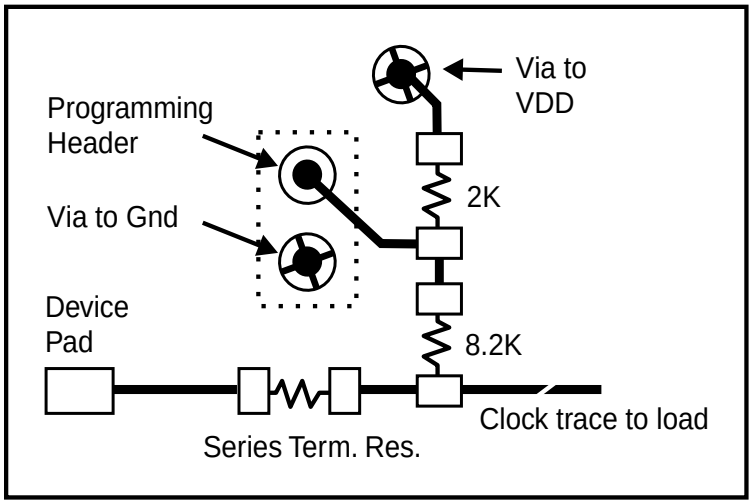
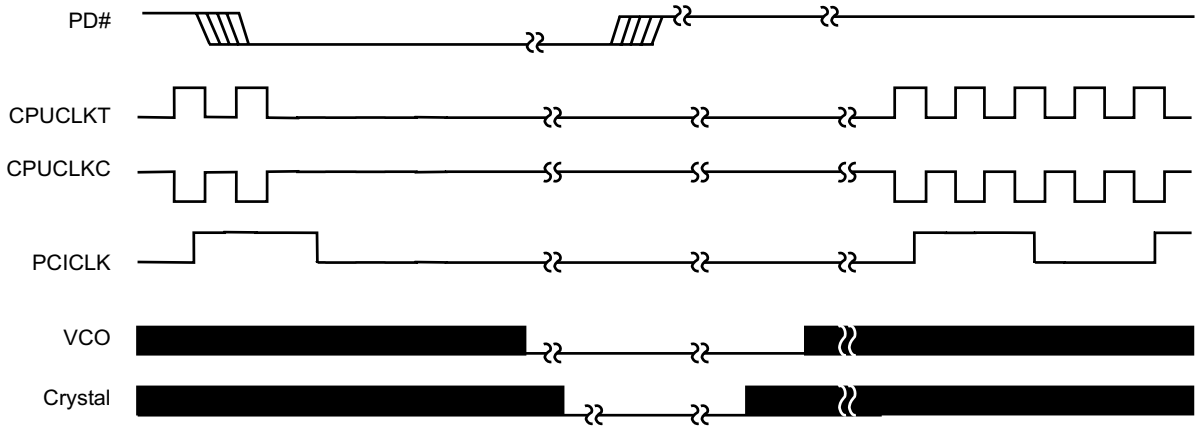


Fig. 1

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

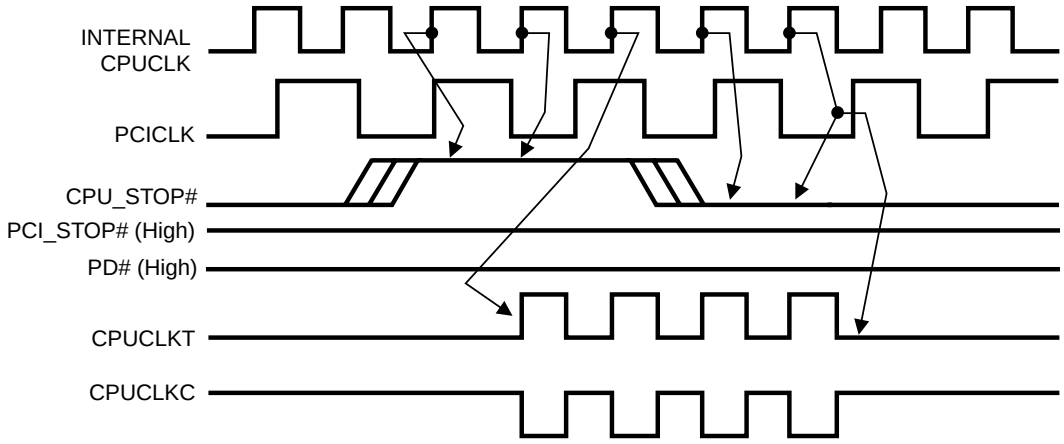
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-64 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

CPU_STOP# Timing Diagram

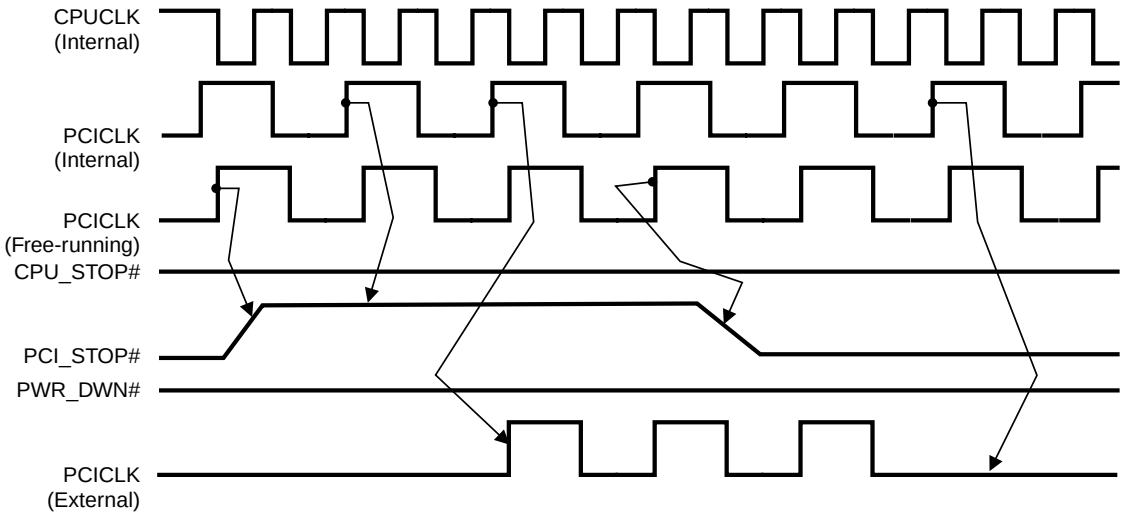
CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9248-64**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



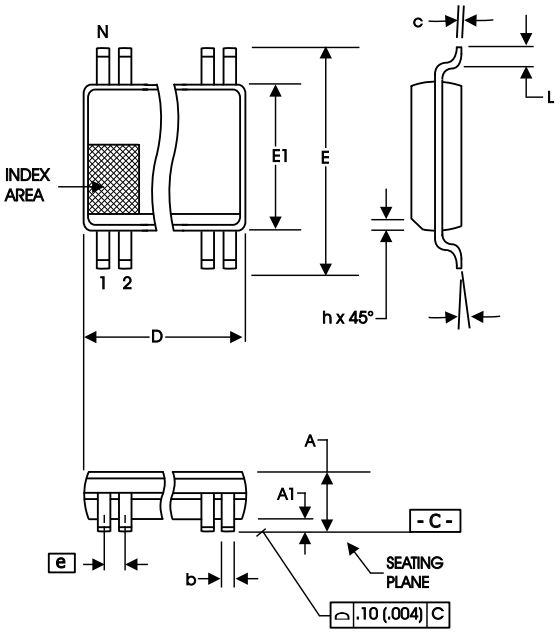
Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-64**.
3. All other clocks continue to run undisturbed including SDRAMR.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-64**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-64** internally. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9248yF-64

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS, AV = Standard Device