Integrated Circuit Systems, Inc.

ICS9248-163

Preliminary Product Preview

AMD - K7™ System Clock Chip

Recommended Application:
VIA KX133 style chipset

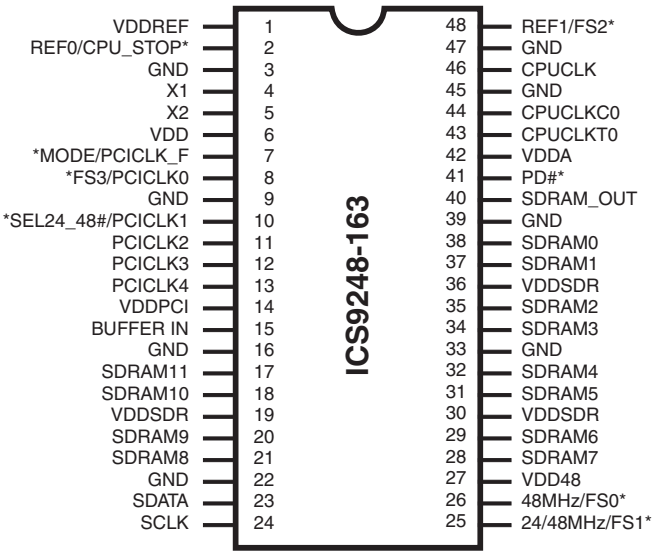
Output Features:

- 1 - Differential pair open drain CPU clocks
- 1 - CPU clock @ 3.3V
- 13 - SDRAM @ 3.3V
- 6 - PCI @3.3V,
- 1 - 48MHz, @3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

Features:

- Up to 166MHz frequency support
- Support power management: CPU stop and Power down Mode from I^2C programming.
- Spread spectrum for EMI control (± 0.25% center spread).
- Uses external 14.318MHz crystal

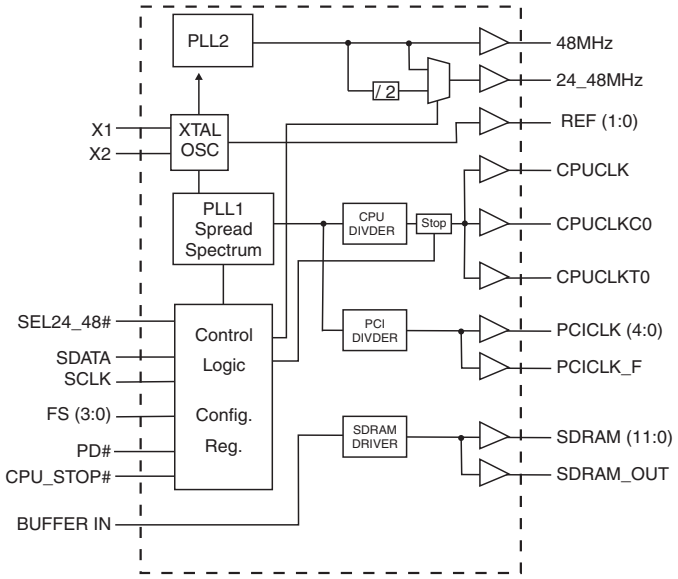
Pin Configuration



48-Pin 300mil SSOP

* Internal Pull-up Resistor of 120K to VDD

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	PCICLK (MHz)
0	0	0	0	90.00	30.00
0	0	0	1	95.00	31.67
0	0	1	0	101.00	33.67
0	0	1	1	102.00	34.00
0	1	0	0	100.90	33.57
0	1	0	1	103.00	34.33
0	1	1	0	105.00	35.00
0	1	1	1	100.00	33.33
1	0	0	0	107.00	35.67
1	0	0	1	109.00	36.33
1	0	1	0	110.00	36.67
1	0	1	1	111.00	37.00
1	1	0	0	113.00	37.67
1	1	0	1	115.00	38.33
1	1	1	0	117.00	39.00
1	1	1	1	133.30	33.33

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	REF, XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 Mhz reference clock.This REF output is the STRONGER buffer for ISA BUS loads
	CPU_STOP#[1, 2]	IN	This asynchronous input halts CPUCLKT, CPUCLKC & SDRAM (11:0) at logic "0" level when driven low.
3,9,16,22, 33,39,45, 47	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (36pF)
6	VDD	PWR	Supply for internal digital logic
7	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
	MODE[1, 2]	IN	Pin 17, pin 18 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
8	FS3[1, 2]	IN	Frequency select pin. Latched Input. Internal Pull-up to VDD
	PCICLK0	OUT	PCI clock output
10	SEL24_48#[1, 2]	IN	Logic input to select 24 or 48MHz for pin 25 output
	PCICLK1	OUT	PCI clock output.
13, 12, 11	PCICLK (4:2)	OUT	PCI clock outputs.
14	VDDPCI	PWR	Supply for PCICLK_F and PCICLK, nominal 3.3V
15	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
17, 18, 20, 21, 28, 29, 31, 32, 34, 35,37,38	SDRAM (11:0)	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
19,30,36	VDDSDR	PWR	Supply for SDRAM 9nominal 3.3V.
23	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
24	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
25	24_48MHz	OUT	24MHz/48MHz clock output
	FS1[1, 2]	IN	Frequency select pin. Latched Input.
26	48MHz	OUT	48MHz output clock
	FS0[1, 2]	IN	Frequency select pin. Latched Input
27	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
40	SDRAM_OUT	OUT	Reference clock for SDRAM buffer
41	PD#	IN	Powers down chip, active low
42	VDDA	PWR	Supply for core, & CPU 3.3V
43	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
44	CPUCLKC0	OUT	"Complementory" clock of differential pair CPU output. This open drain outputs needs an external 1.5V pull-up.
46	CPUCLK	OUT	3.3V CPU clock output powered by VDDA
48	REF1	OUT	14.318 MHz reference clock.
	FS2[1, 2]	IN	Frequency select pin. Latched Input

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General Description

The **ICS9248-163** is a main clock synthesizer chip for AMD-K7 based systems with VIA style chipset. This provides all clocks required for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-163 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Mode Pin - Power Management Input Control

MODE, Pin 7 (Latched Input)	Pin 2
0	CPU_STOP# (Input)
1	REF0 (Output)

Power Groups

VDD48 = 48MHz, PLL2
VDDA = VDD for Core PLL, CPU
VDDREF = REF, Xtal

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description								PWD
Bit 2, Bit 7:4	Bit 2	Bit 7	Bit 6	Bit 5	Bit 4	CPUCLK (MHz)	PCICLK (MHz)	Spread Precentage	Reserved
	0	0	0	0	0	90.00	30.00	±0.25% Center Spread	
	0	0	0	0	1	95.00	31.67	±0.25% Center Spread	
	0	0	0	1	0	101.00	33.67	±0.25% Center Spread	
	0	0	0	1	1	102.00	34.00	±0.25% Center Spread	
	0	0	1	0	0	100.90	33.57	±0.25% Center Spread	
	0	0	1	0	1	103.00	34.33	±0.25% Center Spread	
	0	0	1	1	0	105.00	35.00	±0.25% Center Spread	
	0	0	1	1	1	100.00	33.33	±0.25% Center Spread	
	0	1	0	0	0	107.00	35.67	±0.25% Center Spread	
	0	1	0	0	1	109.00	36.33	±0.25% Center Spread	
	0	1	0	1	0	110.00	36.67	±0.25% Center Spread	
	0	1	0	1	1	111.00	37.00	±0.25% Center Spread	
	0	1	1	0	0	113.00	37.67	±0.25% Center Spread	
	0	1	1	0	1	115.00	38.33	±0.25% Center Spread	
	0	1	1	1	0	117.00	39.00	±0.25% Center Spread	
	0	1	1	1	1	133.30	33.33	±0.25% Center Spread	
	1	0	0	0	0	120.00	40.00	±0.25% Center Spread	
	1	0	0	0	1	125.00	31.25	±0.25% Center Spread	
	1	0	0	1	0	130.00	32.50	±0.25% Center Spread	
	1	0	0	1	1	133.73	33.43	±0.25% Center Spread	
	1	0	1	0	0	135.00	33.75	±0.25% Center Spread	
	1	0	1	0	1	137.00	34.25	±0.25% Center Spread	
	1	0	1	1	0	139.00	34.75	±0.25% Center Spread	
	1	0	1	1	1	100.00	33.33	±0.25% Center Spread	
	1	1	0	0	0	140.00	35.00	±0.25% Center Spread	
	1	1	0	0	1	143.00	35.75	±0.25% Center Spread	
	1	1	0	1	0	145.00	36.25	±0.25% Center Spread	
	1	1	0	1	1	148.00	37.00	±0.25% Center Spread	
	1	1	1	0	0	150.00	37.50	±0.25% Center Spread	
	1	1	1	0	1	155.00	38.75	±0.25% Center Spread	
	1	1	1	1	0	166.66	41.67	±0.25% Center Spread	
	1	1	1	1	1	133.33	33.33	±0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4								0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled ±0.25% Center Spread								1
Bit 0	0 - Running 1- Tristate all outputs								0

Note: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS2#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	X	FS3#
Bit 3	40	1	SDRAM_OUT
Bit 2	-	X	(SEL24_48#)#
Bit 1	43,44	1	CPUCLK0 enable (both differential pair. "True" and Complimentary")
Bit 0	46	1	CPUCLKT enable

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS0#
Bit 6	7	1	PCICLK_F
Bit 5	-	1	(Reserved)
Bit 4	13	1	PCICLK4
Bit 3	12	1	PCICLK3
Bit 2	11	1	PCICLK2
Bit 1	10	1	PCICLK1
Bit 0	8	1	PCICLK0

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	26	1	48MHz
Bit 4	25	1	24_48MHz
Bit 3	17	1	SDRAM 11
Bit 2	18	1	SDRAM 10
Bit 1	20	1	SDRAM 9
Bit 0	21	1	SDRAM 8

Byte 4: SDRAM , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	28	1	SDRAM 7
Bit 6	29	1	SDRAM 6
Bit 5	31	1	SDRAM 5
Bit 4	32	1	SDRAM 4
Bit 3	34	1	SDRAM 3
Bit 2	35	1	SDRAM 2
Bit 1	37	1	SDRAM 1
Bit 0	38	1	SDRAM 0

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	X	MODE#
Bit 3	-	X	FS1#
Bit 2	-	1	(Reserved)
Bit 1	48	1	REF1
Bit 0	2	1	REF0

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Absolute Maximum Ratings

Supply Voltage 5.5V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			180	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz				
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133MHz				
Power Down	PD				600	µA
Input frequency	F_i	V_{DD} = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{CPU-SDRAM}$	V_T = 50%	-125		125	ps
	$t_{CPU-PCI}$		-100		100	
	$t_{CPU-AGP}$		-500		500	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - USB, REF

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK (Open Drain)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$				Ω
Output High Voltage	V_{OH2B}	Termination to $V_{pull\text{-}up(external)}$	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to $V_{pull\text{-}up(external)}$			0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.3 V, V_{OH} = 1.2 V			0.9	ns
Fall Time[1]	t_{f2B}	V_{OH} = 1.2 V, V_{OL} = 0.3 V			0.9	ns
Differential voltage-AC[1]	V_{DIF}	Note 2	0.4		$V_{pullup(external)}$ + 0.6	V
Differential voltage-DC[1]	V_{DIF}	Note 2	0.2		$V_{pullup(external)}$ + 0.6	V
Differential Crossover Voltage[1]	V_X	Note 3	550		1100	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45		55	%
Skew[1]	t_{sk2B}	VT = 50%			200	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc\text{-}cyc2B}$	$V_T = V_X$			250	ps
Jitter, Absolute[1]	t_{jabs2B}	VT = 50%	-250		+250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.

3 - $Vpullup_{(external)}$ = 1.5V, Min = $Vpullup_{(external)}$/2-150mV; Max=($Vpullup_{(external)}$/2)+150mV

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V			1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250		+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-16	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	19			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Skew[1] (window)	T_{sk}[1]	VT = 1.5V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Skew[1] (window)	T_{sk}[1]	VT = 1.5V			200	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V			0.5	ns
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-163 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

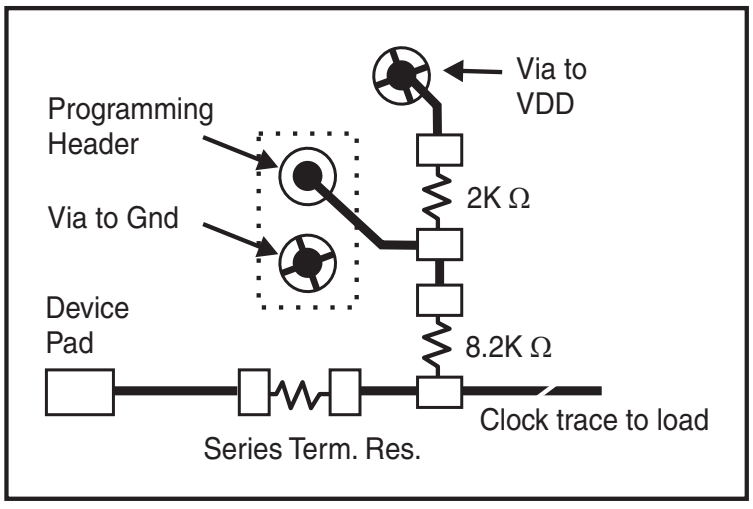
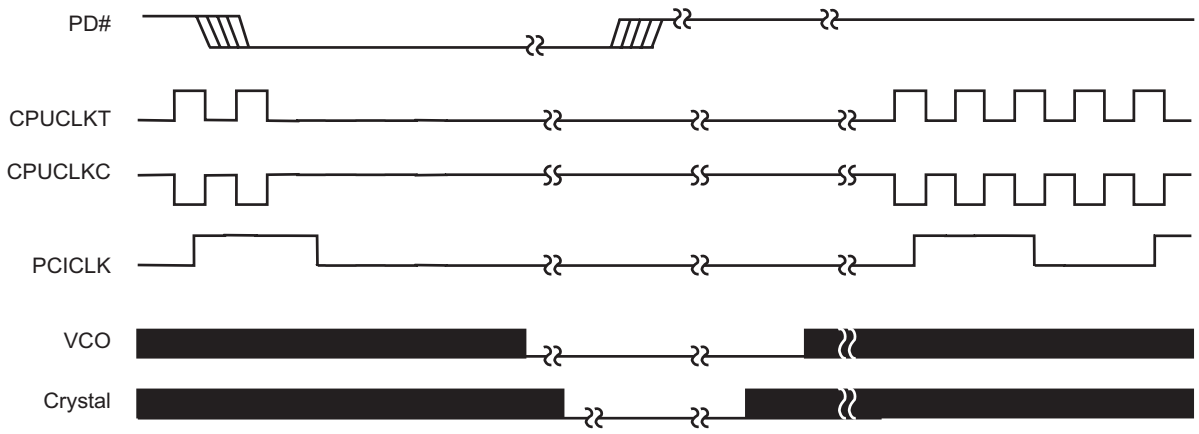


Fig. 1

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

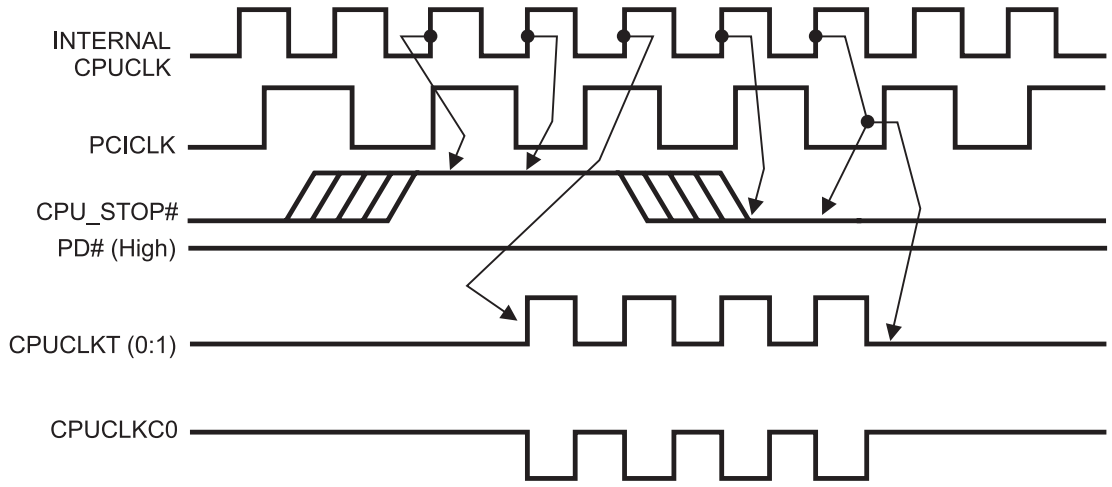
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. CPU_STOP# is considered to be a don't care during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-163 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

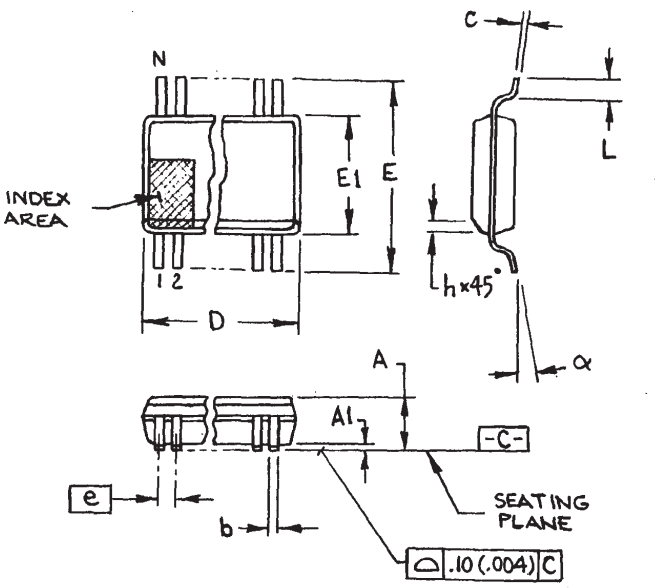
CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-163**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-163.
3. All other clocks continue to run undisturbed.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

Ordering Information

ICS9248yF-163-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device