Integrated Circuit Systems, Inc.

ICS9248-131

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

ALI - Aladdin V™ - mobile style chipsets

Output Features:

- 3 - CPUs @ 2.5/3.3V, up to 100MHz.
- 3 - AGPCLK @ 3.3V
- 13 - SDRAM @ 3.3V
- 6 - PCI @ 3.3V
- 1 - 48MHz, @ 3.3V fixed.
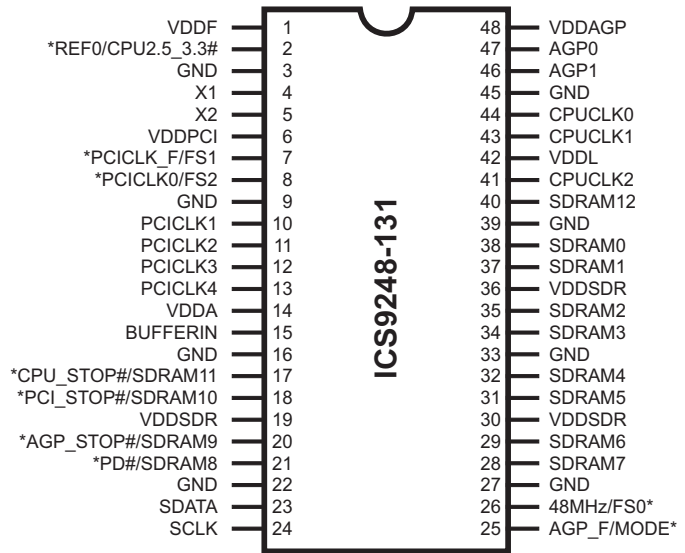- 1 - REF @ 3.3V, 14.318MHz.

Features:

- Support power management: CPU, PCI, AGP stop and Power down Mode from I^2C programming.
- Spread spectrum for EMI control.
- Uses external 14.318MHz crystal
- FS pins for frequency select

Key Specifications:

- CPU – CPU: <250ps
- AGP – PCI: <550ps
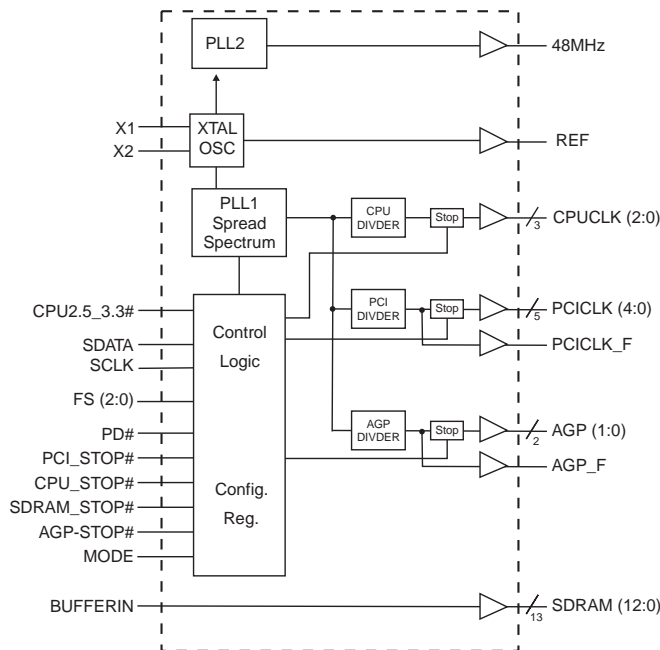- CPU(early)-PCI: 1-4ns, Center 2-6ns

Pin Configuration

VDDF	1	48	VDDAGP
*REF0/CPU2.5_3.3#	2	47	AGP0
GND	3	46	AGP1
X1	4	45	GND
X2	5	44	CPUCLK0
VDDPCI	6	43	CPUCLK1
*PCICLK_F/FS1	7	42	VDDL
*PCICLK0/FS2	8	41	CPUCLK2
GND	9	40	SDRAM12
PCICLK1	10	39	GND
PCICLK2	11	38	SDRAM0
PCICLK3	12	37	SDRAM1
PCICLK4	13	36	VDDSDR
VDDA	14	35	SDRAM2
BUFFERIN	15	34	SDRAM3
GND	16	33	GND
*CPU_STOP#/SDRAM11	17	32	SDRAM4
*PCI_STOP#/SDRAM10	18	31	SDRAM5
VDDSDR	19	30	VDDSDR
*AGP_STOP#/SDRAM9	20	29	SDRAM6
*PD#/SDRAM8	21	28	SDRAM7
GND	22	27	GND
SDATA	23	26	48MHz/FS0*
SCLK	24	25	AGP_F/MODE*

ICS9248-131

48-Pin SSOP

* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

Block Diagram

Functionality

FS2	FS1	FS0	CPU, SDRAM (MHz)	PCI (MHz)	AGP (MHz)
1	1	1	100	33.33	66.67
1	1	0	95.25	31.75	63.50
1	0	1	83.3	33.30	66.60
1	0	0	97	32.33	64.66
0	1	1	91.5	30.50	61.00
0	1	0	96.22	32.07	64.15
0	0	1	66.67	33.33	66.67
0	0	0	60	30.00	60.00

Note: REF & IOAPIC = 14.318MHz

Power Groups

Analog	Digital
VDDF	VDDPCI
VDDA	VDDSDR
	VDDAGP

ICS9248-131

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 6, 14, 19, 30, 36, 48	VDD	PWR	Power supply, nominal 3.3V
2	REF0	OUT	14.318 Mhz reference clock.
	CPU2.5_3.3#[1,2]	IN	Indicates whether VDDL is 3.3V or 2.5V. High=2.5V CPU, LOW=3.3V CPU[1]. Latched input[2]
3,9,16,22,27, 33,39,45	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
7	PCICLK_F	OUT	Free running PCI clock output. Synchronous with CPUCLKs with 1-4ns skew (CPU early) This is not affected by PCI_STOP#
	FS1[1, 2]	IN	Frequency select pin. Latched Input. Along with other FS pins determins the CPU, SDRAM, PCI & AGP frewuencies.
8	PCICLK0	OUT	PCI clock outputs. Synchrounous CPUCLKs with 1-4ns skew (CPU early)
	FS2[1, 2]	IN	Frequency select pin. Latched Input
13, 12, 11, 10	PCICLK(4:1)	OUT	PCI clock outputs. Synchrounous CPUCLKs with 1-4ns skew (CPU early)
15	BUFFERIN	IN	Input pin for SDRAM buffers.
17	CPU_STOP#[1]	IN	Halts CPUCLK clocks at logic 0 level, when input low (in Mobile Mode, MODE=0)
	SDRAM 11	OUT	SDRAM clock output
18	PCI_STOP#[1]	IN	Halts PCICLK clocks at logic 0 level, when input low (In mobile mode, MODE=0)
	SDRAM 10	OUT	SDRAM clock output
40, 28, 29, 31, 32, 34, 35, 37, 38	SDRAM (12, 7:0)	OUT	SDRAM clock outputs.
20	AGP_STOP#	IN	This asynchronous input halts AGP clocks at logic "0" level when input low (in Mobile Mode, MODE=0) Does not affect AGP0
	SDRAM9	OUT	SDRAM clock output
21	PD#	IN	This asyncheronous Power Down input Stops the VCO, crystal & internal clocks when active, Low. (In Mobile Mode, MODE=0)
	SDRAM8	OUT	SDRAM clock output
23	SDATA	I/O	Data pin for I²C circuitry 5V tolerant
24	SCLK	IN	Clock pin of I²C circuitry 5V tolerant
25	AGP_F	OUT	Advanced Graphic Port output, Not affected by AGP_STOP#
	MODE[1, 2]	IN	Pin 17, 18, 20 & 21 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
26	48MHz	OUT	48MHz output clock for USB timing.
	FS0[1, 2]	IN	Frequency select pin. Latched Input. Along with other FS pins determins the CPU, SDRAM, PCI & AGP frewuencies.
41, 43, 44	CPUCLK(2:0)	OUT	CPU clock outputs, powered by VDDL. Low if CPU_STOP#=Low
42	VDDL	PWR	Supply for CPU, either 2.5V or 3.3V nominal
46, 47	AGP (1:0)	OUT	Advanced Graphic Port outputs

Notes:

1:   Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

2:   Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General Description

The **ICS9248-131** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are externally selectable with smooth frequency transitions.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by **8dB** to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-131** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection. The SDRAM12 output may be used as a feed back into an off chip PLL.

Mode Pin - Power Management Input Control

MODE, Pin 25 (Latched Input)	Pin 17	Pin 18	Pin 20	Pin 21
0	CPU_STOP# (INPUT)	PCI_STOP# (INPUT)	AGP_STOP# (INPUT)	PD# (INPUT)
1	SDRAM 11 (OUTPUT)	SDRAM 10 (OUTPUT)	SDRAM 9 (OUTPUT)	SDRAM 8 (OUTPUT)

Power Management Functionality

AGP_STOP#	CPU_STOP#	PCI_STOP#	AGP, CPUCLK Outputs	PCICLK (4:0)	PCICLK_F, REF, 48MHz and SDRAM	Crystal OSC	VCO	AGP (1:0)
1	0	1	Stopped Low	Running	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running
1	1	0	Running	Stopped Low	Running	Running	Running	Running
0	1	1	Running	Running	Running	Running	Running	Stopped Low

CPU 3.3#_2.5V Buffer selector for CPUCLK drivers.

CPU3.3#_2.5 Input level (Latched Data)	Buffer Selected for operation at:
1	2.5V VDD
0	3.3V VDD

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description				PWD
Bit 7,2	Bit7 Bit2	Spread Spectrum Method			0,0
	0,0	+/- 0.25% Center Spread Spectrum Modulation			
	0,1	+/- 0.15% Center Spread Spectrum Modulation			
	1,0	0 to -0.5 Down Spread Spectrum Modulation			
	1,1	+/- 0.375% Center Spread Spectrum Modulation			
Bit 6:4	Bit6 Bit5 Bit4	CPU Clock	PCI	AGP	Note1 001
	111	100	33.33	66.67	
	110	95.25	31.75	63.50	
	101	83.3	33.30	66.60	
	100	97	32.33	64.66	
	011	91.5	30.50	61.00	
	010	96.22	32.07	64.15	
	001	66.67	33.33	66.67	
	000	60	30.00	60.00	
Bit 3	0 - Frequency is selected by hardware select, Latched inputs 1 - Frequency is selected by Bit 6:4 (above)				0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled				0
Bit 0	0 - Running 1 - Tristate all outputs				0

Note 1. Default at Power-up will be for latched logic inputs to define frequency. Bits 4, 5, 6 are default to 001, and if bit 3 is written to a 1 to use Bits 6:4, then these should be defined to desired frequency at same write cycle.

Note: PWD = Power-Up Default

Byte 1: CPU, Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	X	FS2#
Bit 5	-	X	FS1#
Bit 4	40	1	SDRAM12 (Act/Inact)
Bit 3	-	1	(Reserved)
Bit 2	41	1	CPUCLK2 (Act/Inact)
Bit 1	43	1	CPUCLK1 (Act/Inact)
Bit 0	44	1	CPUCLK0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	X	CPU2.5_3.3#
Bit 6	7	1	PCICLK_F (Act/Inact)
Bit 5	-	X	FS0#
Bit 4	13	1	PCICLK4 (Act/Inact)
Bit 3	12	1	PCICLK3 (Act/Inact)
Bit 2	11	1	PCICLK2 (Act/Inact)
Bit 1	10	1	PCICLK1 (Act/Inact)
Bit 0	8	1	PCICLK0(Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

I^2C is a trademark of Philips Corporation

Byte 3: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	28	1	SDRAM7 (Act/Inact)
Bit 6	29	1	SDRAM6 (Act/Inact)
Bit 5	31	1	SDRAM5 (Act/Inact)
Bit 4	32	1	SDRAM4 (Act/Inact)
Bit 3	34	1	SDRAM3 (Act/Inact)
Bit 2	35	1	SDRAM2 (Act/Inact)
Bit 1	37	1	SDRAM1 (Act/Inact)
Bit 0	38	1	SDRAM0 (Act/Inact)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 4: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	25	1	AGP_F (Active/Inactive)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	17	1	SDRAM11 (Act/Inact) (Desktop Mode Only)
Bit 2	18	1	SDRAM10 (Act/Inact) (Desktop Mode Only)
Bit 1	20	1	SDRAM9 (Act/Inact)
Bit 0	21	1	SDRAM8 (Act/Inact)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 5: Peripheral Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	47	1	AGP0 (Act/Inact)
Bit 3	-	1	(Reserved)
Bit 2	-	X	MODE
Bit 1	46	1	AGP1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 6: Optional Register for Possible
Furture Requirements

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	1	(Reserved)
Bit 0	-	1	(Reserved)

Notes:

1. Byte 6 is reserved by Integrated Circuit Systems for futue applications.

Absolute Maximum Ratings

Supply Voltage . . . . 5.5 V

Logic Inputs . . . . GND -0.5 V to $V_{DD} +0.5$ V

Ambient Operating Temperature . . . . 0°C to $+70$°C

Storage Temperature . . . . -65°C to $+150$°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} =V_{DDL}= 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	uA
Input Low Current	I_{IL1}	$V_{IN} = 0$ V; Inputs with no pull-up resistors	-5			uA
Input Low Current	I_{IL2}	$V_{IN} = 0$ V; Inputs with pull-up resistors	-200			uA
Operating Supply Current	$I_{DD3.3OP}$	$C_L = 0$ pF; Select @ 66 MHz		105	160	mA
		$C_L = 0$ pF; Select @ 100 MHz		140	160	mA
Input frequency	F_i	$V_{DD} = 3.3$ V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	Ttrans	To 1st crossing of target Freq			2	ms
Settling Time[1]	Ts	From 1st corssing to 1% target Freq			2	ms
Clk Stabilization[1]	T_{STAB}	From $V_{DD} = 3.3$ V to 1% target Freq.			2	ms
Skew[1]	$T_{CPU-PCI}$	Vt=1.5 V; f=66 / 100 Mhz; CPU leads	1	2	4	ns
	$T_{AGP-PCI}$	Vt = 1.5V; AGP Leads (Vdd+/-5% 25C)		300	550	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL}=2.5V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DDL2.5}$	$C_L = 0$ pF; Select @ 66.8 MHz		8	15	mA
		$C_L = 0$ pF; Select @ 100 MHz		15	20	
Skew[1]	$T_{CPU-PCI1}$	Vt=1.5 V; f=66 / 100 Mhz; CPU leads	1	2	4	ns
	$T_{AGP-PCI1}$	Vt = 1.5V; AGP Leads (Vdd+/-5% 25C)		300	550	ps

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD}=V_{DDL}=3.3V +/- 5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	V_O=V_{DD}*(0.5)	13.5	30	45	Ω
Output Impedance	R_{DSN2B}[1]	V_O=V_{DD}*(0.5)	13.5	32	45	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.5			V
Output Low Voltage	V_{OL2A}	I_{OL} = 27 mA			0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V			-23	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33			mA
Rise Time[1]	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.1	2	ns
Fall Time[1]	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle[1]	d_{t2A}[1]	V_T = 1.5 V	50	52	55	%
Skew window[1]	t_{sk2A}[1]	V_T = 1.5 V		130	250	ps
Jitter, Cycle-to-cycle1	tjcyc-cyc2A[1]	VT = 1.5 V		130	250	ps

[1]Guaranteed by design, not 100% tested in production.

[1]Edge displacement of a period relative to a 10-clock-cycle rolling average period.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD}=3.3V, V_{DDL}=2.5V, both +/- 5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	V_O=V_{DD}*(0.5)	13.5	30	45	Ω
Output Impedance	R_{DSN2B}[1]	V_O=V_{DD}*(0.5)	13.5	32	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -8 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time[1]	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1	1.8	ns
Fall Time[1]	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.3	1.8	ns
Duty Cycle[1]	d_{t2B}[1]	V_T = 1.25 V	45	50	55	%
Skew window[1]	t_{sk2B}[1]	V_T = 1.25 V		130	250	ps
Jitter, Cycle-to-cycle1	tjcyc-cyc2A[1]	VT = 1.5 V		130	250	ps

[1]Guaranteed by design, not 100% tested in production.

[1]Edge displacement of a period relative to a 10-clock-cycle rolling average period.

Electrical Characteristics - PCI

$T_A = 0 - 70C$; $V_{DD} = V_{DDL} = 3.3V$ +/-5%; $C_L = 30$ pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O=V_{DD}*(0.5)$	12	24	55	Ω
Output Impedance	R_{DSN2B}[1]	$V_O=V_{DD}*(0.5)$	12	23	55	Ω
Output High Voltage	V_{OH1}	$I_{OH} = -28$ mA	2.4			V
Output Low Voltage	V_{OL1}	$I_{OL} = 23$ mA			0.4	V
Output High Current	I_{OH1}	$V_{OH} = 2.0$ V			-40	mA
Output Low Current	I_{OL1}	$V_{OL} = 0.8$ V	41			mA
Rise Time[1]	t_{r1}	$V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V		1.7	2.3	ns
Fall Time[1]	t_{f1}	$V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V		1.5	2.0	ns
Duty Cycle[1]	d_{t1}	$V_T = 1.5$ V	45	50	55	%
Skew window[1]	t_{sk1}	$V_T = 1.5$ V		305	500	ps
Jitter, Cyc-to-Cyc	$t_{jcyc-cyc1}$	$V_T = 1.5$ V		100	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

$T_A = 0 - 70C$; $V_{DD}=V_{DDL}=3.3V$ +/-5%; $C_L = 30$ pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O=V_{DD}*(0.5)$	12	24.19	55	Ω
Output Impedance	R_{DSN2B}[1]	$V_O=V_{DD}*(0.5)$	12	23.08	55	Ω
Output High Voltage	V_{OH1}	$I_{OH} = -28$ mA	2.4			V
Output Low Voltage	V_{OL1}	$I_{OL} = 23$ mA			0.4	V
Output High Current	I_{OH1}	$V_{OH} = 2.0$ V			-40	mA
Output Low Current	I_{OL1}	$V_{OL} = 0.8$ V	41			mA
SD (0:1,3:12) Rise Time[1]	t_{r1}	$V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V		1.4	2	ns
SD(0:1,3:12) Fall Time[1]	t_{f1}	$V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V		1.5	2	ns
SD(0:1,3:12) Duty Cycle[1]	d_{t1}	$V_T = 1.5$ V	50	54	58	%
SD 2 Rise Time[1]	t_{r1}	$V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V		1.8	2.4	ns
SD 2 Fall Time[1]	t_{f1}	$V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V		1.9	2.4	ns
SD 2 Duty Cycle[1]	d_{t1}	$V_T = 1.5$ V	50	54	58	%
Propagation Delay	Tprop	$V_T = 1.5$ V		4	6	ns
Skew window[1]	t_{sk1}	$V_T = 1.5$ V		350	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGP

T_A = 0 - 70C; V_{DD}=V_{DDL}=3.3V +/-5%; C_L = 30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	V_O=V_{DD}*(0.5)	12	24.19	55	Ω
Output Impedance	R_{DSN2B}[1]	V_O=V_{DD}*(0.5)	12	23.08	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.3	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	48	55	%
Skew window1	tsk1	V_T = 1.5 V		100	250	ps
Jitter Cyc-Cyc, AGP(1:2)	tjcyc-cyc[1]	V_T = 1.5 V		120	250	ps
Jitter Cyc-Cyc, AGP_F	tjcyc-cyc[1]	V_T = 1.5 V		500	850	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3V +/-5%; C_L = 10 - 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	V_O=V_{DD}*(0.5)	20	47	60	Ω
Output Impedance	R_{DSN2B}[1]	V_O=V_{DD}*(0.5)	20	44	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -16 Ma	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.3	4.0	ns
Fall Time[1]	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.3	4.0	ns
Duty Cycle[1]	d_{t5}[1]	V_T = 1.5 V	45	50	55	%
REF Jitter, Cyl-to-Cyl	t_{j1s5}[1]	V_T = 1.5 V		0.7	1	ns

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.
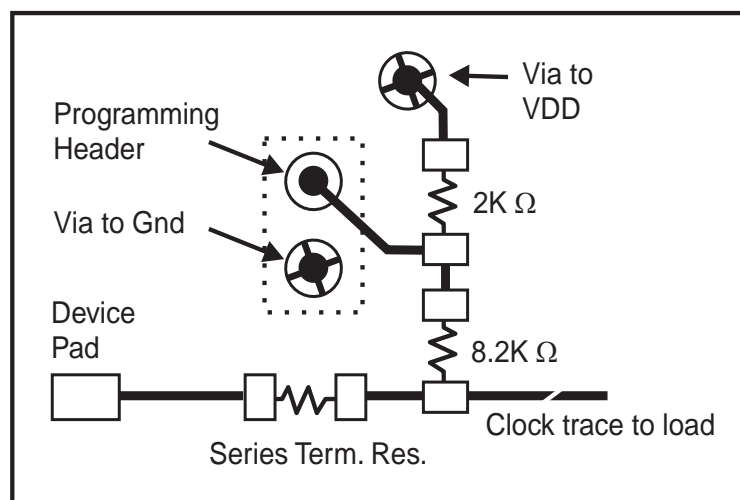
Fig. 1

General I^{2}C serial interface information

The information in this section assumes familiarity with I^{2}C programming.
For more information, contact ICS for an I^{2}C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2$_{(H)}$
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3$_{(H)}$
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte *(Byte 0) through byte 5*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2$_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

| How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3$_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^{2}C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^{2}C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

AGP_STOP# Timing Diagram

AGP_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the AGP clocks. for low power operation. AGP_STOP# is synchronized by the **ICS9248-131**. The AGPCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. AGPCLK on latency is less than AGPCLK and AGPCLK off latency is less than 4 AGPCLKs. This function is available only with MODE pin latched low.
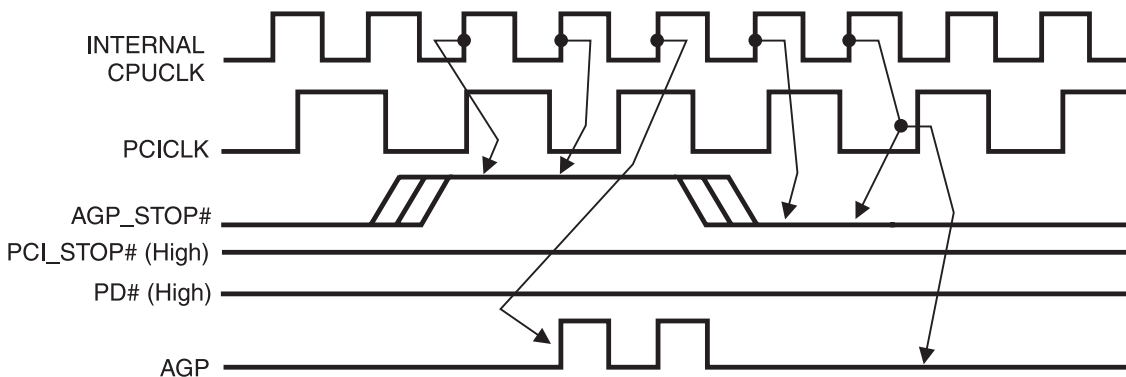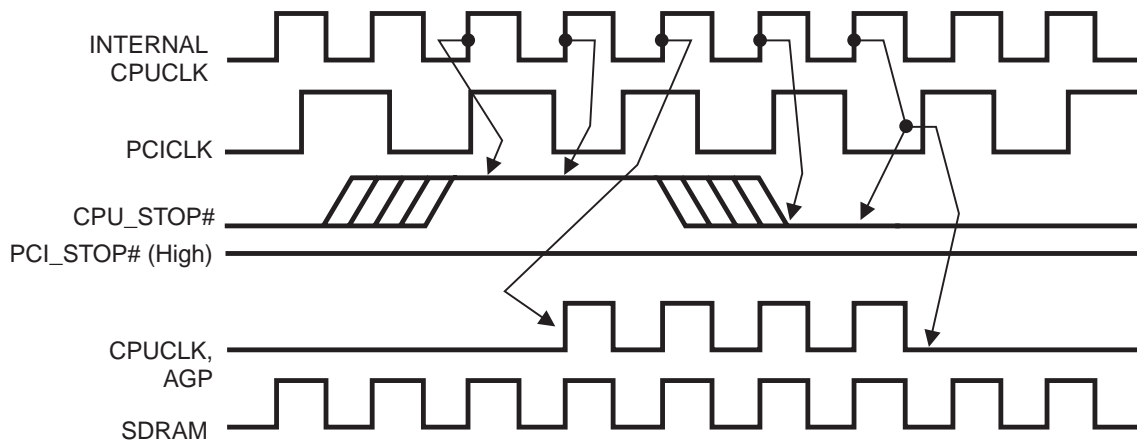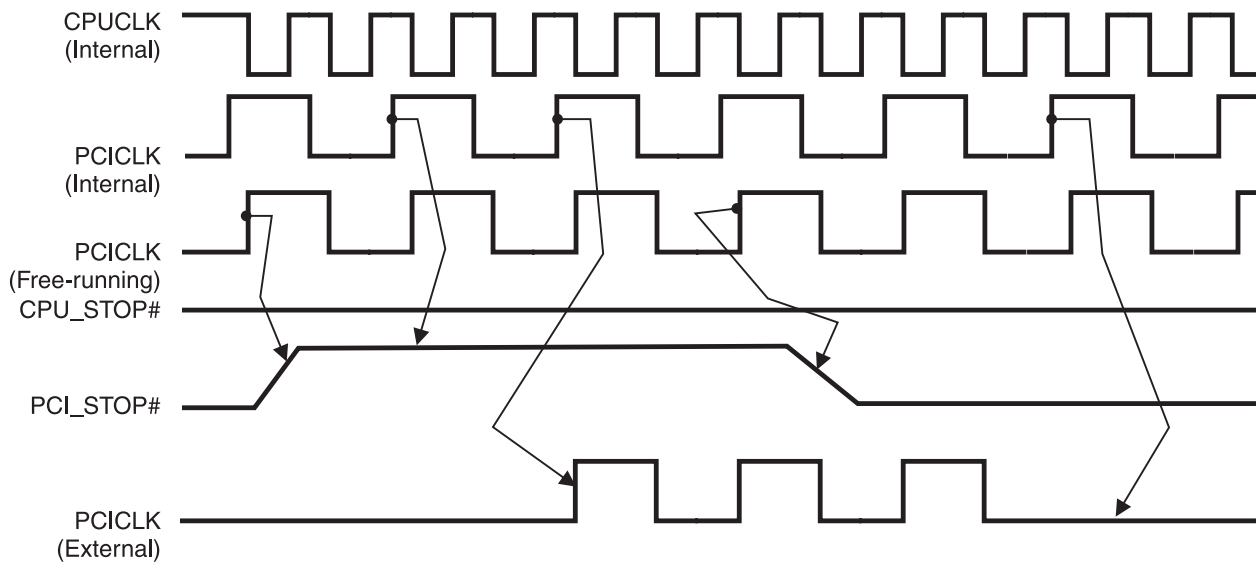

Notes:

1. All timing is referenced to the internal CPUCLK.

2. AGP_STOP# is an asychronous input and metastable conditions may exist.
   This signal is synchronized to the CPUCLKs inside the **ICS9248-131**.

3. All other clocks continue to run undisturbed.

4. PD# and PCI_STOP# are shown in a high (true) state.

5. Only applies if MODE pin latched 0 at power up.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-131**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

Notes:

1. All timing is referenced to the internal CPU clock.

2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-131.

3. All other clocks continue to run undisturbed. (including SDRAM outputs).

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-131**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-131** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.
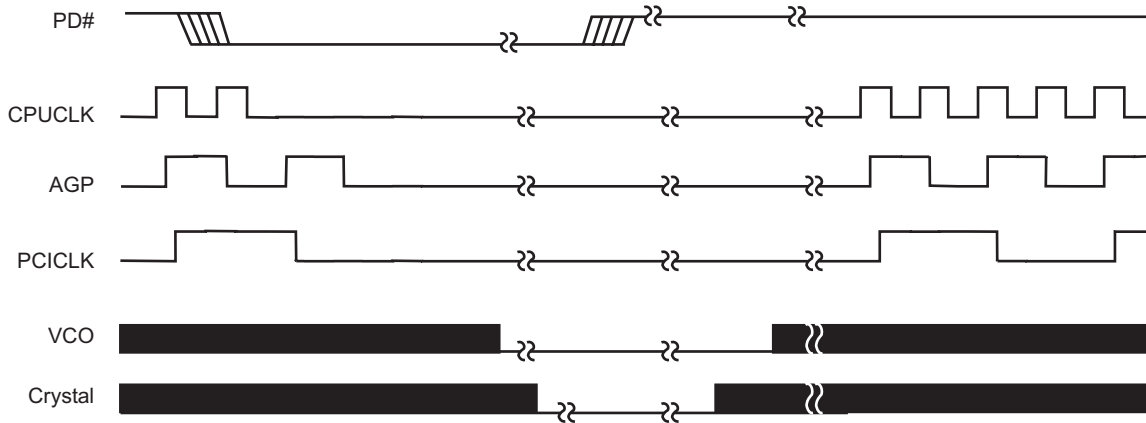

Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)

2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248 device.

3. All other clocks continue to run undisturbed.

4. CPU_STOP# is shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-131 device).

2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.

3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.

4. The shaded sections on the VCO and the Crystal signals indicate an active clock.

5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

300 mil SSOP
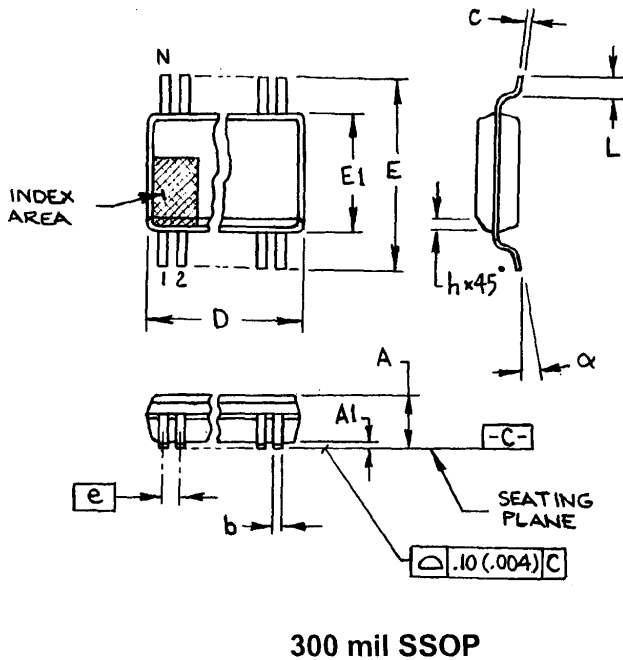
SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

JEDEC MO-118   6/1/00
DOC# 10-0034   REVB

Ordering Information

ICS9248yF-131-T

Example:

ICS XXXX y F - PPP - T

— **Designation for tape and reel packaging**

— **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**

— **Package Type**
F=SSOP

— **Revision Designator** (will not correlate with datasheet revision)

— **Device Type (consists of 3 or 4 digit numbers)**

— **Prefix**
ICS, AV = Standard Device

16