Integrated Circuit Systems, Inc.

ICS85320I
LVCMOS / LVTTL-TO-DIFFERENTIAL 2.5V / 3.3V LVPECL TRANSLATOR

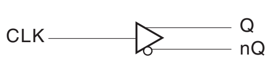
GENERAL DESCRIPTION

The ICS85320I is a LVCMOS / LVTTL-to-Differential 2.5V / 3.3V LVPECL translator and a member of the HiPerClocks™family of High Performance Clocks Solutions from ICS. The ICS85320I has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to 2.5V / 3.3V LVPECL levels. The small outline 8-pin SOIC package makes this device ideal for applications where space, high performance and low power are important.

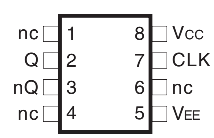
FEATURES

- 1 differential 2.5V/3.3V LVPECL output
- LVCMOS/LVTTL CLK input
- CLK accepts the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 267MHz
- Part-to-part skew: 275ps (maximum)
- Additive phase jitter, RMS: 0.05ps (typical)
- 3.3V operating supply voltage (operating range 3.135V to 3.465V)
- 2.5V operating supply voltage (operating range 2.375V to 2.625V)
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85320I

8-Lead SOIC
3.90mm x 4.92mm x 1.37mm body package
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 4, 6	nc	Unused		No connect.
2,3	Q, nQ	Output		Differential output pair. LVPECL interface levels.
5	V_{EE}	Power		Negative supply pin.
7	CLK	Input	Pullup	LVCMOS / LVTTL clock input.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				25	mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK		-0.3		1.3	V
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	$V_{CC} = V_{IN}$ = 3.465V	-150			µA

TABLE 3C. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK		1.6		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK		-0.3		0.9	V
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 2.625V			5	µA
I_{IL}	Input Low Current	CLK	$V_{CC} = V_{IN}$ = 2.625V	-150			µA

TABLE 3D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4A. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				267	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 267MHz	0.8		1.4	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	Integration Range: 12KHz - 20MHz		0.05		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				275	ps
t_R, t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%

NOTE 1: Measured from V_{CC}/2 point of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

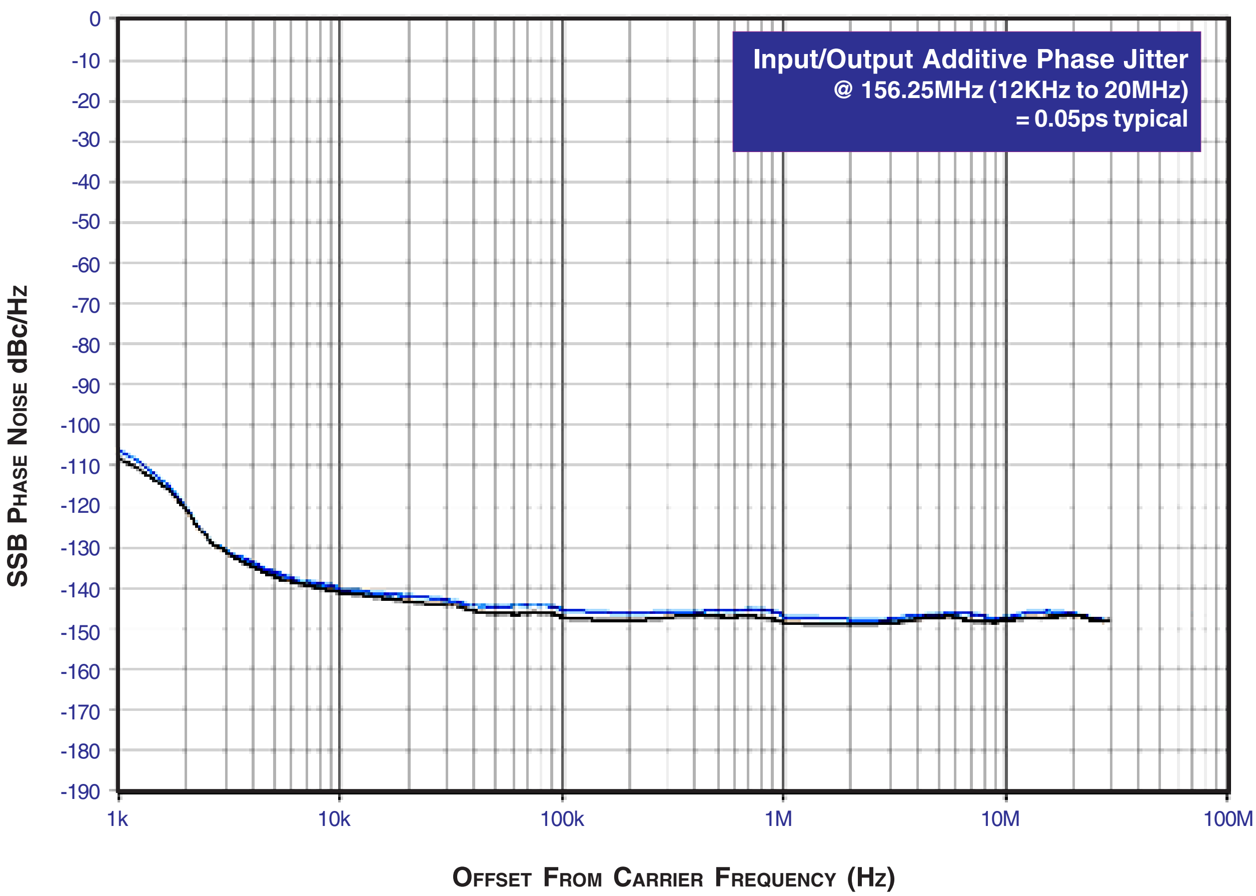
TABLE 4B. AC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				215	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 267MHz	0.8		1.7	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	Integration Range: 12KHz - 20MHz		0.05		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				375	ps
t_R, t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%

NOTE 1: Measured from V_{CC}/2 point of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

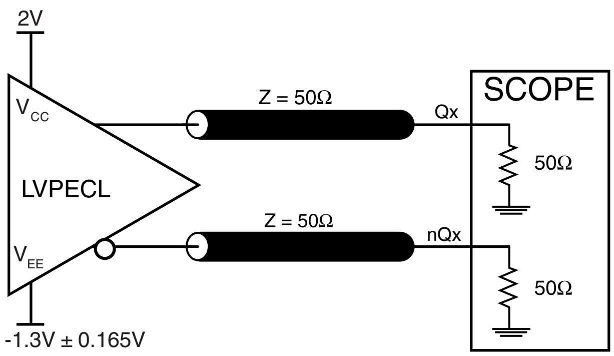
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

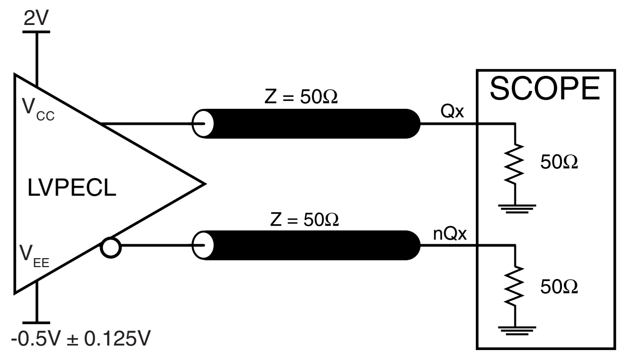


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

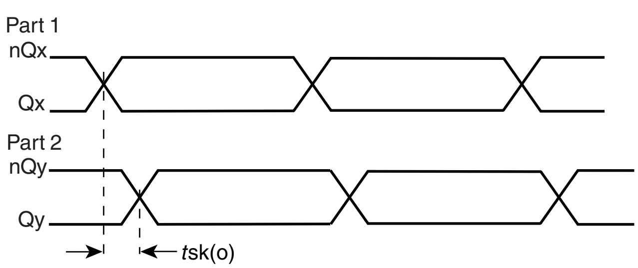
PARAMETER MEASUREMENT INFORMATION



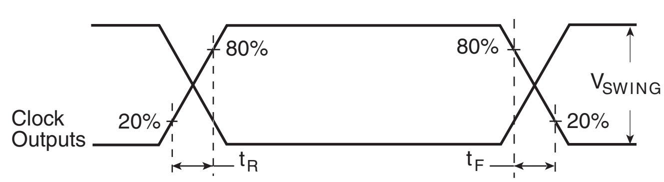
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



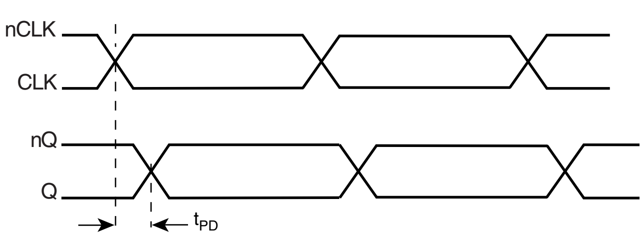
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



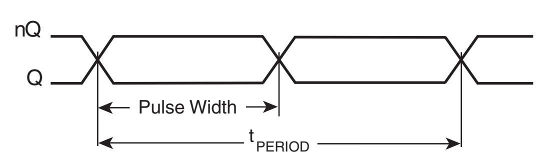
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

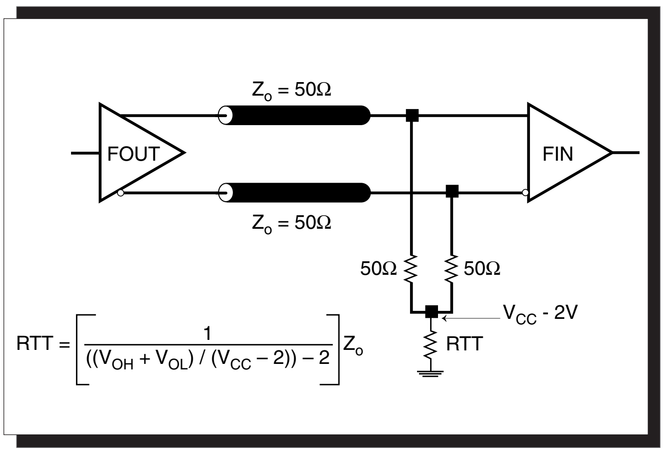


FIGURE 1A. LVPECL OUTPUT TERMINATION

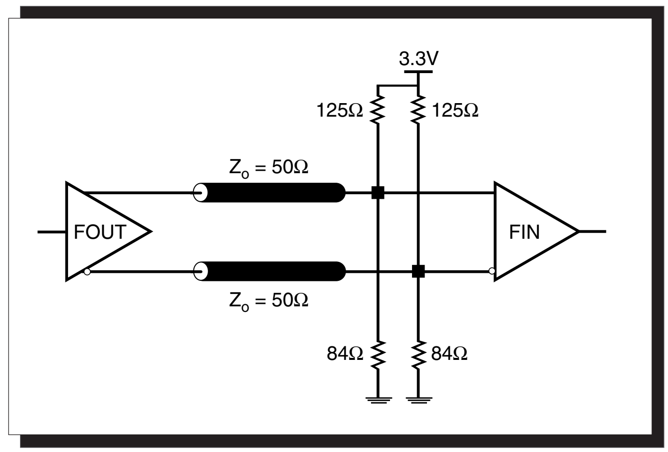


FIGURE 1B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 2A and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 2B can be eliminated and the termination is shown in *Figure 2C.*

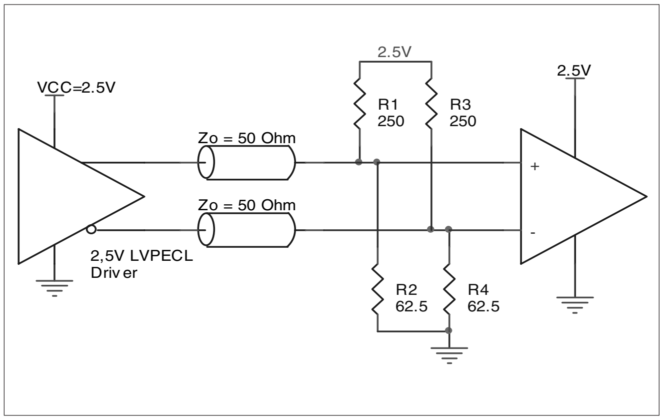


FIGURE 2A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

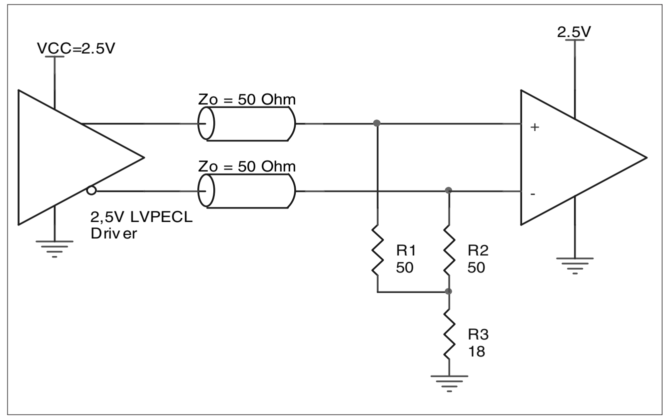


FIGURE 2B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

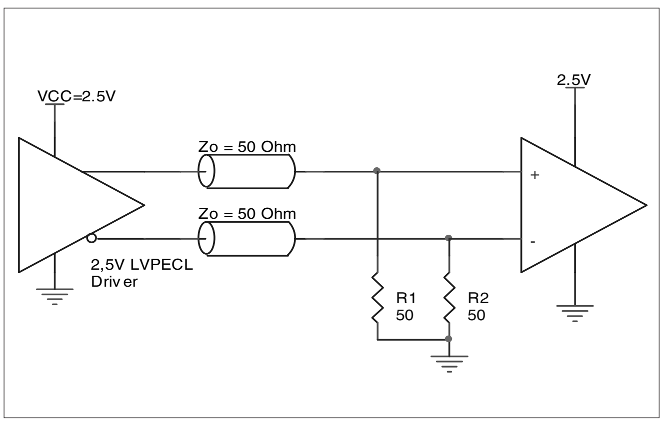


FIGURE 2C. 2.5V LVPECL TERMINATION EXAMPLE

APPLICATION SCHEMATIC EXAMPLE

Figure 3 shows an example of ICS85320I application schematic. In this example, the device is operated at V_{CC}=3.3V. The decoupling capacitor should be located as close as possible to the power pin. For LVPECL output termination, only two terminations examples are shown in this schematic. For more termination approaches, please refer to the LVPECL Termination Application Note.

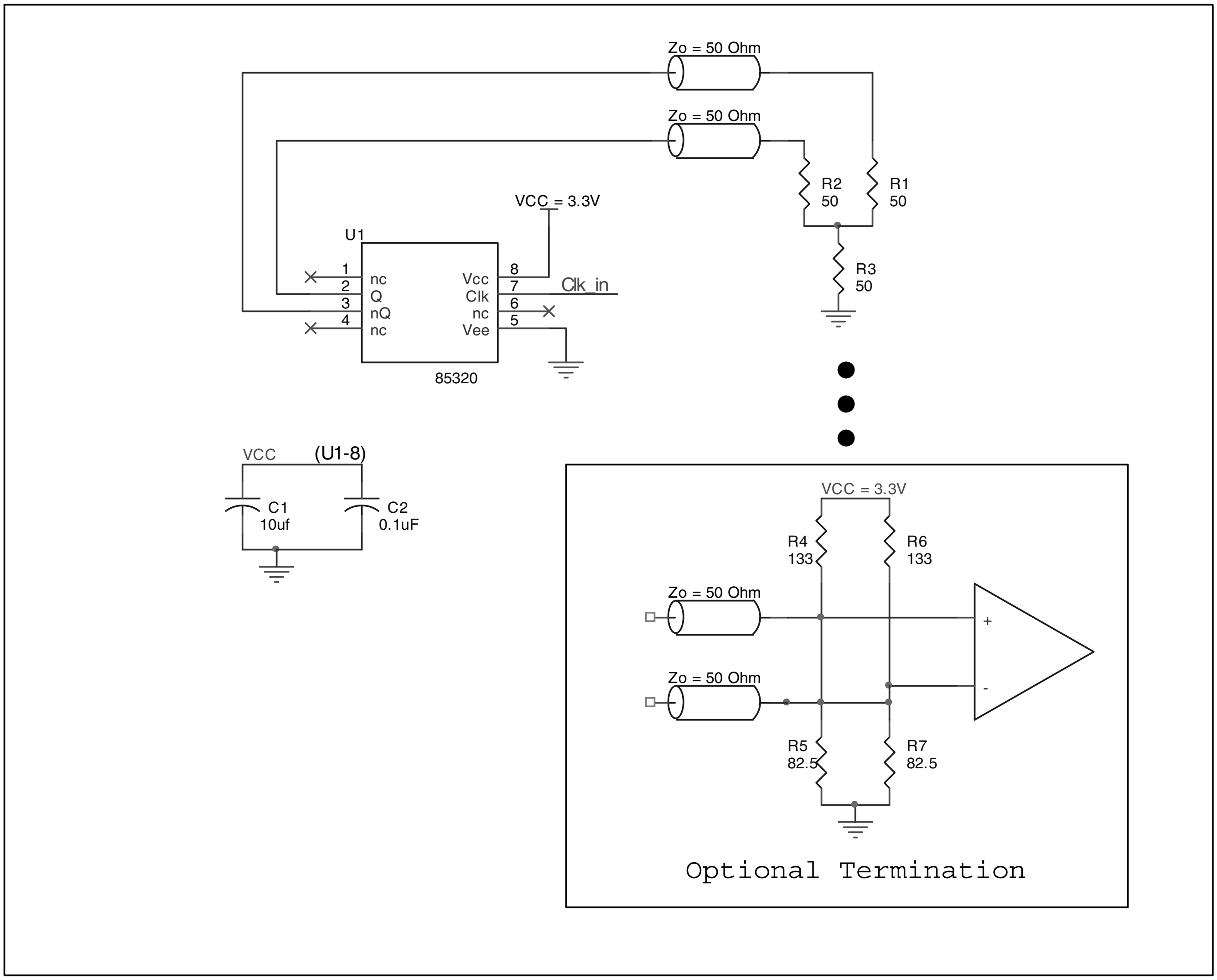


FIGURE 3. ICS85320I APPLICATION SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85320I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85320I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 25mA = **86.6mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 86.6mW + 30.2mW = **116.6mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.117W * 103.3°C/W = 97.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

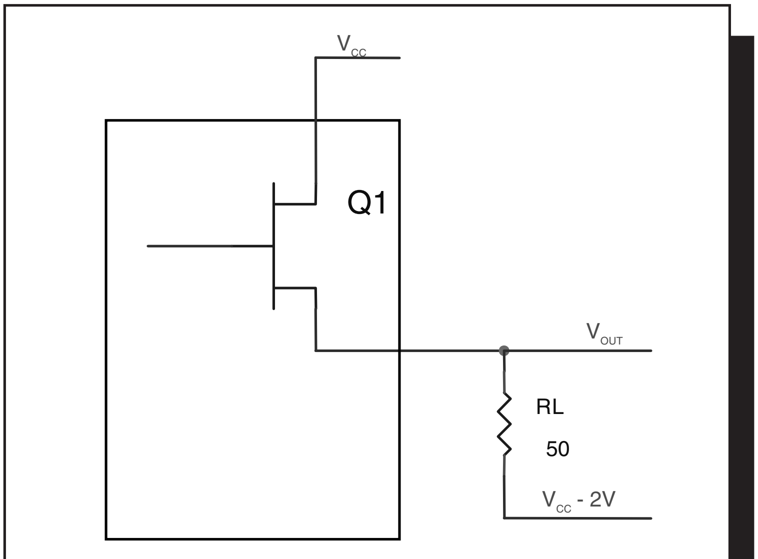


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 1.0V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85320I is: 269

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

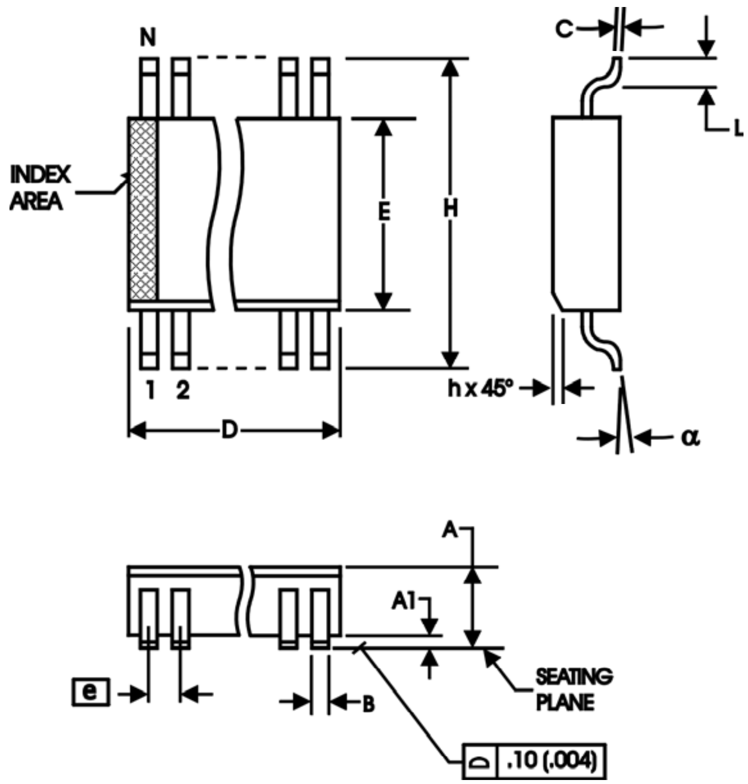


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85320AMI	5320AMI	8 lead SOIC	96 per tube	-40°C to 85°C
ICS85320AMIT	5320AMI	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C