PRELIMINARY

Integrated Circuit Systems, Inc.

ICS853111

LOW SKEW, 1-TO-10 DIFFERENTIAL-TO-2.5V/3.3V LVPECL/ECL FANOUT BUFFER

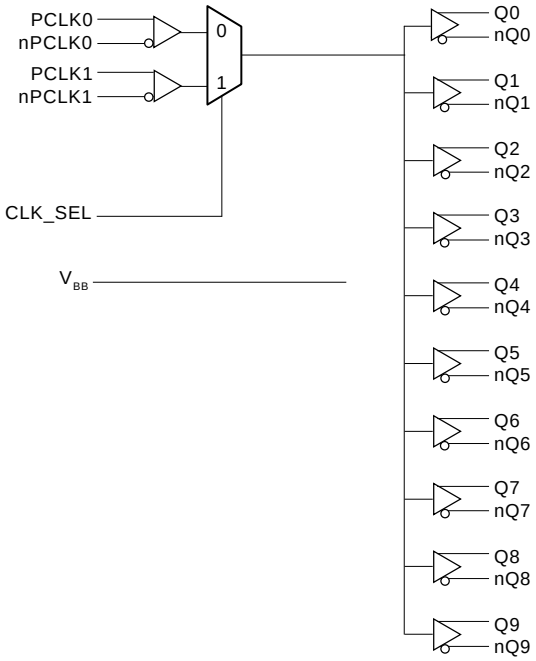
GENERAL DESCRIPTION

The ICS853111 is a low skew, high performance 1-to-10 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853111 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853111 ideal for those clock distribution applications demanding well defined performance and repeatability.

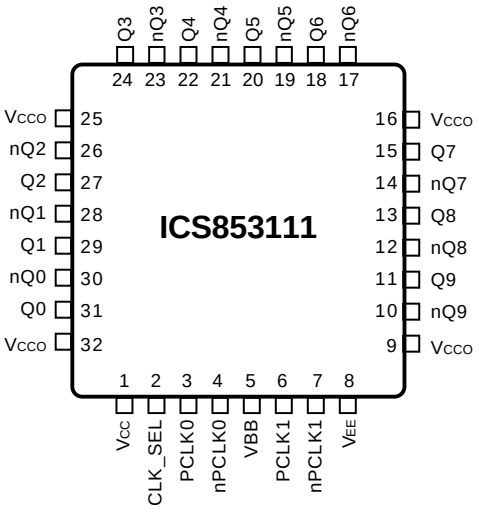
FEATURES

- 10 differential 2.5V/3.3V LVPECL / ECL outputs
- 2 selectable differential input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >3GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: TBD
- Part-to-part skew: TBD
- Propagation delay: TBD
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Pin compatible with MC100EP111 and MC100LVEP111

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CC}	Power		Core supply pin.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVCMOS / LVTTL interface levels.
3	PCLK0	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK0	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
5	V_{BB}	Output		Bias voltage.
6	PCLK1	Input	Pulldown	Non-inverting differential clock input.
7	nPCLK1	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
8	V_{EE}	Power		Negative supply pin.
9, 16, 25, 32	V_{CCO}	Power		Output supply pins.
10, 11	nQ9, Q9	Output		Differential output pair. LVPECL interface levels.
12, 13	nQ8, Q8	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ7, Q7	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ6, Q6	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		KΩ

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLKx	nCLKx	Q0:Q9	nQ0:Q9		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	Selected Source
0	CLK0, nCLK0
1	CLK1, nCLK1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	37.8°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375 TO 3.8V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current			TBD		mA

TABLE 4B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage(Single-Ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage(Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Single-ended input operation is limited $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.375	1.475	1.58	1.425	1.495	1.57	1.495	1.53	1.565	V
V_{OL}	Output Low Voltage; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage(Single-Ended)		1.275		1.56	1.275		1.56	1.275		-0.8	V
V_{IL}	Input Low Voltage(Single-Ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125V to -1.3V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is V_{CC} + 0.3V.

TABLE 4C. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.8V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.486		-1.386	-1.486		-1.386	-1.486		-1.386	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1	-150			-150			-150			µA

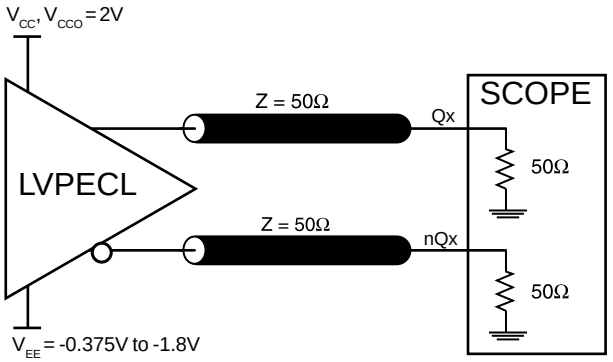
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Single-ended input operation is limited $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.8V TO -2.375V OR V_{CC} = 2.375 TO 3.8V; V_{EE} = 0V

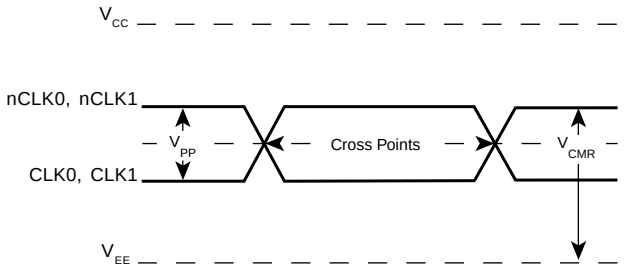
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>3			>3			>3		GHz
t_{PD}	Propagation Delay; NOTE 1			660			695			745		ps
*t*sk(o)	Output Skew; NOTE 2, 4			TBD			TBD			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD			TBD			TBD		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		TBD			TBD			TBD		ps

All parameters are measured ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

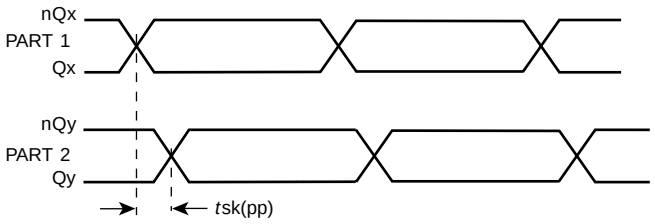
PARAMETER MEASUREMENT INFORMATION



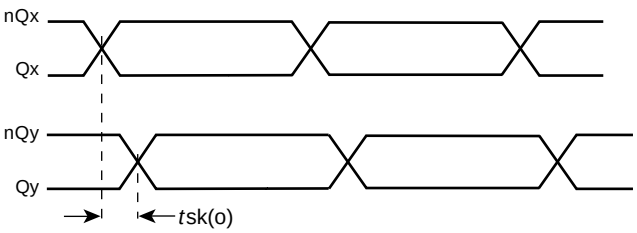
3.3V OUTPUT LOAD AC TEST CIRCUIT



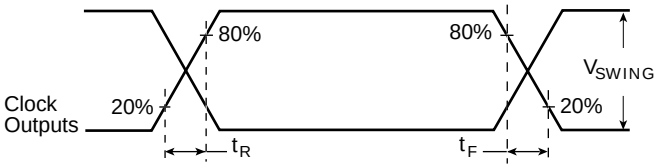
DIFFERENTIAL INPUT LEVEL



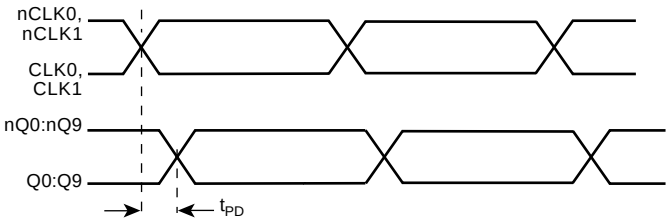
PART-TO-PART SKEW



OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS LEVELS

Figure 2A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

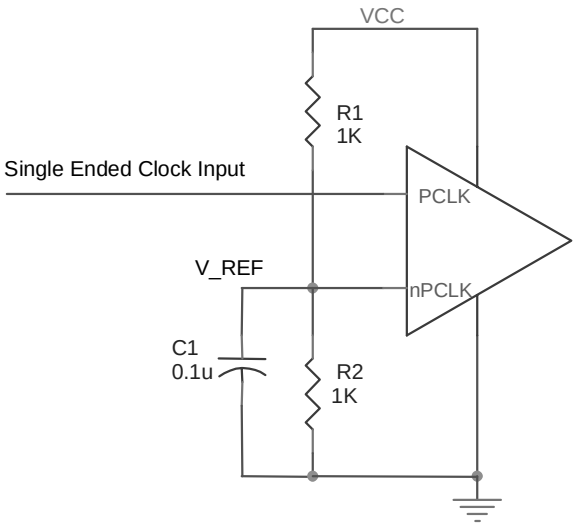


FIGURE 2A. SINGLE ENDED LVCMOS SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 2B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

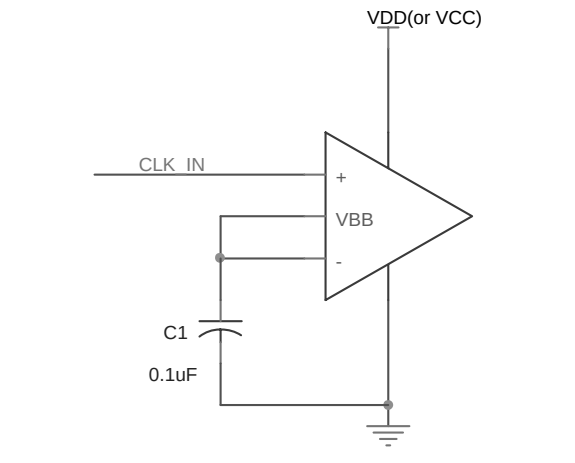


FIGURE 2B. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

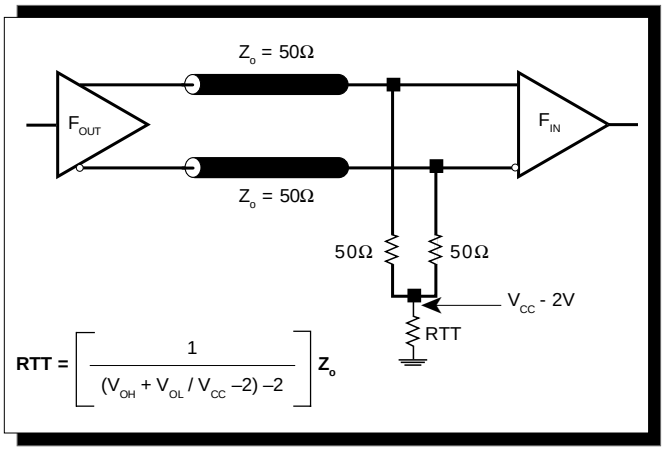


FIGURE 3A. LVPECL OUTPUT TERMINATION

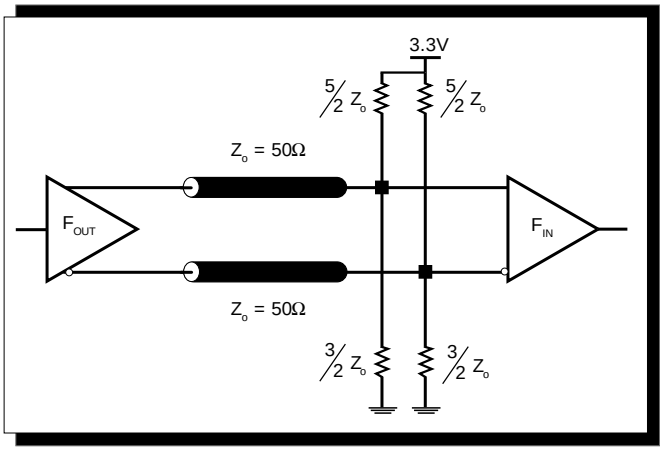


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in *Figure 4B* can be eliminated and the termination is shown in *Figure 4C.*

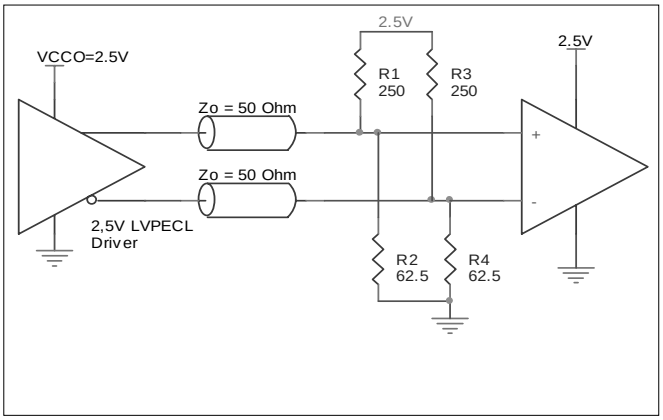


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

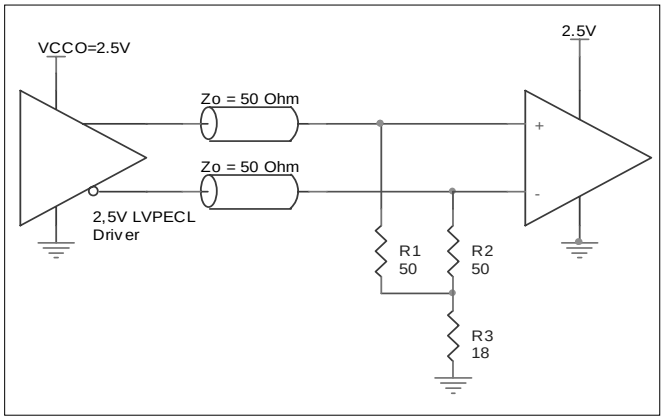


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

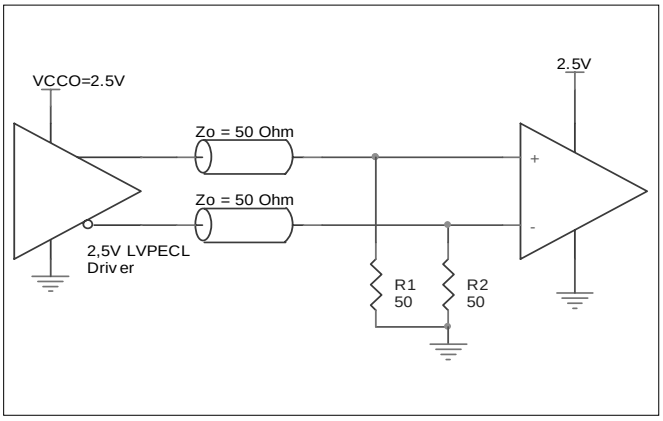


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

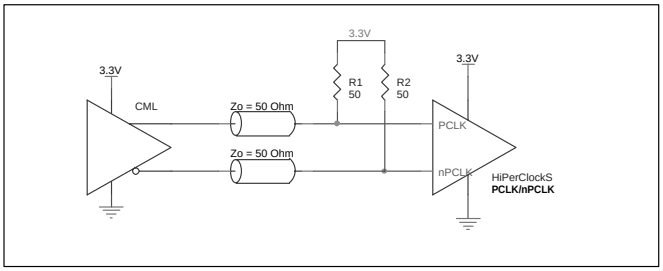


FIGURE 5A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A CML DRIVER

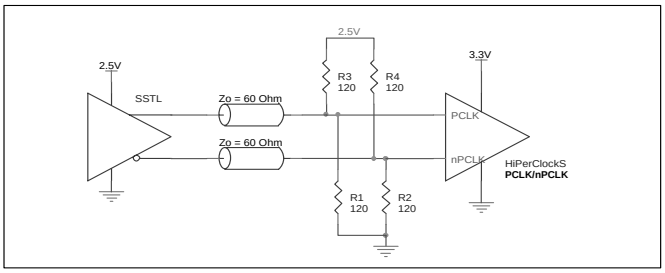


FIGURE 5B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

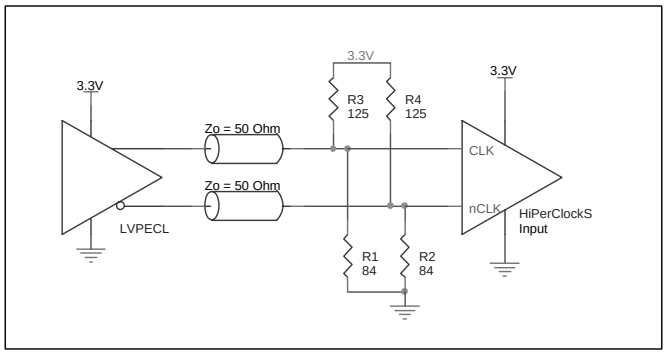


FIGURE 5C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

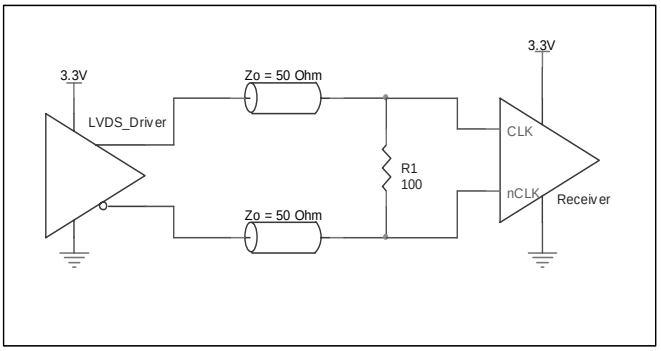


FIGURE 5D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

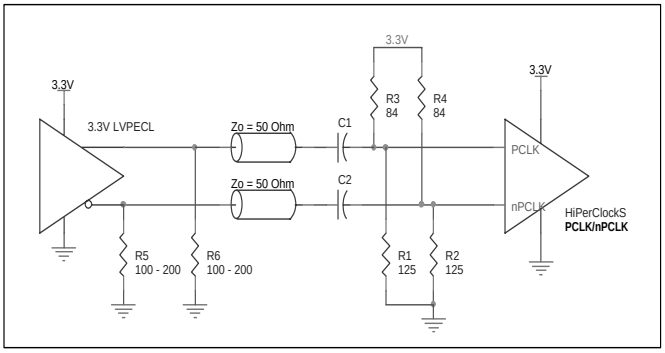


FIGURE 5E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

This application note provides general design guide using ICS853111 LVPECL buffer. *Figure 6* shows a schematic example of the ICS853111 LVPECL clock buffer. In this example, the input is driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK0/nPCLK0 input.

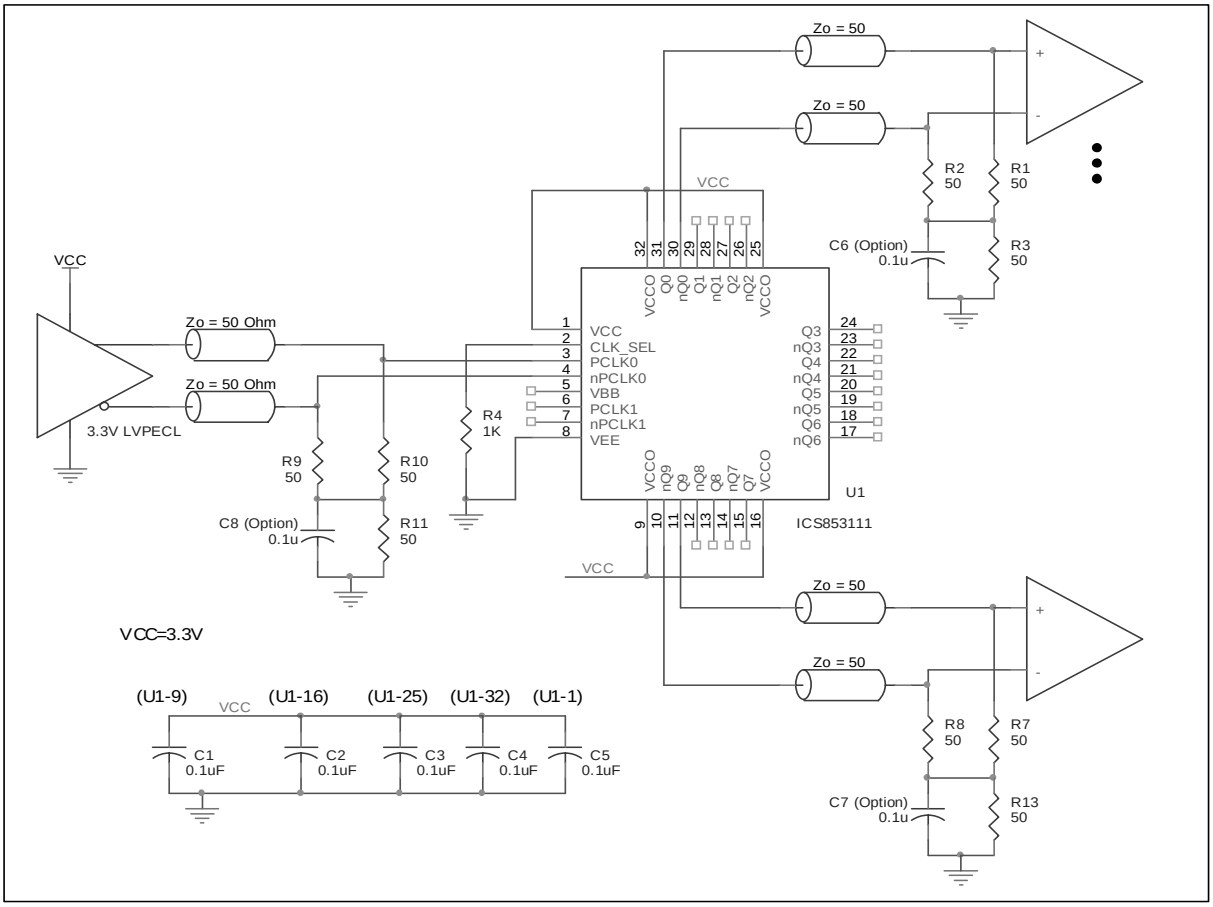


FIGURE 6. EXAMPLE ICS853111 LVPECL CLOCK OUTPUT BUFFER SCHEMATIC

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853111 is: 1340

PACKAGE OUTLINE - Y SUFFIX

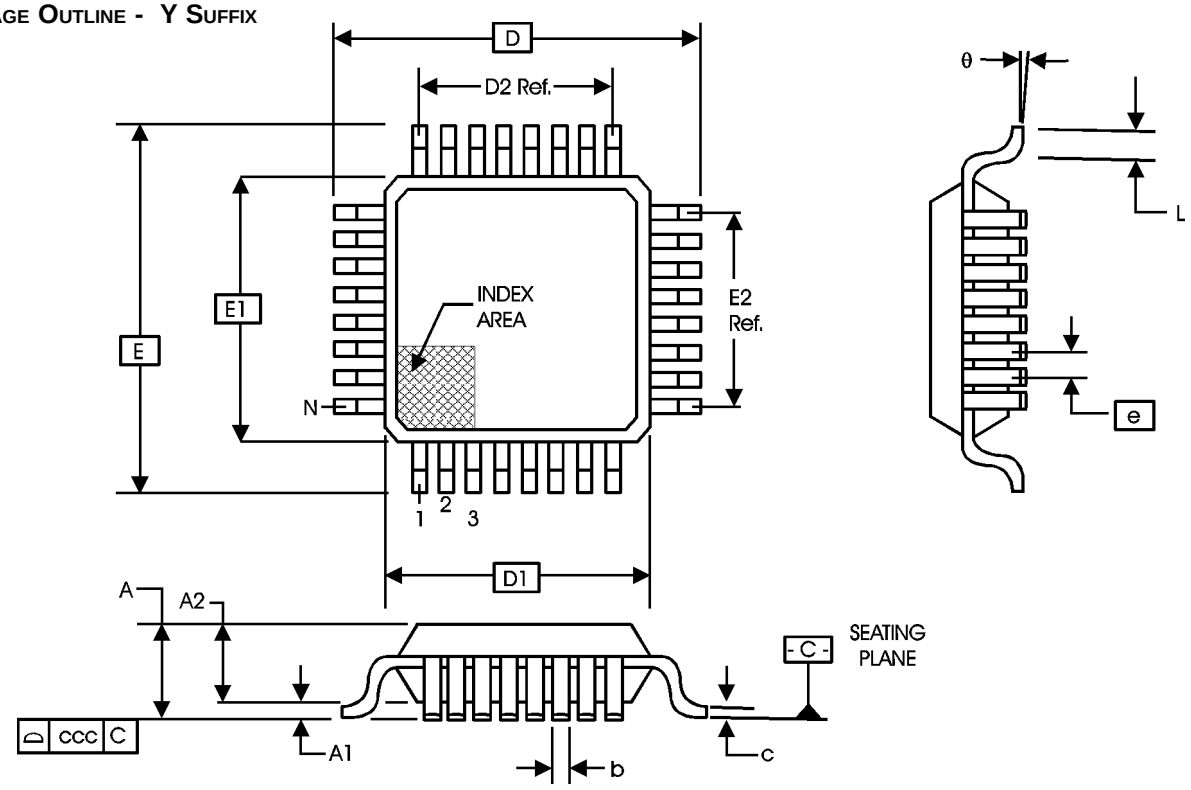


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS853111AY	ICS853111AY	32 lead LQFP	250 per tray	-40°C to 85°C
ICS853111AYT	ICS853111AY	32 lead LQFP on Tape and Reel	1000	-40°C to 85°C