LOW SKEW, 1-TO-8 DIFFERENTIAL/ LVCMOS-TO-LVCMOS FANOUT BUFFER

ICS8308I

General Description

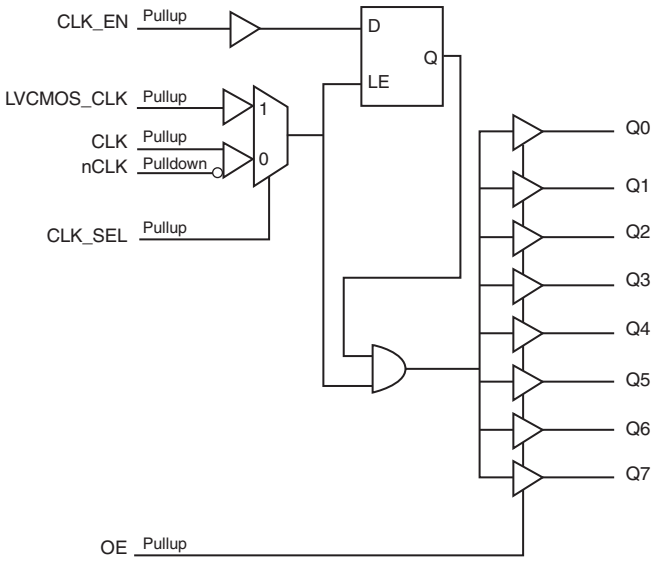
The ICS8308I is a low-skew, 1-to-8 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8308I has two selectable clock inputs. The CLK, nCLK pair can accept most differential input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 8 to 16 by utilizing the ability of the outputs to drive two series terminated transmission lines.

The ICS8308I is characterized for 3.3V core/3.3V output, 3.3V core/2.5V output or 2.5V core/2.5V output operation. Guaranteed output and part-part skew characteristics make the 8308I ideal for those clock distribution applications requiring well defined performance and repeatability.

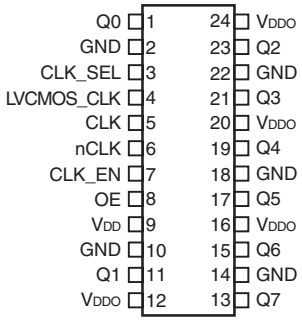
Features

- Eight LVCMOS/LVTTL outputs, (7Ω typical output impedance)
- Selectable LVCMOS_CLK or differential CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum Output Frequency: 350MHz
- Output Skew: (3.3V± 5%): 100ps (maximum)
- Part to Part Skew: (3.3V± 5%): 1ns (maximum)
- Supply Voltage Modes:
  (Core/Output)
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8308I
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.925mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11, 13, 15, 17, 19, 21, 23	Q0, Q1, Q7, Q6, Q5, Q4,Q3, Q2	Output		Clock outputs. LVCMOS / LVTTL interface levels.
2, 10, 14, 18, 22	GND	Power		Power supply ground.
3	CLK_SEL	Input	Pullup	Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK, nCLK inputs when LOW. See Table 3A. LVCMOS / LVTTL interface levels.
4	LVCMOS_CLK	Input	Pullup	Clock input. LVCMOS / LVTTL interface levels.
5	CLK	Input	Pullup	Non-inverting differential clock input.
6	nCLK	Input	Pulldown	Inverting differential clock input.
7	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTL interface levels.
8	OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels. See Table 3B.
9	V_{DD}	Power		Core supply pin.
12, 16, 20, 24	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			12		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock Input
CLK_SEL	
0	CLK, nCLK is selected
1	LVCMOS_CLK is selected

TABLE 3B. OE SELECT FUNCTION TABLE

Control Input	Output Operation
OE	
0	Outputs Q0:Q7 are in Hi-Z (disabled)
1	Outputs Q0:Q7 are active (enabled)

TABLE 3C. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q0:Q7		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40° to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				46	mA
I_{DDO}	Output Supply Current				11	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40° to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				46	mA
I_{DDO}	Output Supply Current				10	mA

Table 4C. Power Supply DC Characteristics, $V_{DD}, V_{DDO} = 2.5V \pm 5\%$, T_A = -40° to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				43	mA
I_{DDO}	Output Supply Current				10	mA

TABLE 4D. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_EN, OE				0.8	0.8
I_{IN}	Input Current		$V_{IN} = V_{DD}$ or V_{IN} = GND			300	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -24mA	2.4			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 24mA			0.55	V
			I_{OL} = 12mA			0.30	V
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to $V_{DDO}/2$.
See Parameter Measurement section, "3.3V Output Load AC Test Circuit".
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

TABLE 4E. DC CHARACTERISTICS, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_EN, OE				0.8	V
I_{IN}	Input Current		$V_{IN} = V_{DD}$ or V_{IN} = GND			300	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -15mA	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 15mA			0.6	V
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to $V_{DDO}/2$.
See Parameter Measurement section, "3.3V Output Load AC Test Circuit".
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

TABLE 4F. DC CHARACTERISTICS, V_{DD}, V_{DDO} = 2.5V±5%, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_EN, OE				0.7	V
I_{IN}	Input Current		V_{IN} = V_{DD} or V_{IN} = GND			300	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -15mA	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 15mA			0.6	V
V_{PP}	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "3.3V Output Load AC Test Circuit".
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
t_{PD}	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq$ 350MHz	2		4	ns
		LVCMOS_CLK; NOTE 2	$f \leq$ 350MHz	2		4	ns
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on rising edge @V_{DDO}/2			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on rising edge @V_{DDO}/2			1	ns
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	0.2		1	ns
odc	Output Duty Cycle		$f \leq$ 150MHz, Ref = CLK, nCLK	45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE 1: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40° TO 85°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
t_{PD}	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq$ 350MHz	2		4	ns
		LVCMOS_CLK; NOTE 2	$f \leq$ 350MHz	2		4	ns
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on rising edge @V_{DDO}/2			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on rising edge @V_{DDO}/2			1	ns
t_R / t_F	Output Rise/Fall Time		0.6V to 1.8V	0.2		1.0	ns
odc	Output Duty Cycle		$f \leq$ 150MHz, Ref = CLK, nCLK	45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

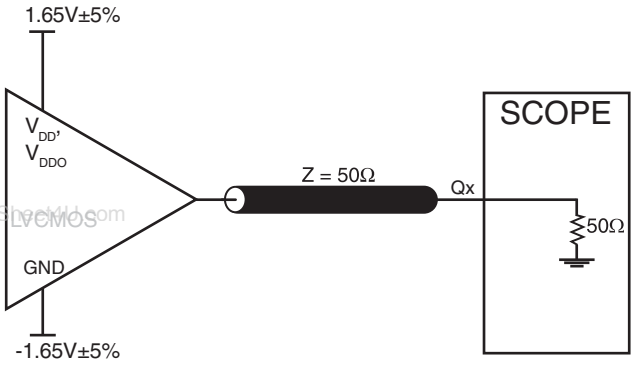
NOTE 1: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40° TO 85°

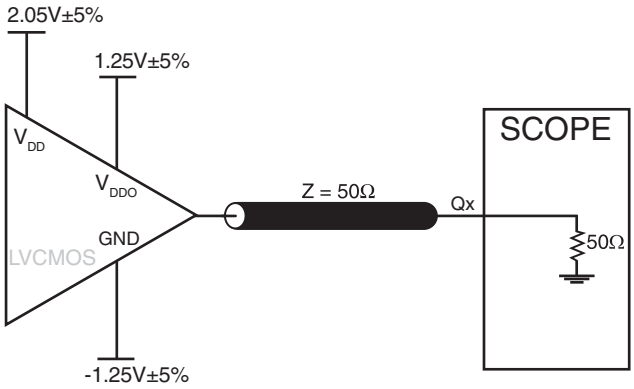
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
t_{PD}	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq$ 350MHz	1.5		4.2	ns
		LVCMOS_CLK; NOTE 2	$f \leq$ 350MHz	1.7		4.4	ns
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on rising edge @V_{DDO}/2			160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on rising edge @V_{DDO}/2			2	ns
t_R / t_F	Output Rise/Fall Time		0.6V to 1.8V	0.2		1.0	ns
odc	Output Duty Cycle		$f \leq$ 150MHz, Ref = CLK, nCLK	40		60	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE 1: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

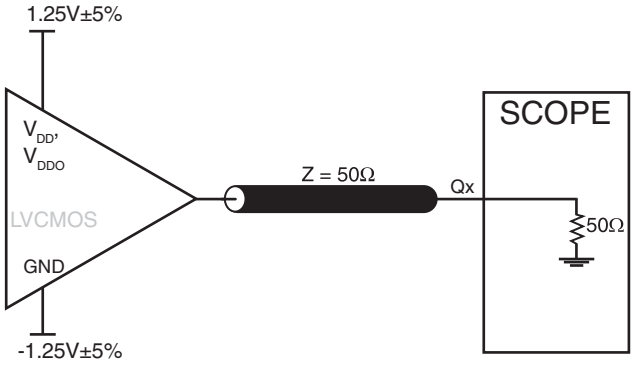
PARAMETER MEASUREMENT INFORMATION



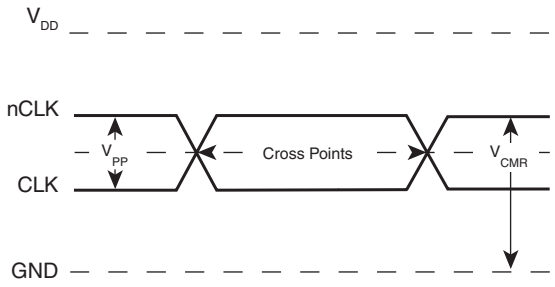
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



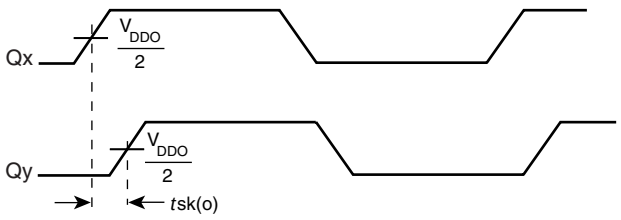
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



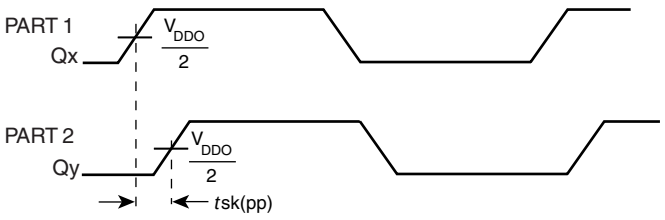
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



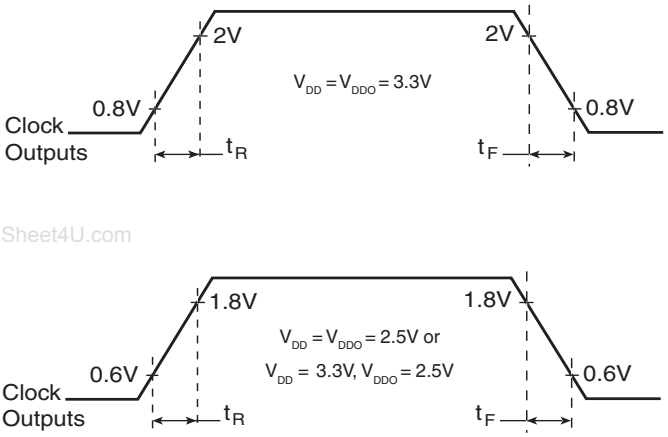
DIFFERENTIAL INPUT LEVEL



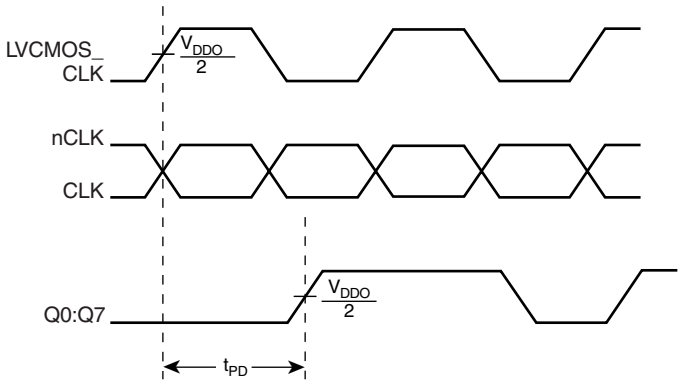
OUTPUT SKEW



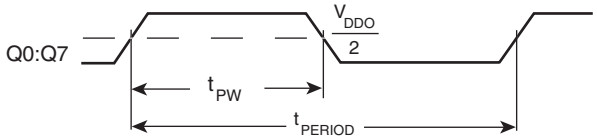
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

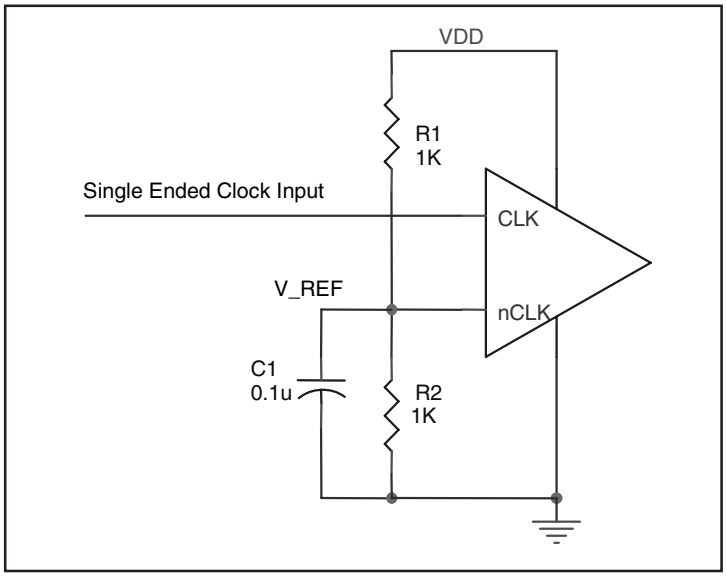


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK INPUTS
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS
All unused LVCMOS output can be left floating. There should be no trace attached.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

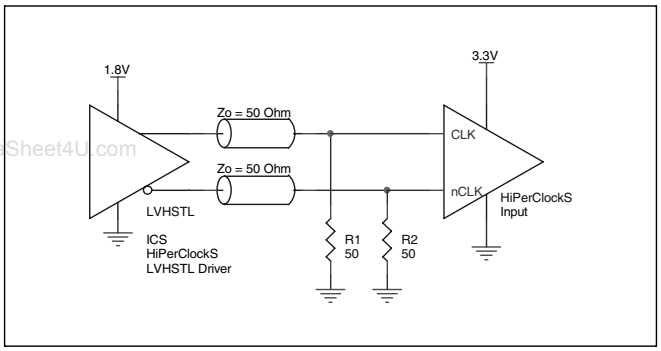


FIGURE 2A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

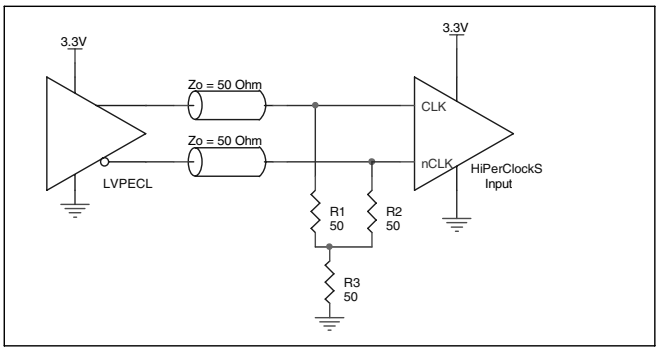


FIGURE 2B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

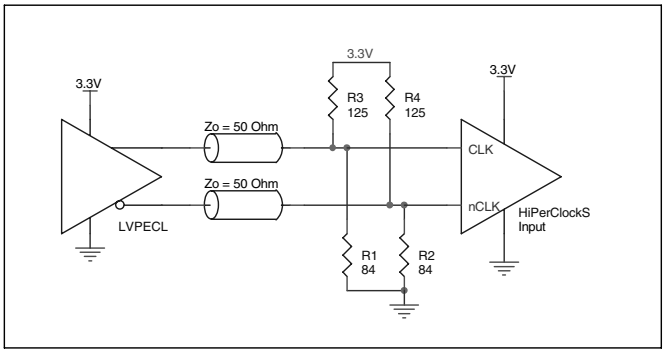


FIGURE 2C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

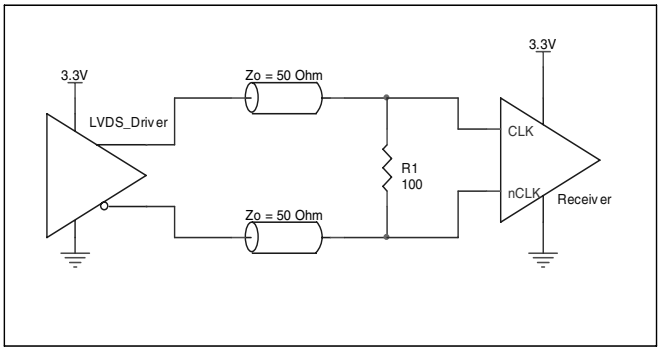


FIGURE 2D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

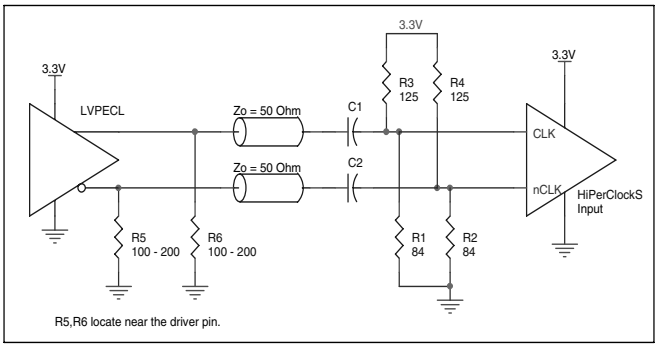


FIGURE 2E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of the ICS8308I. In this example, the LVCMOS_CLK input is selected. The decoupling capacitors should be physically located near the power pin.

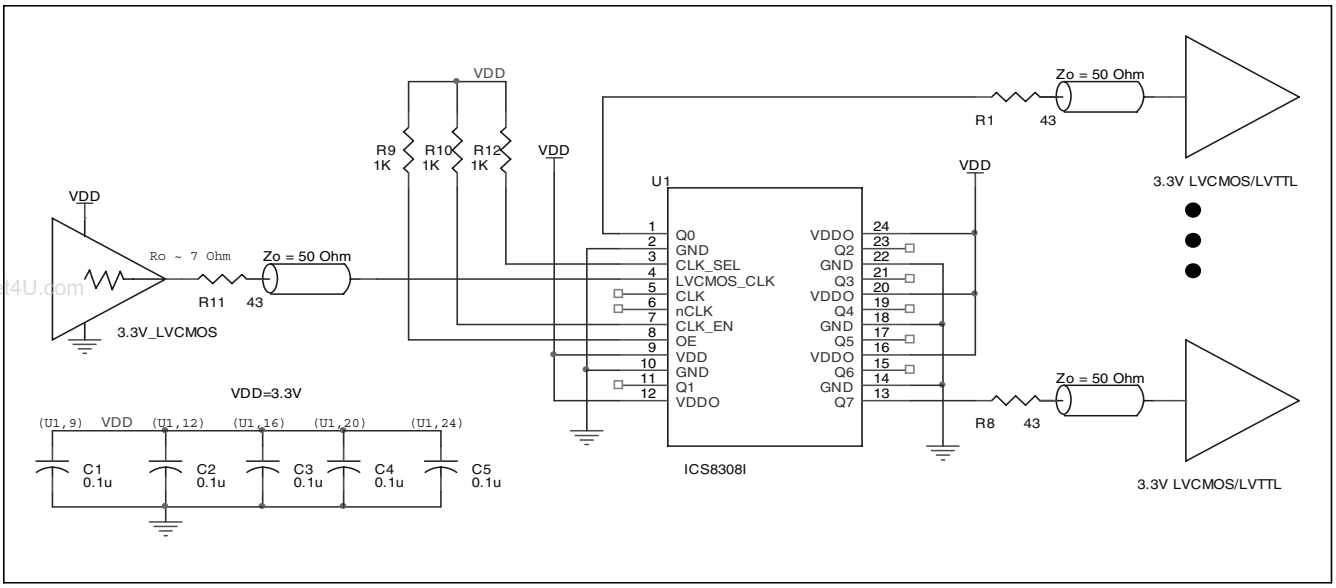


FIGURE 3. ICS8308I LVPECL BUFFER SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

TRANSISTOR COUNT

The transistor count for ICS8308I is: 1040

Package Outline - G Suffix for 24 Lead TSSOP

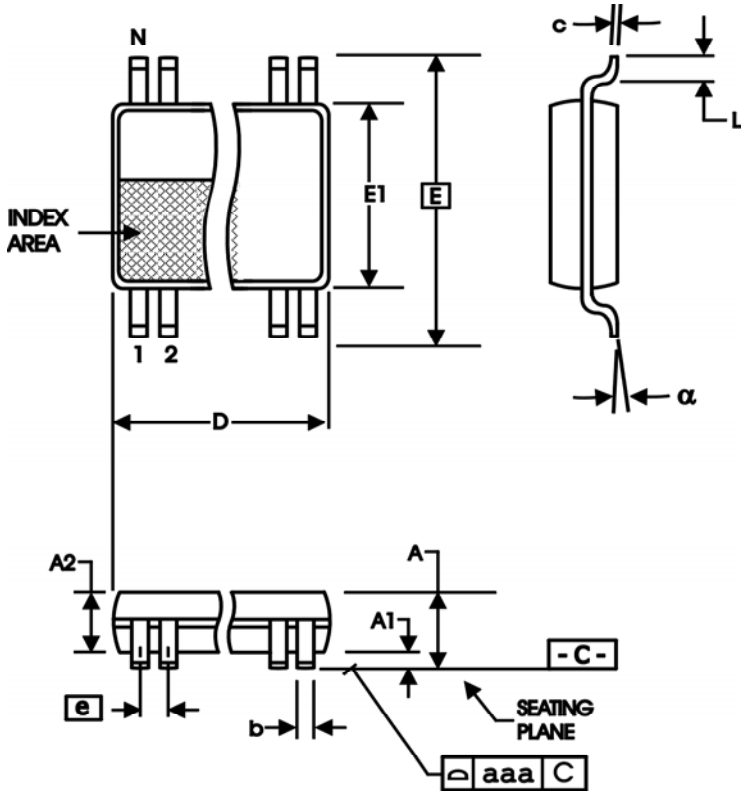


Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8308AGI	ICS8308AGI	24 Lead TSSOP	tube	-40°C to 85°C
ICS8308AGIT	ICS8308AGI	24 Lead TSSOP	tape & reel	-40°C to 85°C
ICS8308AGILF	ICS8308AGILF	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS8308AGILFT	ICS8308AGILF	24 Lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuraiton and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		11	Added Schematic Layout	4/16/04
B	T4B T4E T5B	1 3 4 6 8	Features section - added mix supply voltage bullet. Added Mix Power Supply Table. Added Mix DC Characteristics Table. Added Mix AC Characteristics Table. Added Mix Output Load AC Test Circuit Diagram.	10/20/04
B	T8	14	Ordering Information Table - added "Lead-Free" part number.	1/12/05
B	T8	1 10 14	Corrected Block Diagram, added CLK_SEL. Added "Recommendations for Unused Input and Output Pins". Ordering Information Table - added Lead-Free note.	7/25/05
B		1	Pin Assignment - corrected package information from 300-MIL to 173-MIL.	8/4/06
B	T3B	2	Added OE Select Function Table.	10/16/07

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