PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843002I-41

700MHz, FemtoClocks™ VCXO Based SONET/SDH Jitter Attenuator

General Description

The ICS843002I-41 is a member of the HiperClockS™ family of high performance clock solutions from ICS. The ICS843002I-41 is a PLL based synchronous clock generator that is optimized for SONET/SDH line card applications where jitter attenuation and frequency translation is needed. The device contains two internal PLL stages that are cascaded in series. The first PLL stage uses a VCXO which is optimized to provide reference clock jitter attenuation and to be jitter tolerant, and to provide a stable reference clock for the 2nd PLL stage (typically 19.44MHz). The second PLL stage provides additional frequency multiplication (x32), and it maintains low output jitter by using a low phase noise FemtoClock™ VCO. PLL multiplication ratios are selected from internal lookup tables using device input selection pins. The device performance and the PLL multiplication ratios are optimized to support non-FEC (non-Forward Error Correction) SONET/SDH applications with rates up to OC-48 (SONET) or STM-16 (SDH). The VCXO requires the use of an external, inexpensive pullable crystal. VCXO PLL uses external passive loop filter components which are used to optimize the PLL loop bandwidth and damping characteristics for the given line card application.

The ICS843002I-41 includes two clock input ports. Each one can accept either a single-ended or differential input. Each input port also includes an activity detector circuit, which reports input clock activity through the LOR0 and LOR1 logic output pins. The two input ports feed an input selection mux. “Hitless switching” is accomplished through proper filter tuning. Jitter transfer and wander characteristics are influenced by loop filter tuning, and phase transient performance is influenced by both loop filter tuning and alignment error between the two reference clocks.

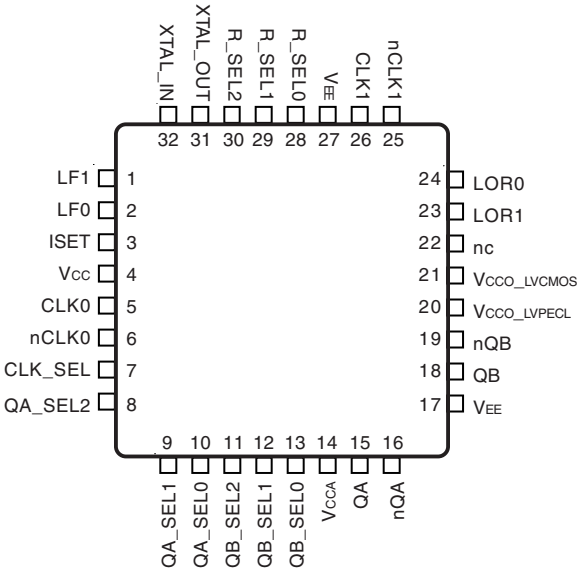
Typical ICS843002I-41 configuration in SONET/SDH Systems:

- VCXO 19.44MHz crystal
- Loop bandwidth: 50Hz - 250Hz
- Input Reference clock frequency selections: 19.44MHz, 38.88MHz, 77.76MHz, 155.52MHz, 311.04MHz, 622.08MHz
- Output clock frequency selections: 19.44MHz, 77.76MHz, 155.52MHz, 311.04MHz, 622.08MHz, Hi-Z

Features

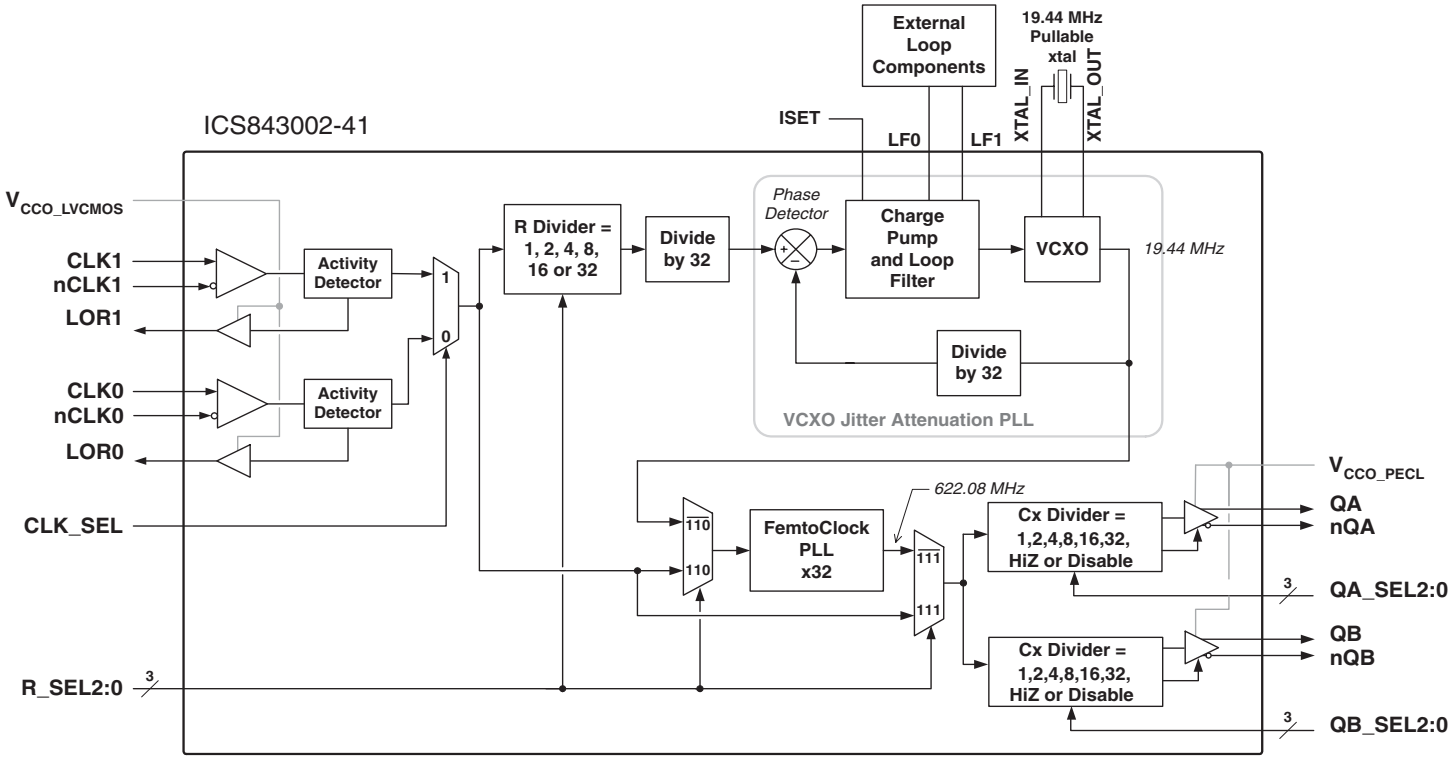
- (2) Differential LVPECL outputs
- Selectable CLKx, nCLKx differential input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL or single-ended LVCMOS or LVTTL levels
- Maximum output frequency: 700MHz
- FemtoClock VCO frequency range: 560MHz - 700MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz to 20MHz): 0.81ps (typical)
- Full 3.3V or mixed 3.3V core/2.5V output supply voltage
- -40°C to 85°C ambient operating temperature

Pin Assignment



ICS843002I-41
32-Lead VFQFN
5mm x 5mm x 0.75mm package body
K Package
Top View

Block Diagram



NOTE 1: 19.44MHz VCXO crystal shown is typical for SONET/SDH device applications.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4	V_{CC}	Power		Core power supply pin.
5	CLK0	Input	Pulldown	Non-inverting differential clock input.
6	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 bias voltage when left floating.
7	CLK_SEL	Input	Pulldown	Input clock select. LVCMOS/LVTTL interface levels. See Table 3A.
8	QA_SEL2	Input	Pulldown	LVPECL output divider control for QA/nQA outputs. See Table 3C.
9, 10	QA_SEL1, QA_SEL0	Input	Pullup	LVPECL output divider control for QA/nQA outputs. See Table 3C.
11	QB_SEL2	Input	Pulldown	LVPECL output divider control for QB/nQB outputs. See Table 3C.
12, 13	QB_SEL1, QB_SEL0	Input	Pullup	LVPECL output divider control for QB/nQB outputs. See Table 3C.
14	V_{CCA}	Power		Analog supply pin.
15, 16	QA, nQA	Output		Differential clock output pair. LVPECL interface levels.
17, 27	V_{EE}	Power		Negative supply pins.
18, 19	QB, nQB	Output		Differential clock output pair. LVPECL interface levels.
20	V_{CCO_LVPECL}	Power		Output power supply pin for QA, nQA and QB, nQB.
21	V_{CCO_LVCMOS}	Power		Power supply pin for LOR0 and LOR1.
22	nc	Unused		No connect.
23	LOR1	Output		Alarm output, loss of reference for CLK1. LVCMOS/LVTTL interface levels.
24	LOR0	Output		Alarm output, loss of reference for CLK0. LVCMOS/LVTTL interface levels.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28, 29, 30	R_SEL0, R_SEL1, R_SEL2	Input	Pulldown	Input divider selection. LVCMOS/LVTTL interface. See Table 3B.
31, 32	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ

Table 3A. Input Reference Selection Function Table

Inputs	
CLK_SEL	**Input Selected**
0	CLK0
1	CLK1

Table 3B. Input Reference Divider Selection Function Table

Inputs	
R_SEL2:0	**R Divider Value or State**
000	÷1
001	÷2
010	÷4
011	÷8
100	÷16
101	÷32
110	bypass VCXO PLL
111	bypass VCXO and FemtoClock™ PLL's

Table 3C. Output Divider Selection Function Table

Inputs	
Qx_SEL2:0	**Output Divider Value or State**
000	Output Q and nQ Hi-Z
001	÷32
010	÷8
011	÷4
100	÷16
101	÷2
110	÷1
111	Output Q at LVPECL V_{OL}, Output nQ at LVPECL V_{OH}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	34.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, V_{CCO_LVCMOS}, $V_{CCO\_LVPECL} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO_LVCMOS}, V_{CCO_LVPECL}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current			175		mA
I_{CCA}	Analog Supply Current			10		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO\_LVCMOS} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, QA_SEL2, QB_SEL2, R_SEL0:R_SEL2	$V_{CC} = V_{IN} = 3.465V$			150	µA
		QA_SEL0:1, QB_SEL0:1	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK_SEL, QA_SEL2, QB_SEL2, R_SEL0:R_SEL2	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		QA_SEL0:1, QB_SEL0:1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	LOR0, LOR1; NOTE 1	$V_{CCO\_LVCMOS} = 3.3V$	2.6			V
			$V_{CCO\_LVCMOS} = 2.5V$	1.8			V
V_{OL}	Output Low Voltage	LOR0, LOR1; NOTE 1	$V_{CCO\_LVCMOS} = 3.3V$ or 2.5V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_LVCMOS}/2$ .See Parameter Measurement Information Section, "Output Load Test Circuit".

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO\_LVPECL} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{CC} = 3.465V$			150	µA
		nCLK0, nCLK1				150	µA
I_{IL}	Input Low Current	CLK0, CLK1	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-5			µA
		nCLK0, nCLK1	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{CC} + 0.3V.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO\_LVPECL} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO_LVPECL} - 2V. See "Parameter Measurement Information" section, "Output Load Test Circuit".

Table 5. Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_N	Nominal Frequency			19.44		MHz
f_T	Frequency Tolerance				±TBD	ppm
f_S	Frequency Stability				±TBD	ppm
	Operating Temperature Range		0		70	°C
C_L	Load Capacitance			12		pF
C_O	Shunt Capacitance			4		pF
C_O/C_1	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				50	Ω
	Drive Level				1	mW
	Mode of Operation		Fundamental			

Table 6A. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$, V_{CCO_LVPECL} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		19.44		700	MHz
*t*jit(ø)	RMS Phase Jitter, (Random); NOTE 1	155.52MHz, Integration range: 12kHz - 20MHz		0.81		ps
*t*sk(o)	Output Skew; NOTE 2, 3			105		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		890		ps
odc	Output Duty Cycle			50		%

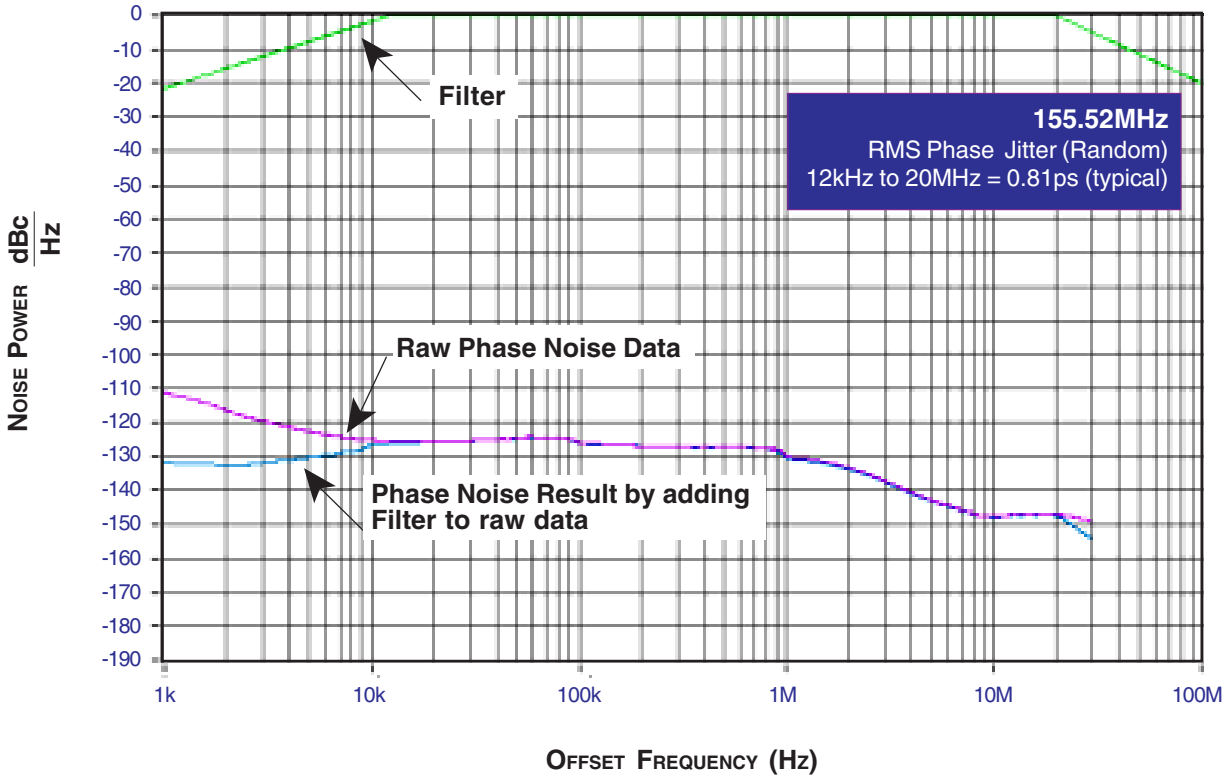
See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 6B. AC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO_LVCMOS}, V_{CCO_LVPECL} = 2.5V±5%, T_A = -40°C to 85°C

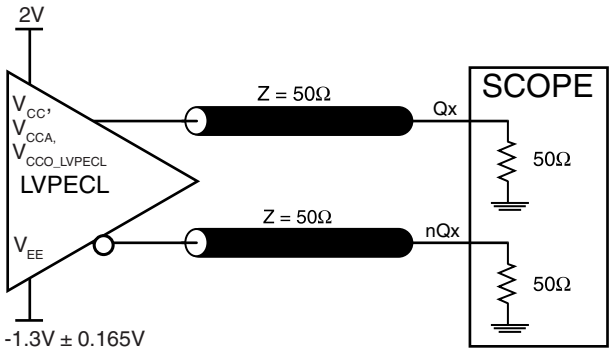
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		19.44		700	MHz
*t*jit(ø)	RMS Phase Jitter, (Random); NOTE 1	155.52 MHz, Integration range: 12kHz - 20MHz		0.83		ps
*t*sk(o)	Output Skew; NOTE 2, 3			95		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		900		ps
odc	Output Duty Cycle			50		%

See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

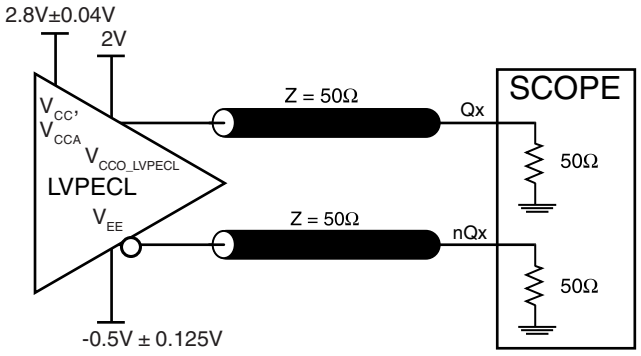
Typical Phase Noise at 155.52MHz



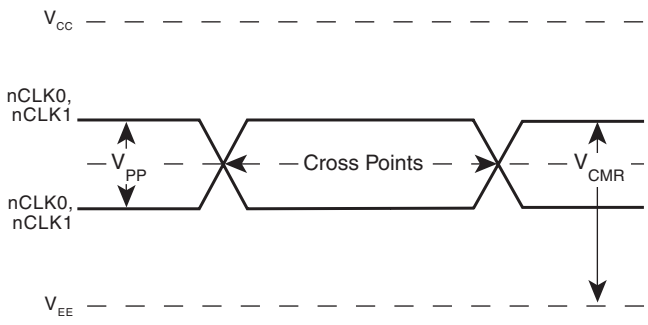
Parameter Measurement Information



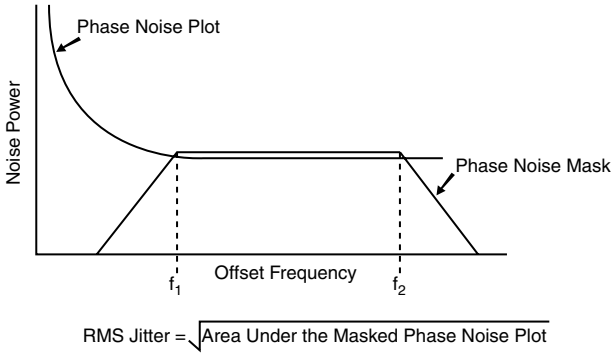
3.3V Core/3.3V LVPECL Output Load AC Test Circuit



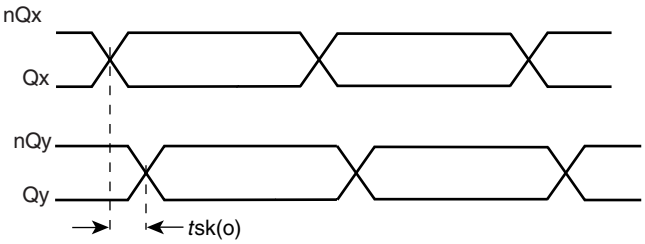
3.3V Core/2.5V LVPECL Output Load AC Test Circuit



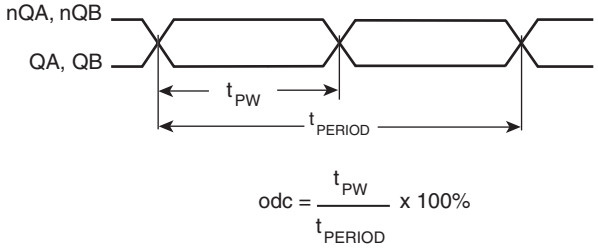
Differential Input Level



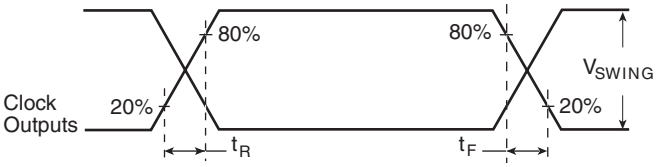
Phase Jitter



Output Skew



Output Duty Cycle/Pulse Width/tPeriod



Output Rise/Fall Time

Application Information

Description of the PLL Stages

The ICS843002I-41 is a two stage device, a VCXO PLL followed by a low phase noise FemtoClock PLL. The VCXO uses an external pullable crystal which can be pulled ±100ppm by the VCXO PLL circuitry to phase lock it to the input reference frequency. The FemtoClock PLL is a wide bandwidth PLL (about 800kHz) which means it will phase track the VCXO PLL. Most of the reference clock jitter attenuation needs to be accomplished by VCXO PLL.

By using the bypass FemtoClock PLL mode (Table 3B), the selected input reference clock can be passed directly to the FemtoClock PLL which will multiply it up by 32 to a higher frequency. A second mode, VCXO and FemtoClock bypass, routes the selected input refrence directly to the LVPECL output dividers.

VCXO PLL Loop Response Considerations

Loop response characteristics of the VCXO PLL is affected by the VCXO feedback divider value (bandwidth and damping factor), and by the external loop filter components (bandwidth, damping factor, and 2nd frequency response). A practical range of VCXO PLL bandwidth is from about 10Hz to about 1kHz. The setting of VCXO PLL bandwidth and damping factor is covered later in this document. A PC based PLL bandwidth calculator is also under development. For assistance with loop bandwidth suggestions or value calculation, please contact ICS applications.

Setting the VCXO PLL Loop Response

The VCXO PLL loop response is determined both by fixed device characteristics and by other characteristics set by the user. This includes the values of R_S, C_S, C_P and R_{SET} as shown in the External VCXO PLL Components figure on this page.

The VCXO PLL loop bandwidth is approximated by:

$$\text{NBW (VCXO PLL)} = \frac{R_S \times I_{CP} \times K_O}{32}$$

Where:

R_S = Value of resistor R_S in loop filter in Ohms

I_{CP} = Charge pump current in amps (see table on page 12)

K_O = VCXO Gain in Hz/V

The above equation calculates the “normalized” loop bandwidth (denoted as “NBW”) which is approximately equal to the - 3dB bandwidth. NBW does not take into account the effects of damping factor or the second pole imposed by C_P. It does, however, provide a useful approximation of filter performance.

To prevent jitter on the clock output due to modulation of the VCXO PLL by the phase detector frequency, the following general rule should be observed:

$$\text{NBW (VCXO PLL)} \leq \frac{f\,\text{(Phase Detector)}}{20}$$

f(Phase Detector) = Input Frequency ÷ (R Divider x 32)

The PLL loop damping factor is determined by:

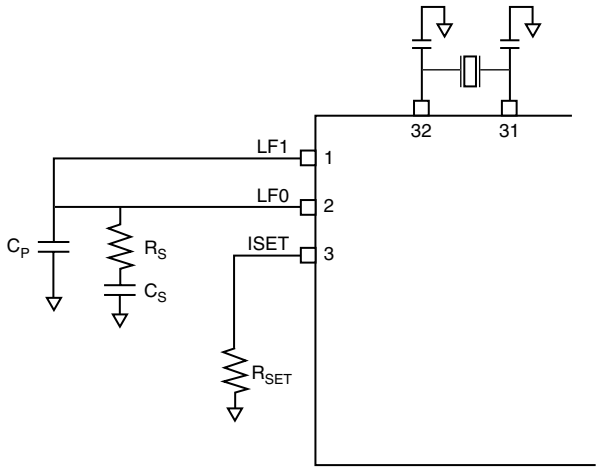
$$\text{DF (VCLK)} = \frac{R_S}{2} \times \sqrt{\frac{I_{CP} \times C_S \times K_O}{32}}$$

Where:

C_S = Value of capacitor C_S in loop filter in Farads

EXTERNAL VCXO PLL COMPONENTS

In general, the loop damping factor should be 0.7 or greater to ensure output stability. A higher damping factor will create less peaking in the passband. A higher damping factor may also increase lock time and output clock jitter when there is excess digital noise in the system application, due to the reduced ability of the PLL to respond to and therefore compensate for phase noise ingress.



The external crystal devices and loop filter components should be kept close to the device. Loop filter and crystal PCB connection traces should be kept short and well separated from each other and from other signal traces. Other signal traces should not run underneath the device, the loop filter or crystal components.

NOTES ON SETTING THE VALUE OF C_P

As another general rule, the following relationship should be maintained between components C_S and C_P in the loop filter:

$$C_P = \frac{C_S}{20}$$

C_P establishes a second pole in the VCXO PLL loop filter. For higher damping factors (> 1), calculate the value of C_P based on a C_S value that would be used for a damping factor of 1. This will minimize baseband peaking and loop instability that can lead to output jitter.

C_P also dampens VCXO PLL input voltage modulation by the charge pump correction pulses. A C_P value that is too low will result in increased output phase noise at the phase detector frequency due to this. In extreme cases where input jitter is high, charge pump current is high, and C_P is too small, the VCXO PLL input voltage can hit the supply or ground rail resulting in non-linear loop response.

The best way to set the value of C_P is to use the filter response software under development from ICS (please refer to the following section). C_P should be increased in value until it just starts affecting the passband peak.

LOOP FILTER RESPONSE SOFTWARE

Online tools to calculate loop filter response (coming soon) at www.icst.com. Contact your local sales representative if a tool cannot be found for this product.

NOTES ON EXTERNAL CRYSTAL LOAD CAPACITORS

In the loop filter schematic diagram, capacitors are shown between pins 32 to ground and between pins 31 to ground. These are optional crystal load capacitors which can be used to center tune the external pullable crystal (the crystal frequency can only be lowered by adding capacitance, it cannot be raised). Note that the addition of external load capacitors will decrease the crystal pull range and the Kvco value.

LOSS OF REFERENCE INDICATOR (LOR0 AND LOR1) OUTPUT PINS.

The LOR0 and LOR1 pins are controlled by the internal clock activity monitor circuits. The clock activity monitor circuits are clocked by the VCXO PLL phase detector feedback clock. The LOR output is asserted high if there are three consecutive feedback clock edges without any reference clock edges (in both cases, either a negative or positive transition is counted as an “edge”). The LOR output will otherwise be low. The activity monitor does not flag excessive reference transitions in an phase detector observation interval as an error. The monitor only distinguishes between transitions occurring and no transitions occurring.

Notes on Setting Charge Pump Current

The recommended range for the charge pump current is 50µA to 300µA. Below 50µA, loop filter charge leakage, due to PCB or capacitor leakage, can become a problem. This loop filter leakage can cause locking problems, output clock cycle slips, or low frequency phase noise.

As can be seen in the loop bandwidth and damping factor equations or by using the filter response software available from ICS, increasing charge pump current (I_{CP}) increases both bandwidth and damping factor.

Charge Pump Current, Example Settings

R_{SET}	Charge Pump Current (I_{CP})
17.6k	62.5µA
8.8k	125µA
4.4k	250µA
2.2k	500µA

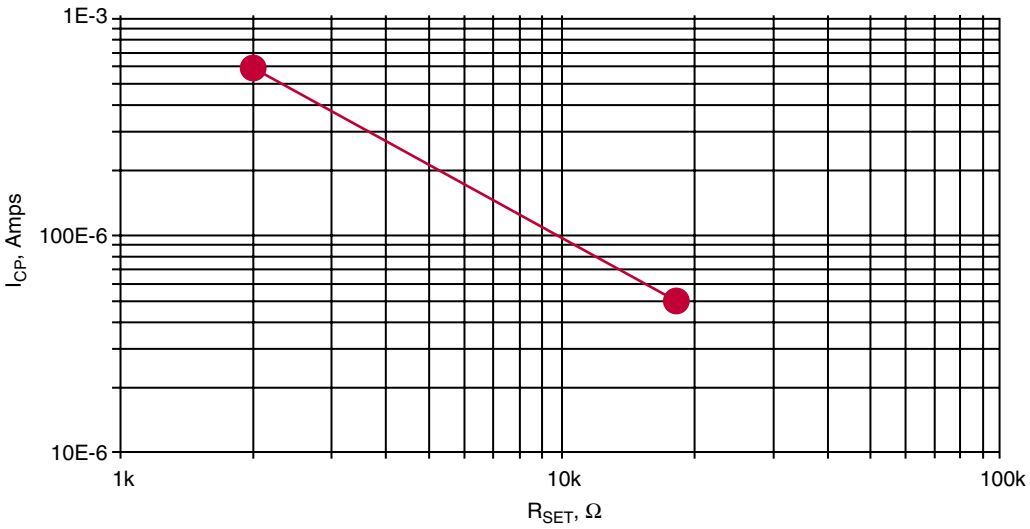


Figure 1. Charge Pump Current vs. Value of R_{SET} (External Resistor) Graph

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843002I-41 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_X} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

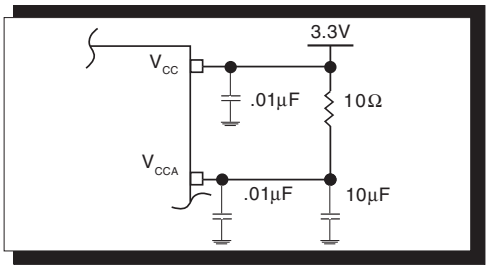


FIGURE 2. POWER SUPPLY FILTERING

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

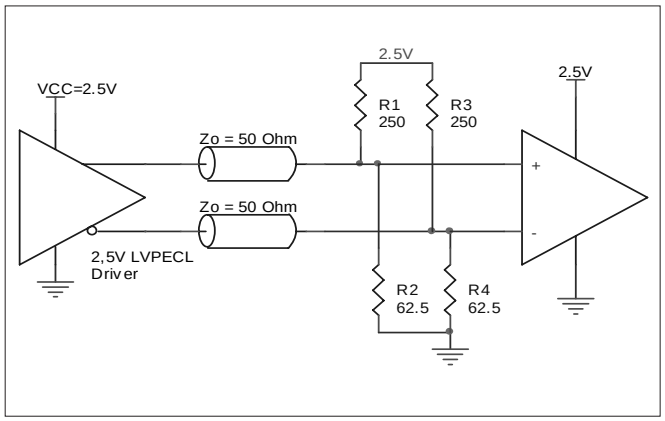


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

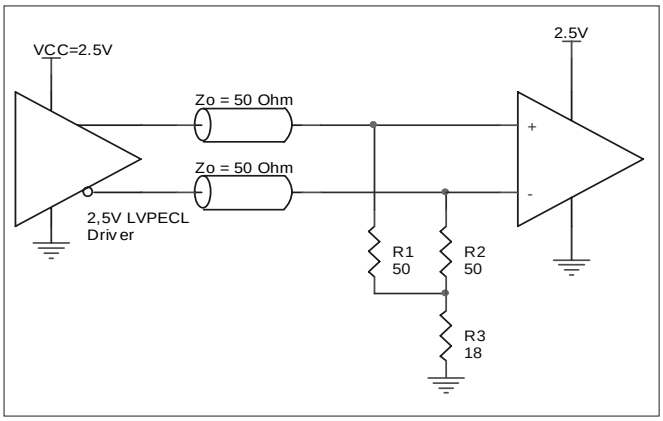


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

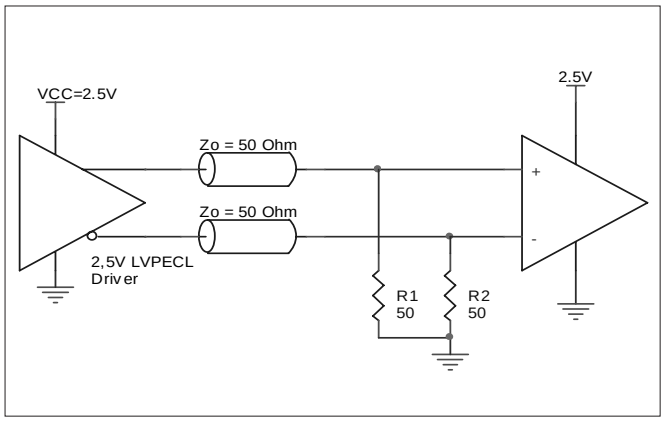


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

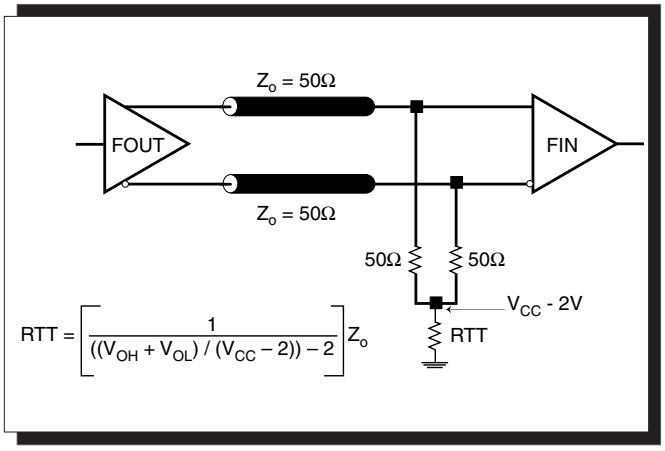


Figure 4A. LVPECL Output Termination

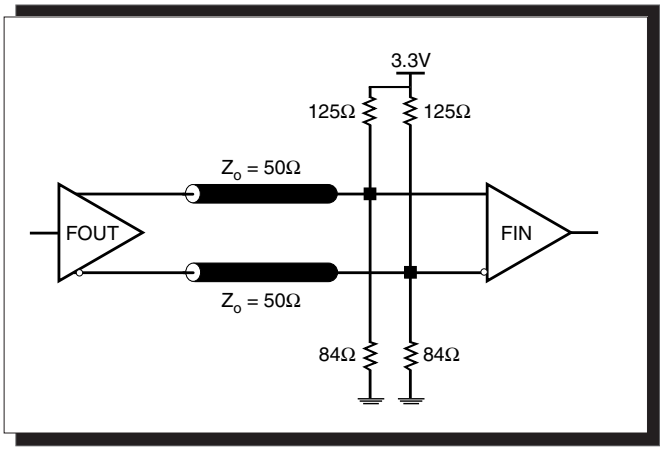


Figure 4B. LVPECL Output Termination

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 5A to 5E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 5A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

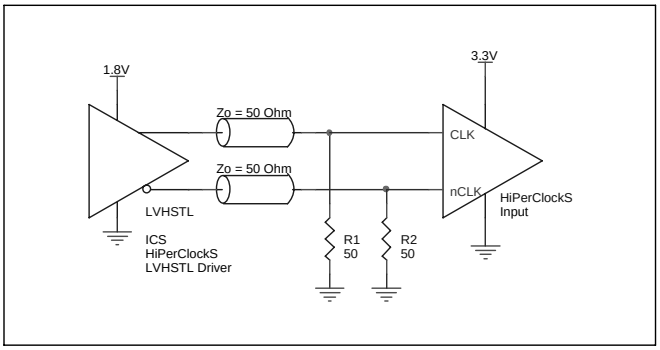


Figure 5A. HiPerClockS CLK/nCLK Input Driven by ICS HiPerClockS LVHSTL Driver

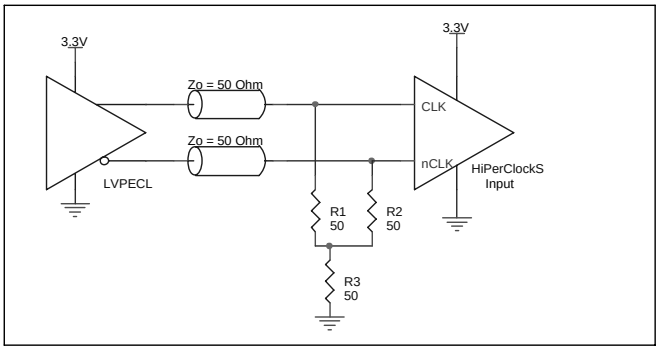


Figure 5B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

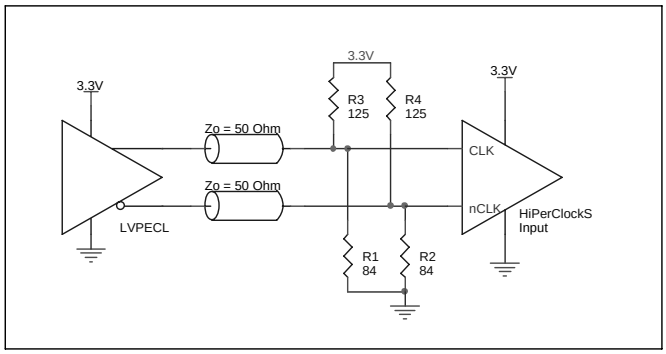


Figure 5C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

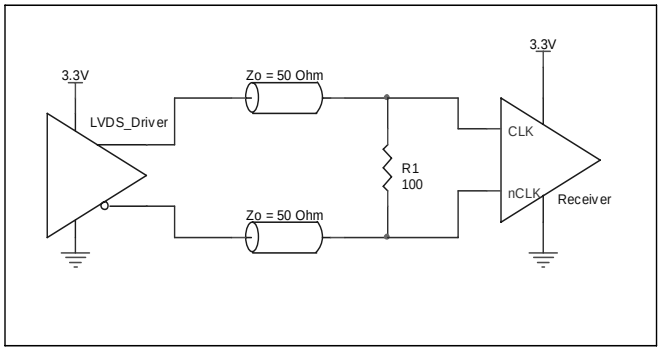


Figure 5D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

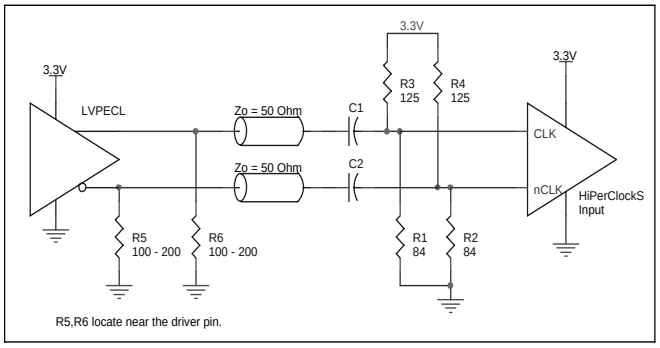


Figure 5E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

Single Ended Clock Input Interface

When using a LVCMOS or LVTTL clock driver, the clock input is connected to the CLKx (CLK0 or CLK1) input pin. The nCLKx (nCLK0 or nCLK1) pin is left unconnected. To help reduce interference with the internal VCO circuits, an external resistor can be placed in series with the clock signal right near the CLKx input pin. Combined with the input pin capacitance, this resistor acts as a low pass signal filter. The typical value for this optional series filter resistor is 100Ω. This will lower both the amplitude and edge rate of the clock input signal. In the case of a very short clock trace a series termination resistor may not be needed.

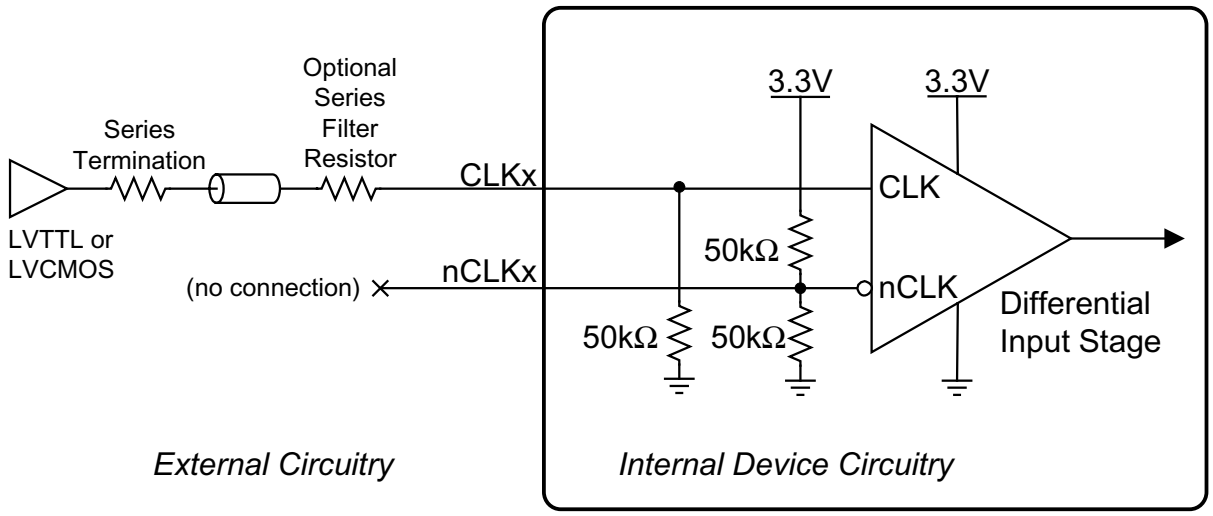


Figure 6. Single-Ended Clock Input Interface

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843002I-41. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843002I-41 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 175mA = **606.375mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **120mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 606.375mW + 60mW = 666.38**mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming an air flow of 0 linear feet per minute and a multi-layer board, the appropriate value is 34.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.666W * 34.8°C/W = 108.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32-pin VFQFN, Forced Convection

θ_{JA} vs. Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

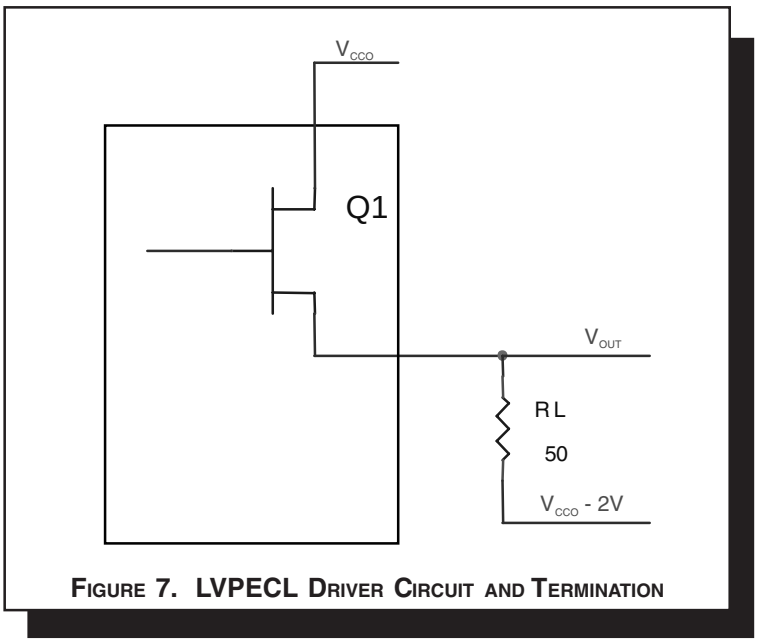


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega) * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega) * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

Transistor Count

The transistor count for ICS843002I-41 is: 5536

Package Outline - K Suffix for a 32 Lead VFQFN

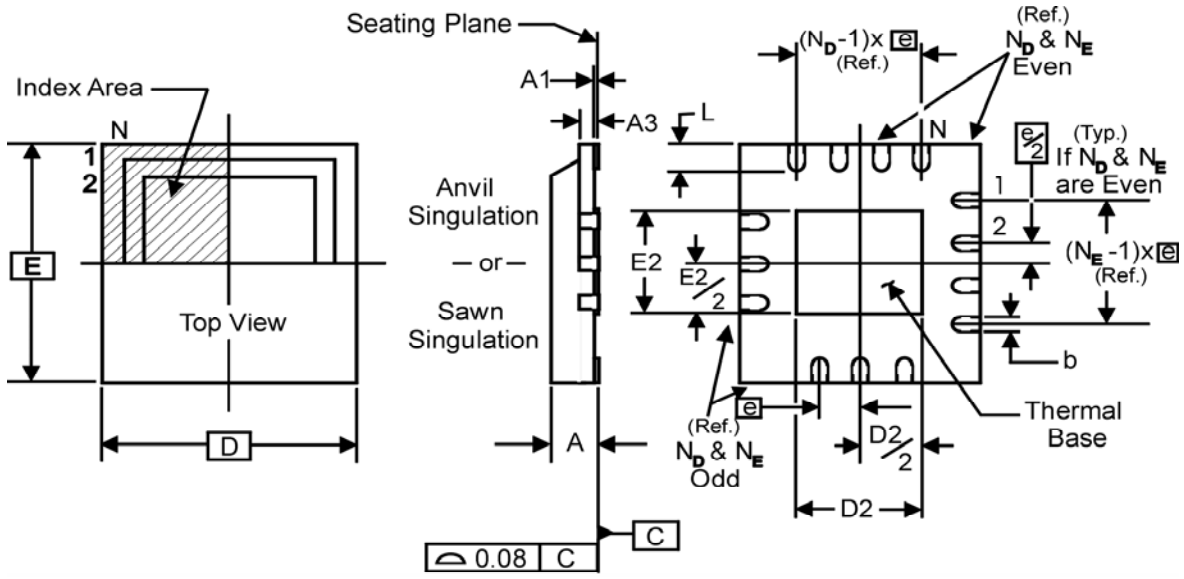


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	1.25	2.25	3.25
E		5.00 BASIC	
E2	1.25	2.25	3.25
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843002AKI-41	ICS43002A41	32 Lead VFQFN	tray	-40°C to 85°C
ICS843002AKI-41T	ICS43002A41	32 Lead VFQFN	2500 tape & reel	-40°C to 85°C