

OptiMOS™ - 6 Power-Transistor



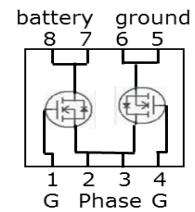
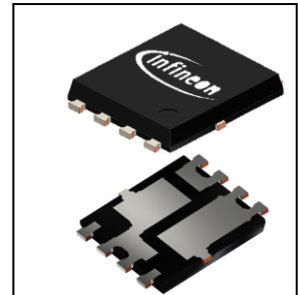
Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	3.0	mΩ
I_D	60	A

Features

- OptiMOS™ - power MOSFET for automotive applications
- Half-Bridge - N-channel - Enhancement mode - Logic Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TDSON-8-56



Type	Package	Marking
IAUC60N04S6L030H	PG-TDSON-8-56	6N04L030

Maximum ratings per channel, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS}=10\text{V}$, Chip Limitation ^{1,2)}	119	A
		$V_{GS}=10\text{V}$, DC current ³⁾	60	
		$T_a=85^\circ\text{C}$, $V_{GS}=10\text{V}$, R_{thJA} on 2s2p ^{2,4)}	22	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$, $t_p=100\mu\text{s}$	311	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=20\text{A}$, $R_{g,min}=25\Omega$	100	mJ
Avalanche current, single pulse	I_{AS}	$R_{g,min}=25\Omega$	20	A
Gate source voltage	V_{GS}	-	± 16	V
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	75	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	2.0	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	-	-	34	-	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=25\mu A$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=30A$	-	3.1	4.2	m Ω
		$V_{GS}=10V, I_D=30A$	-	2.3	3.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	1637	2128	pF
Output capacitance	C_{oss}		-	458	596	
Reverse transfer capacitance	C_{rss}		-	29	44	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=60A, R_G=3.5\Omega$	-	3	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32V, I_D=60A,$ $V_{GS}=0 \text{ to } 10V$	-	5.0	6.6	nC
Gate to drain charge	Q_{gd}		-	5.2	7.9	
Gate charge total	Q_g		-	27	35	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	60	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25^\circ C, t_p=100\mu s$	-	-	311	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=30A,$ $T_J=25^\circ C$	-	0.85	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	30	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	18	-	nC

¹⁾ Practically the current is limited by overall system design including customer specific PCB.

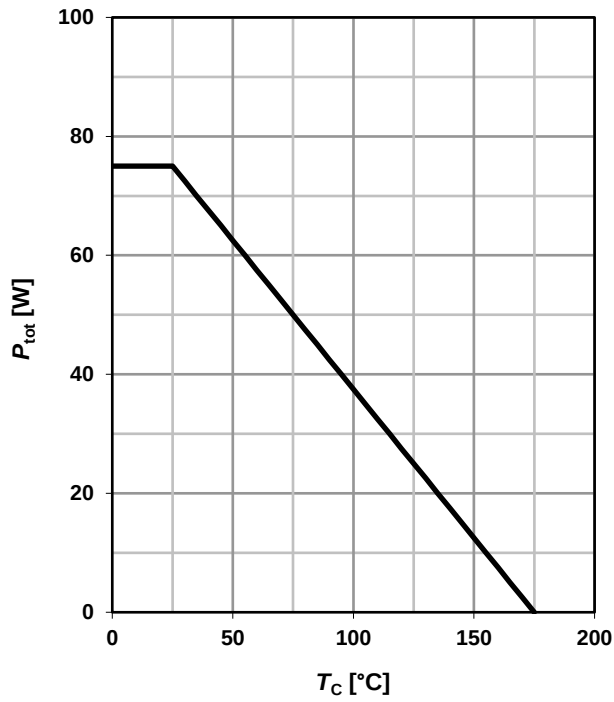
²⁾ The parameter is not subject to production test - specified by design.

³⁾ The product can operate at specified current based on best practice to minimize electromigration at the solder joint. For rare events and inrush currents the value may be exceeded.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

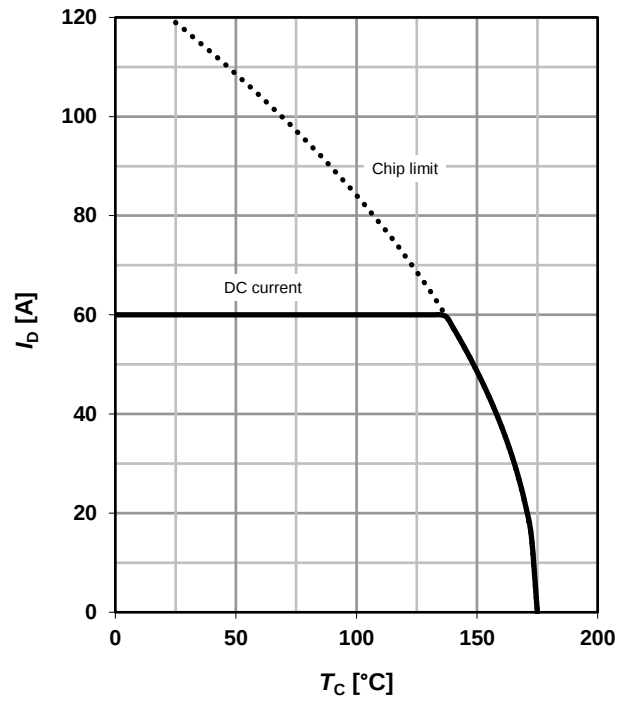
1 Power dissipation

$$P_{\text{tot}} = f(T_{\text{C}}); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

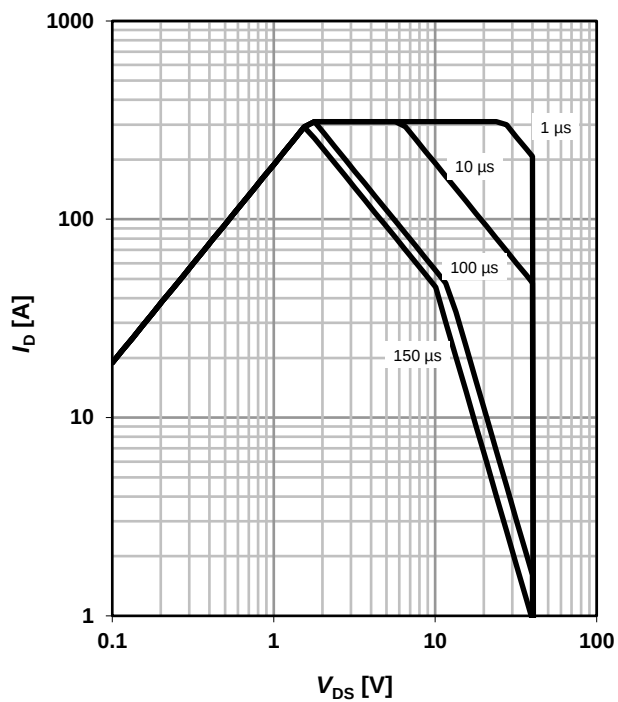
$$I_{\text{D}} = f(T_{\text{C}}); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_{\text{D}} = f(V_{\text{DS}}); T_{\text{C}} = 25^{\circ}\text{C}; D = 0$$

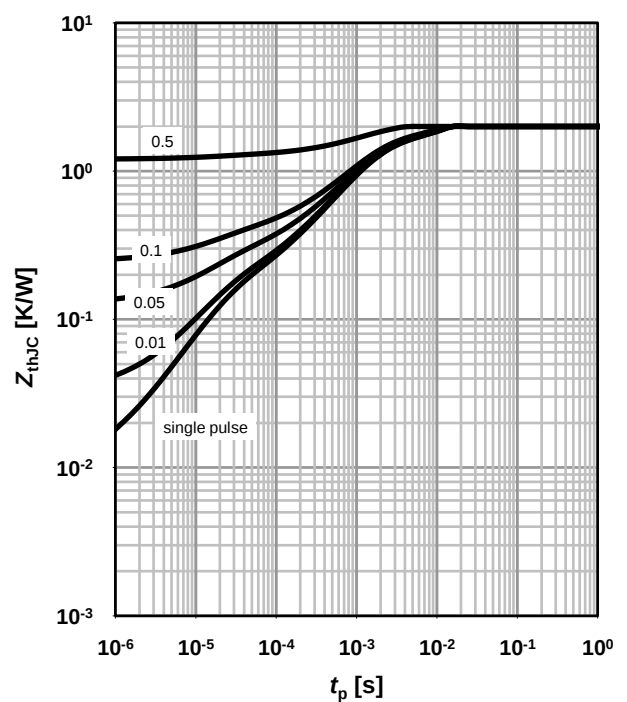
parameter: t_{p}



4 Max. transient thermal impedance

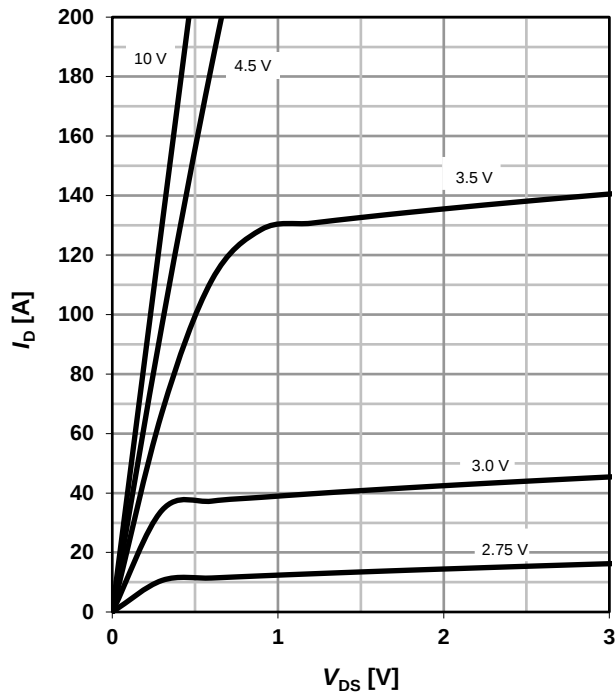
$$Z_{\text{thJC}} = f(t_{\text{p}})$$

parameter: $D = t_{\text{p}}/T$



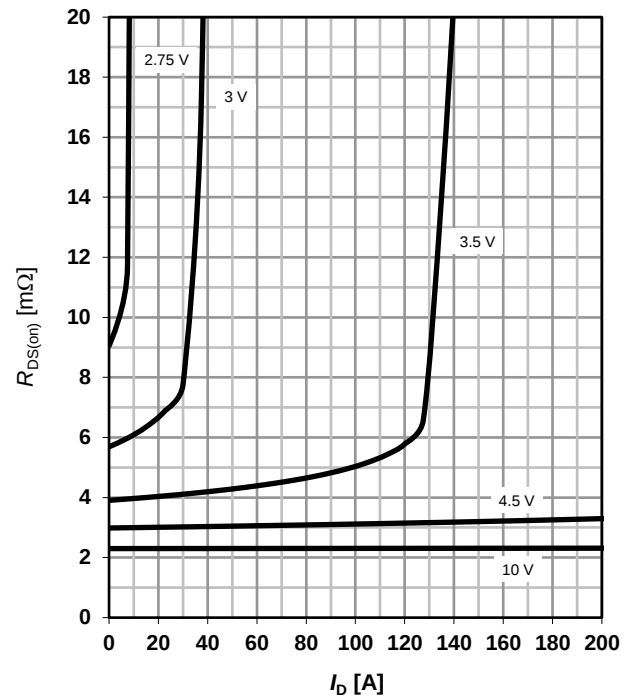
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25\text{ °C}$

parameter: V_{GS}


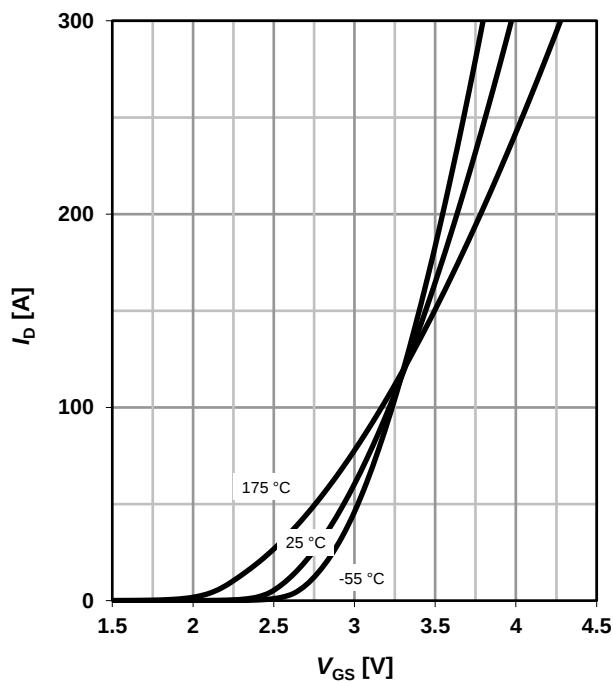
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

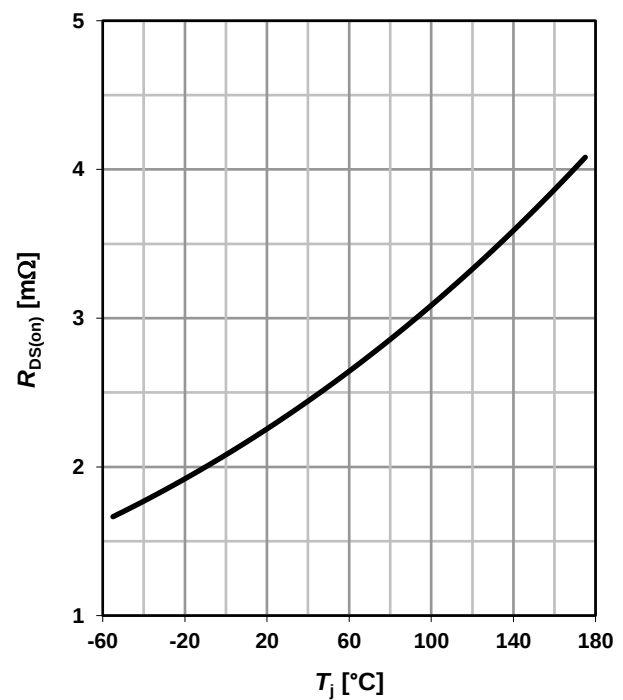
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


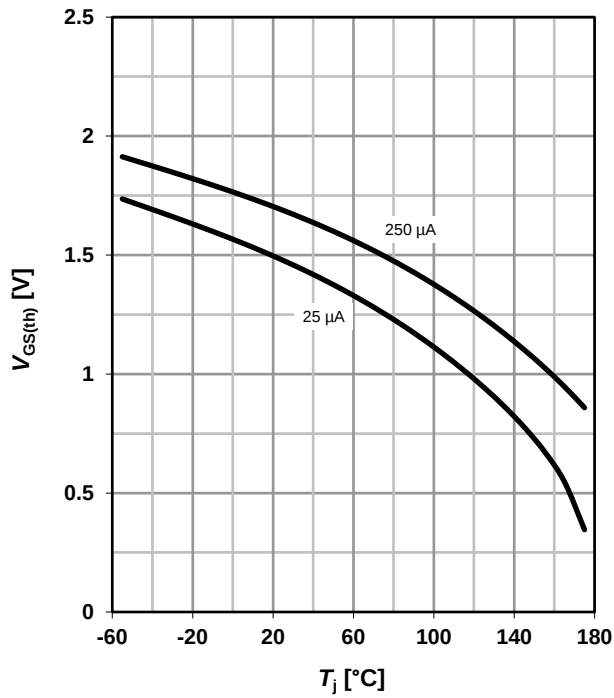
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 30\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

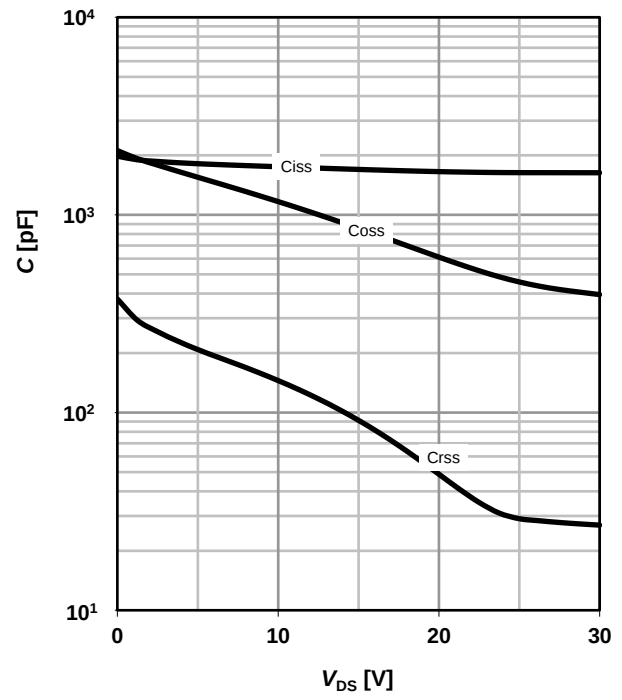
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

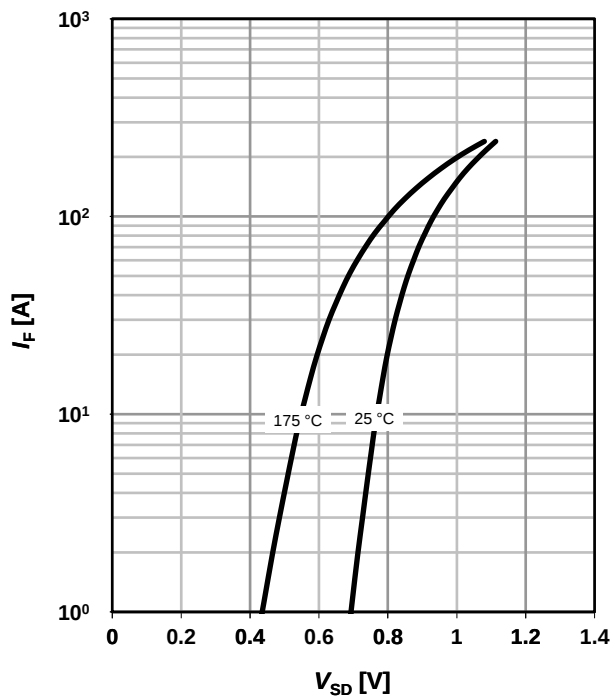
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

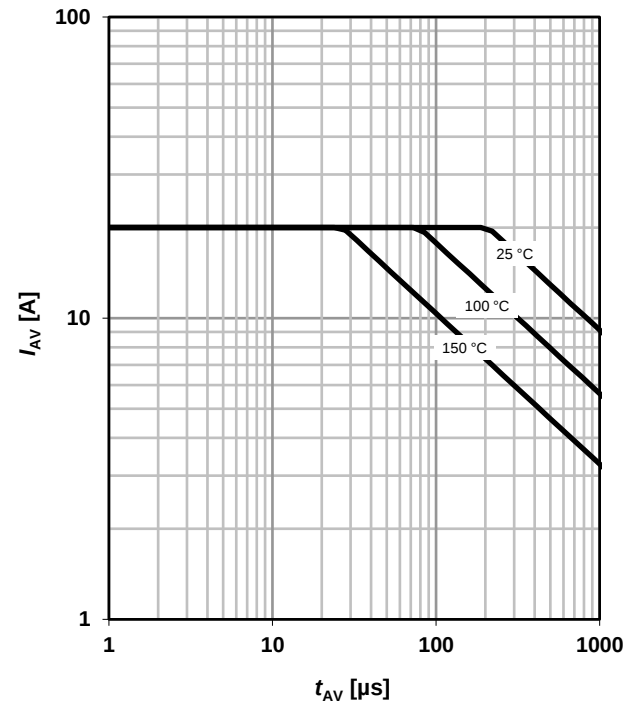
parameter: T_j



12 Avalanche characteristics

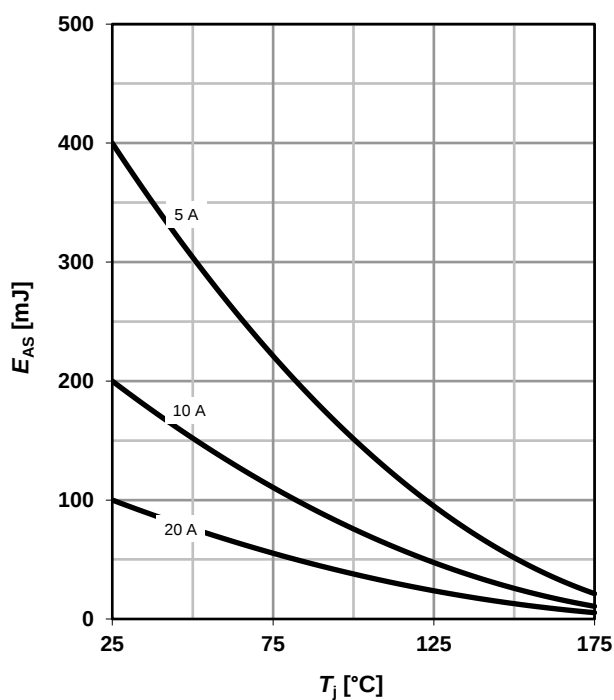
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



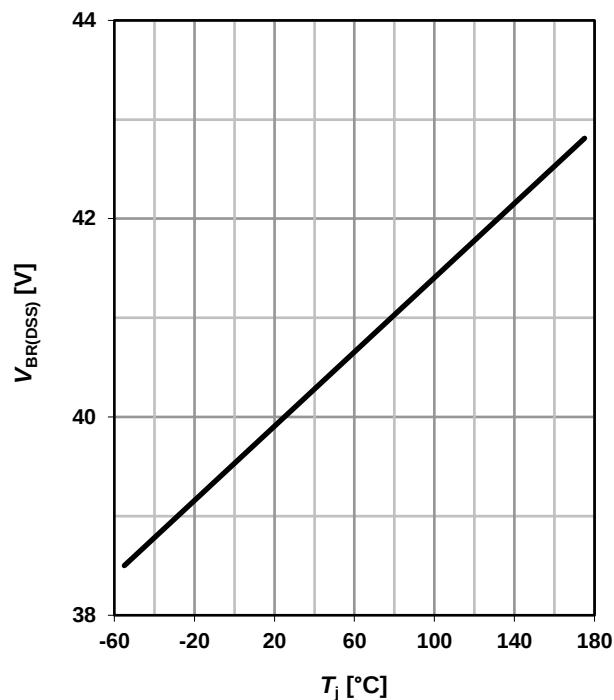
13 Avalanche energy

$$E_{AS} = f(T_j)$$



14 Drain-source breakdown voltage

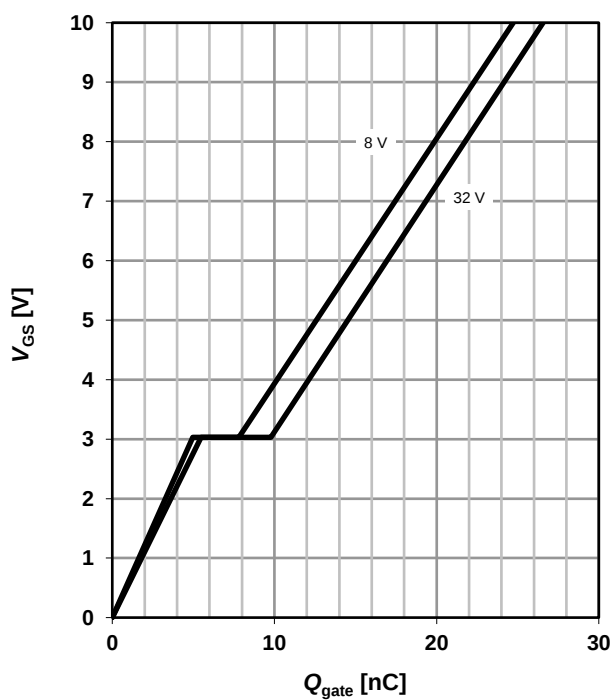
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



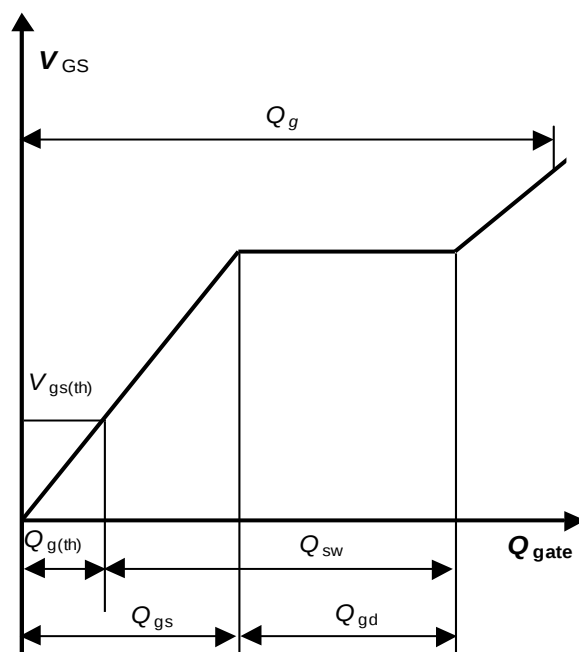
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 60 \text{ A pulsed}$$

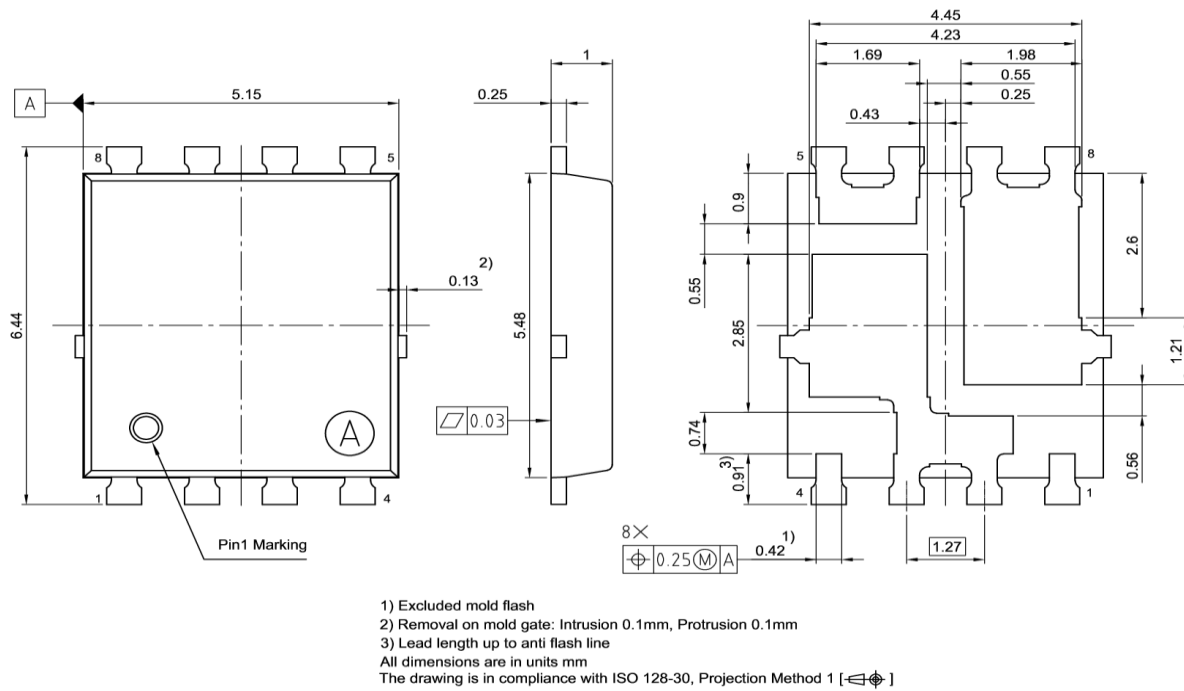
parameter: V_{DD}



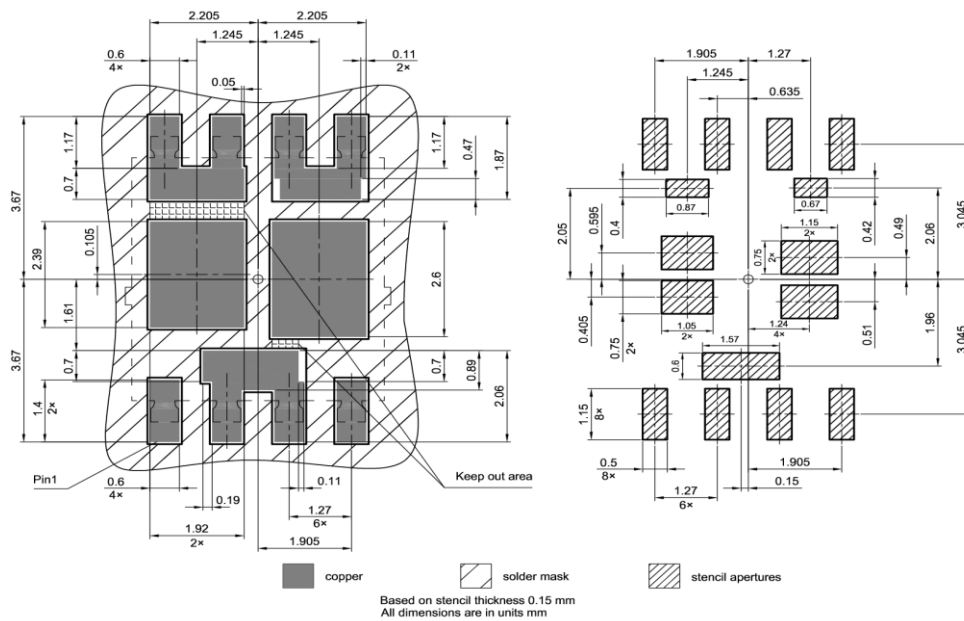
16 Gate charge waveforms



PG-TDSON-8: Outline

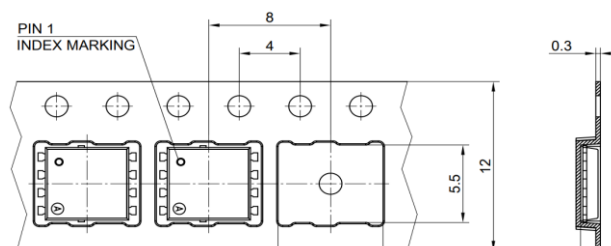


Footprint



Dimensions in mm

Packaging



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Revision History

Version	Date	Changes
Revision 1.0	18/09/2020	Final datasheet
Revision 1.1	07/02/2025	Updated Is, Is,pulse, Vsd values, plot 11, plot 9 labelling, plot 15 testing condition.