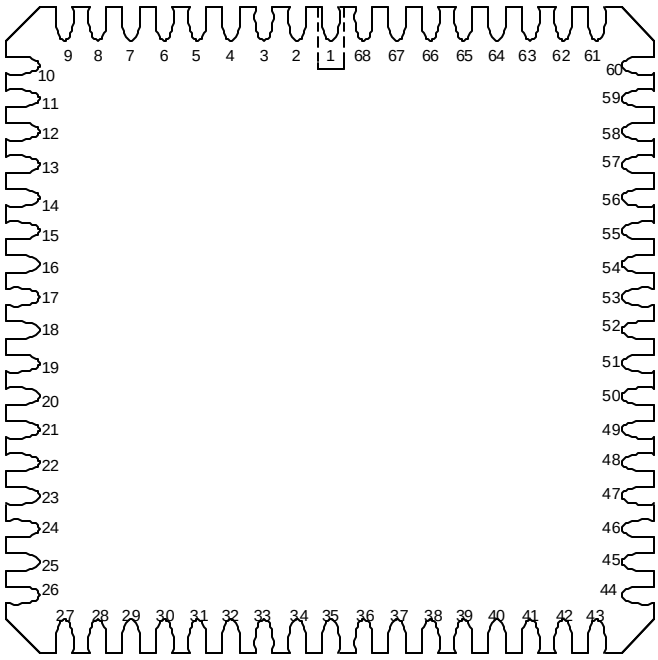
FEATURES

- **Histogram and Hough Transform Calculation**
- **Four 512 X 9 Look-up Tables Provided to Perform User-defined Point-wise Transformations**
- **Real-time Histogram Equalization**
- **High Data Rates**
- **512 X 24 Accumulation RAM**
- **Pixel Location Function**

The IA64250 is a "plug-and-play" drop-in replacement for the original LSI® L64250. This replacement IC has been developed using innovASIC's MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA64250 including functional and I/O descriptions, electrical characteristics, and applicable timing.

Package Pinout for 68 PLCC PACKAGE:



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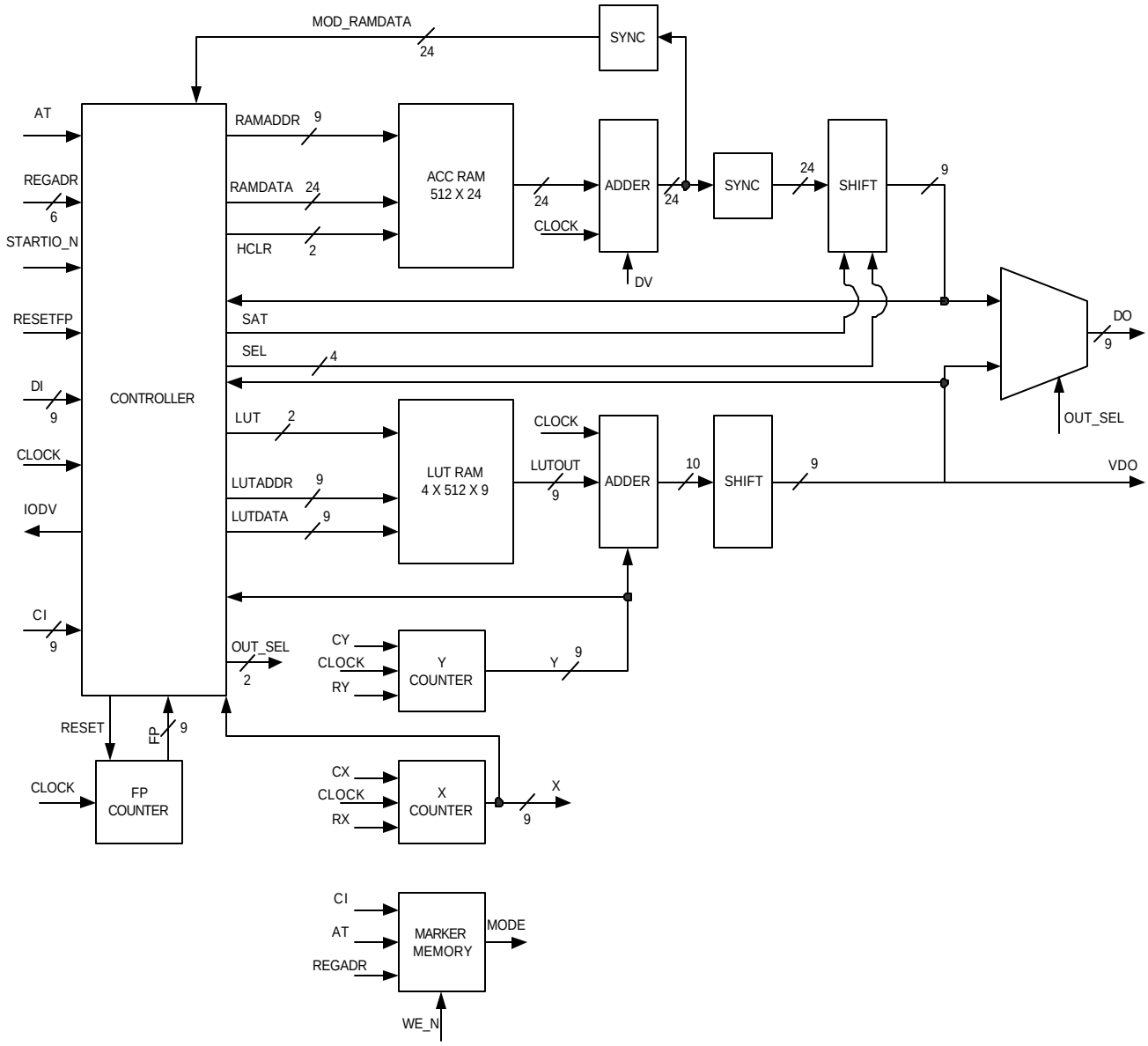
PIN DESIGNATOR:

PIN NAME	GRID #	PIN NAME	GRID #	PIN NAME	GRID #	PIN NAME	GRID #
GND	1	GND	18	GND	35	DO.5	52
CI.5	2	VDD	19	STARTIO	36	DO.6	53
CI.4	3	VDO.6	20	VDD	37	DO.7	54
CI.3	4	VDO.5	21	CLK2	38	DO.8	55
CI.2	5	VDO.4	22	PO	39	DI.0	56
CI.1	6	VDO.3	23	IODV	40	DI.1	57
CI.0	7	VDO.2	24	DV	41	DI.2	58
WE	8	VDO.1	25	AT	42	DI.3	59
REGADR.5	9	VDO.0	26	GND	43	DI.4	60
VDD	10	VDD	27	VDD	44	VDD	61
REGADR.4	11	RESET FP	28	DO.0	45	DI.5	62
REGADR.3	12	GND	29	DO.1	46	DI.6	63
REGADR.2	13	RY	30	DO.2	47	DI.7	64
REGADR.1	14	CY	31	DO.3	48	DI.8	65
REGADR.0	15	RX	32	DO.4	49	CI.8	66
VDO.8	16	CX	33	VDD	50	CI.7	67
VDO.7	17	CLK1	34	GND	51	CI.6	68

BLOCK DIAGRAM:

Figure 1



Description

The IA64250 performs three separate tasks, histogram generation, modified Hough transforms, and pixel location. There are three modes of operation for the IA64250: computation, I/O, and initialization.

The controller block in the block diagram decodes the instructions and contains the mode registers. After decoding the mode, the controller generates all of the control signals to the rest of the part. These control signals include the addresses and input data for the LUT and ACC RAMs, the select lines for both the output mux and the shifter, and the reset for the FP counter. This block also controls the clearing of the ACC RAM.

The ACC RAM stores the video data that is to be output during the I/O mode. This data can be modified, depending on mode, by several methods prior to being output. These methods are described in the computation mode section.

The LUT RAM can store up to four different data modifying functions. These functions are used to modify the video data coming in and access the appropriate data in the ACC RAM through the ACC RAM address. This data is then sent out on the DO output.

During the initialization mode, the functions to be performed are defined. This is accomplished by setting the values in the mode registers contained in the controller block.

During the computation mode, the histogram, Hough transform, or pixel location data is computed. Data equalization also occurs during this mode if desired. The controller block controls the adders and shifters during this mode to ensure correct data manipulation. This is accomplished through the data stored in the mode registers as well as the DV input. The controller block also generates the addresses to both the RAMs.

The I/O mode allows data to be transferred to the Accumulation RAM (ACC RAM) and/or to and from the Look Up Table RAM (LUT RAM). The user can also update the marker memory during the I/O mode. The marker memory is used to quickly find points of interest on the histogram, Hough transform, or accumulated histogram curves. Up to seven points of interest can be specified on the grey level axis or parameter axis. The corresponding value on the accumulation axis will then be available. The reverse is also true, where the user can specify accumulation values of interest and obtain the corresponding grey values. The memory map located in the I/O mode description shows the configuration of the data stored in the memory. The transfer of data from an external source to either of the RAMs is done through either the CI or DI input bus. The controller block takes in the data and passes it along to the appropriate RAM. The controller block also supplies the RAM with the address and control signals needed to write the data. During a data transfer from one RAM to the other, the controller block performs a similar task, overseeing the transfer and supplying the necessary control signals and address.

I/O SIGNAL DESCRIPTION:

The diagram below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provide.

I/O Characteristics:

IODV	O	When HIGH, ACC RAM or LUT RAM data on the DO bus is valid.
VDO.0 - VDO.8	O	LUT RAM data output (uses CLK1).
CIO.0 - CIO.8	I	Control register and LUT input data bus.
WE	I	Used to strobe data into mode latches when LOW.
REGADR0 - REGADR5	I	Selects mode latch, marker or maximum registers.
AT	I	Selects marker and maximum registers when HIGH or mode latches when LOW. AT must be LOW to access the LUT or ACC RAMs via the DO bus.
CLK1	I	Pixel clock active at rising edge.
CLK2	I	User I/O clock (may be connected to CLK1)
STARTIO	I	Initiates RAM I/O at HIGH to LOW transition.
CX,CY	I	Used to increment X or Y counters when HIGH.
RX,RY	I	Resets X or Y counters(overrides CX, CY) when HIGH.
RESET FP	I	Resets FP counter when HIGH.
PO	O	Test pin should be left unconnected.

INITIALIZATION MODE:

Initialization defines the operation of the IA64250. The mode and marker memories store 66 nine-bit words that define the operation of the part and contain marker information. The REGADR input is used to select the proper register. Data is written over the CI bus and read on the DO bus. The AT pin controls whether data is a mode word or a marker. When AT is low, the data written is mode information, which is stored in the mode registers contained in the controller block. When AT is high, the data is a marker, and is stored in the marker memory. To prevent erroneous operation STARTIOn should be high, and IODV and DV should be low during initialization.

Mode Register Table:

AT	REGADR	R/W	BIT LOCATION								
		W	ci0	ci1	ci2	ci3	ci4	ci5	ci6	ci7	ci8
		R	do0	do1	do2	do3	do4	do5	do6	do7	do8
0	0	W	sel0	sel1	sel2	sel3	lut0	lut1	sh1	sat	TESTn
0	1	W	fn0	fn1	Eq	io0	io1	hclr0	hclr1	func	pdwn

Marker Memory Table:

AT	REGADR	R/W	CONTENTS
1	0	R	GREY LEVEL OF MAXIMUM ACC COUNT BITS 0-8
1	1	R	MAXIMUM ACC COUNT BITS 0-8
1	2	R	MAXIMUM ACC COUNT BITS 9-17
1	3	R	MAXIMUM ACC COUNT BITS 18-23*
1	16	W	TEST MODE, DO NOT ACCESS
1	17	W	TEST MODE, DO NOT ACCESS
1	18	W	TEST MODE, DO NOT ACCESS
1	19	W	TEST MODE, DO NOT ACCESS
1	32	R/W	R/W MARKER 0 GREY LEVEL BITS 0-8
1	33	R/W	R/W MARKER 0 ACC COUNT BITS 0-8
1	34	R/W	R/W MARKER 0 ACC COUNT BITS 9-17
1	35	R/W	R/W MARKER 0 ACC COUNT BITS 18-23*
1	36	R/W	R/W MARKER 1 GREY LEVEL BITS 0-8
1	37	R/W	R/W MARKER 1 ACC COUNT BITS 0-8
1	38	R/W	R/W MARKER 1 ACC COUNT BITS 9-17
1	39	R/W	R/W MARKER 1 ACC COUNT BITS 18-23*
			.
			.
			.
1	56	R/W	R/W MARKER 6 GREY LEVEL BITS 0-8
1	57	R/W	R/W MARKER 6 ACC COUNT BITS 0-8
1	58	R/W	R/W MARKER 6 ACC COUNT BITS 9-17
1	59	R/W	R/W MARKER 6 ACC COUNT BITS 18-23*

*ACC COUNT BIT 18-23 APPEARS ON BIT LOCATION 0-5 RESPECTIVELY

Mode Definition:

The controller block decodes the instructions brought in to the IA64250 on the CI bus, with the REGADR input determining which instructions are being read in. The Mode Memory table shows the configuration of the CI bus encoded instruction depending on the state of REGADR. A brief description of the instruction bits follows:

sel(3:0) selects the nine bits of the ACC RAM to be transferred to the DO output or to the LUT RAM.

sel0	sel1	sel2	sel3	Sel	window
0	0	0	0	0	select bits 0-8
1	0	0	0	1	select bits 1-9
0	1	0	0	2	select bits 2-10
1	1	0	0	3	select bits 3-11
0	0	1	0	4	select bits 4-12
…					
1	1	1	1	15	select bits 15-23

lut(1:0) defines one of the four 512 X 9 LUTs as active.

sh1 When low, the least significant nine bits of the 10 bit LUT and Y count sum will address the ACC RAM. When high, the nine most significant bits of the sum will be used.

sat When high, the nine bits selected from the 24 bit ACC RAM output will be forced to 511 (111111111) if the 24 bit ACC RAM output contains a 1 in the range of bits from the sel + 9 to 23. Otherwise the nine bits selected from the ACC RAM output will be unchanged.

test Used for testing when low. Should be high for normal operation.

fn(1:0) Determines the operation performed during the computational mode.

fn0	fn1	FUNCTION
0	0	modified Hough transform computation
0	1	undefined
1	0	histogram computation
1	1	pixel location

eq When high, causes the output of the ACC RAM to be accumulated as it is read. This is commonly used to compute the histogram equalization transfer function. When low, the ACC RAM output is not modified.

io(1:0) Control the operations of the ACC and LUT RAMs during I/O mode (when the STARTIOn signal has been asserted).

io0	io1	FUNCTION
0	0	transfer data from the ACC RAM to the LUT RAM
0	1	read the ACC RAM
1	0	read the LUT RAM
1	1	write the LUT RAM

hclr(1:0) Control the clearing of the ACC RAM during I/O mode

hclr0	hclr1	FUNCTION
0	0	ACC RAM cleared when either the ACC RAM or LUT RAM is accessed
0	1	Undefined
1	0	ACC RAM cleared only when the ACC RAM is accessed
1	1	ACC RAM not cleared during an i/o operation

func Determines the function performed by the marker processor. When high, each marker circuit within the processor will locate an accumulated count from the ACC RAM corresponding to the previously given grey value. When low, each marker will locate the grey value corresponding to a previously given accumulation count from the ACC RAM.

pdwn When high, the ACC and LUT RAMs are placed in an inactive mode. Should be low for normal operation.

MEMORY CONFIGURATIONS:

The following memory maps specify the configuration of the ACC RAM and the LUT RAM in the various computational modes.

ACC RAM Histogram Mode:

Grey Level	Memory Contents
0	Count for Grey Value 0
1	Count for Grey Value 1
. . . .	. . . .
511	Count for Grey Value 511

ACC RAM Modified Hough Transform Mode:

Hough Transform Parameter Axis	Memory Contents
0	Projection Along r = 0
1	Projection Along r = 1
. . . .	. . . .
511	Projection Along r = 511

ACC RAM Find Pixel Mode:

Address	Memory Contents		
	0-8	9-17	18-23
0	X0	Y0	FLAG
1	X1	Y1	FLAG
. . . .			
N	XN	YN	FLAG
N + 1	0	0	0
. . . .			
511	0	0	0

LUT RAM Histogram Computation:

Histogram Transfer Function	Memory Contents
0	f(0)
1	f(1)
. . . .	. . . .
511	f(511)

LUT RAM Hough Transform Mode (45 < f £ 90):

Address	Memory Contents
0	0*cotϕ
1	1*cotϕ
. . . .	. . . .
511	511*cotϕ

LUT RAM Find Pixel Mode:

Address	Memory Contents		
	0-5	6-7	8
0	Flag for Grey Value 0	t0	Not Used
1	Flag for Grey Value 1	t1	
. . . .	. . . .	Tag Bit	
511	Flag for Grey Value 511	t511	

COMPUTATION MODE:

Histogram Computation:

During histogram computation, the ACC RAM and LUT RAM form the active elements of the data path. The ACC RAM is addressed by the controller block. The ACC RAM address is the DI input signal. The data addressed by the DI signal is incremented if the DV input signal is high, otherwise the data is left unchanged. The LUT is not used in the computation of the histogram and can concurrently modify the image by a user-defined transfer function. The DI signal addresses the LUT and the LUT data appears on the VDO output pins two clock cycles later.

Histogram equalization can be performed in real time. The histogram is stored in the ACC RAM. The equalization transfer function must be computed and transferred into the LUT RAM. Then during the next frame as a new histogram is being computed, data will also be equalized in real time and passed to the VDO output pins.

Hough Transform Computation:

During Hough Transform computation, the ACC RAM stores the projection image, and the LUT RAM is loaded with the function listed in the Modified Hough Transform Parameterization Table.

Case	F	r(X,Y,F)	LUT[i]	CX,RX Controls	CY,RY Controls
1a	$0 \le \Phi < 45$	$X \tan\Phi + Y$	$i\tan\Phi$	X	Y
1b	$45 \le \Phi < 90$	$Y \cot\Phi + X$	$i\cot\Phi$	Y	X
1c	$90 \le \Phi < 135$	$(YMAX - Y) \cot (180 - \Phi) + X$	$(YMAX - I) \cot (180 - \Phi)$	Y	X
1d	$135 \le \Phi < 180$	$(XMAX - X) \tan (180 - \Phi) + Y$	$(XMAX - I) \tan (180 - \Phi)$	X	Y

During initialization, the LUT is loaded with the appropriate transfer function to compute either f(x) or f(y). Once the LUT is loaded, the X and Y counters are used to generate the proper memory addresses. The X counter is incremented at each valid pixel and reset at the beginning of each line. The Y counter is incremented at the beginning of each line and reset at the beginning of each frame. The control signals for these two counters are generated in the controller block. As each pixel location along a line is addressed, the grey value at that point is added to the partial sum in the memory location.

Intensity Averaging:

Another computational mode is possible by generating ACC RAM addresses differently. An example of this is to compute the average intensity of an image as a function of position. Consider a 512 X 512 pixel image divided into 256 blocks (16 X 16) of 32 X 32 pixels each. To compute the average intensity, the Y counter would be incremented every 32 pixels and reset at the beginning of each line. The X counter would be incremented every 32 lines and reset at the beginning of a frame. The proper addresses will be generated by multiplying the X counter output by 16 (this is done via the LUT). After processing, the first 256 locations of the ACC RAM will hold the accumulated intensity in each 32 X 32 region. Setting sel(3:0) = 10 will give the average intensity in each region.

Pixel Location:

Pixel location is used to determine the X and Y coordinates of up to 64 specific pixels or group of pixels in an image. When performing pixel location, the user first loads one of the LUTs with a table indicating which pixels are of interest. Each pixel in the table is assigned a 6 bit flag that allows the user to distinguish groups of pixels.

Each time an interesting pixel (as specified in the LUT) is found, the X, Y, and flag values are stored in the ACC RAM at the address given by the FP counter. The FP counter is then incremented. Note that only 512 values can be stored at any instance. In the event that more values are stored, the first RAM locations will be overwritten.

Pixel location uses the LUT and the X and Y counters to store a six-bit code and location information about pixels of interest. The X and Y counters hold the coordinates of the grey value on the DI pins and are controlled in the same manner described in the Hough transform section. DI addresses the LUT producing a one-bit tag and a six bit flag associated with the grey value. If the tag bit is high and DV is high the six bit flag and X, Y

coordinates are stored in the ACC RAM. Storage space is assigned sequentially as defined by the FP counter.

I/O Mode:

Once a computation has taken place, the user reads data from the LUT or the ACC RAM. These operations typically take place during a vertical retrace or some other period when the processor is not busy and AT is low. This mode is also to load the LUT with the desired transfer function. Generally, these operations are controlled by CLK2 so that data may be read or written at a different rate than the pixel clock. If the ACC RAM is accessed, the marker values will be updated.

The internal signals hclr(1:0) control whether or not the ACC RAM is cleared during I/O operations. These values are stored in the mode registers of the controller block during the initialization mode. If both hclr0 and hclr1 are high then the ACC RAM will not be cleared during any I/O operation. If hclr0 is high and hclr1 is low, then each ACC RAM location will be cleared after it is read. If both hclr0 and hclr1 are low then each ACC RAM location is cleared when either the ACC RAM location or the corresponding LUT RAM location is accessed.

Read/Transfer ACC RAM:

Once the histogram has been computed and stored in the ACC RAM, the user asserts STARTIOn low to initiate reading of the data. One data value is read out of the ACC RAM during each clock cycle of CLK2 starting with address 0. The address counter for the ACC RAM is contained in the controller block. If STARTIO remains low, all 512 data values will be read in sequential address order and the processor will return to pixel processing mode after 512 clock cycles. If STARTIOn is returned high, the I/O mode halts and the user can return to pixel processing operations. When the output flag IODV is high, the processor has placed valid data from the LUT or ACC RAMs onto the I/O bus.

The user controls the destination of the ACC RAM data via the io(1:0) bits in the mode registers located in the control memory. Code 01 signifies that histogram data will be placed on the DO output bus, while code 00 will transfer data from the ACC RAM to the LUT RAM.

In both cases the user can modify the histogram data. By setting the internal EQ control bit high, an accumulated histogram will be output. The shifter allows the user to determine which nine bits of the 24 bit ACC RAM output will be directed to the DO bus and LUT RAM. The shifter control data is stored in the mode registers. The control signals for the shifter are generated in the controller block. Additional control over the output format can be obtained via the SAT pin in the control memory. When SAT is high, the resultant nine bit shifted output will be forced to 511 (111111111) if overflow occurs in the shifter.

Marker Circuitry:

When ACC RAM is accessed, the marker circuitry in the marker memory is updated. The user can specify up to seven values of grey level and the associated count will be stored in the mode memory. Setting func = 1 in the control memory register will accomplish this. By setting func = 0, the user can specify a particular count and the marker memory will be updated with the last grey value whose count is equal to (or just exceeds) the count of interest.

The maximum count, and the grey value which it occurred at, are also updated during each I/O cycle and stored in mode memory locations 0-3.

If the accumulated histogram is being computed, i.e. the EQ bit in the mode register is set, then the maximum count register will be equal to the number of pixels scanned, and the grey value will be the maximum grey level occurring in the image.

Reading and Writing the LUT:

Data input to and output from the LUT RAM is also controlled by CLK2 and STARTIOn. On the falling edge of STARTIOn, the I/O cycle is initiated with the LUT RAM addresses being read or written sequentially with each cycle of CLK2. This process is controlled by the address counter in the controller block.

LUT read/write operations are defined by the io0-1 bits in the control memory. Code 10 is used to read the LUT RAM. Data will be read sequentially and output on the DO bus. To write the LUT RAM, code 11 is used in the control memory. Input from the CI bus is stored in successive addresses with each cycle of CLK2.

The LUT RAM can also be addressed from the DI bus. A typical application would be histogram equalization. The LUT would contain the equalized transfer function generated by transferring ACC RAM data to the LUT with EQ high. Setting the FN0-FN1 bits for histogram computation configures data from the DI bus to address both the ACC RAM and the LUT. Equalized data is then output on the VDO bus. Histogram computation is taking place concurrently. In this case CLK2 should be connected to CLK1 to achieve an equalization rate equal to the pixel rate.

I/O SEQUENCES:

Read ACC, Read LUT, Transfer ACC to LUT

I/O operations can be divided into two groups: those that end before all 512 elements of the ACC or LUT RAM have been accessed (short cycle) and those that end after all 512 elements have been accessed (long cycle). All I/O cycles are initiated by a high to low transition on the STARTIOn input signal. AT must be low in each case.

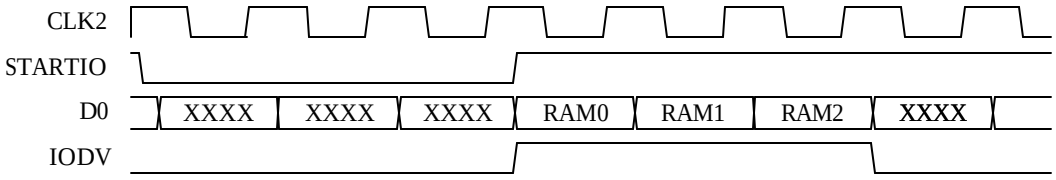
The short cycle is terminated when STARTIOn is returned high before all elements of the RAM have been read. The first data value appears on the DO pins three CLK2 cycles after STARTIOn goes low. The IODV flag also goes high after three cycles, indicating that the

data is valid. After the desired number of memory elements have been read, the user returns STARTIOn high. The I/O mode completes three cycles later and IODV returns low to indicate the end of the I/O operation. As soon as IODV returns low, the processor returns to the pixel processing mode specified by the mode register.

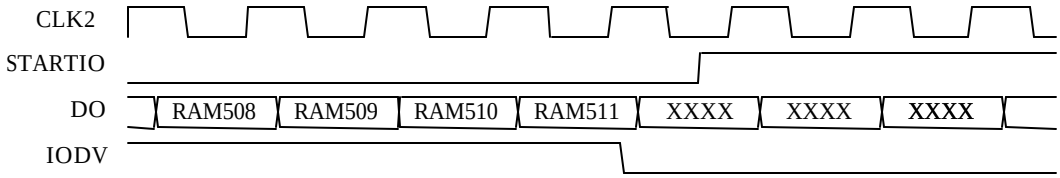
The long cycle is terminated without user intervention after all elements of the ACC or LUT RAMs have been accessed. Again, valid data appears on the DO pins three CLK2 cycles after STARTIOn goes low. In this case, IODV is high for 512 CLK2 cycles and goes low after the last RAM element has been read. After IODV returns low, STARTIOn can remain low or be raised high at any time without affecting the operation of the IA64250.

READING ACC/LUT RAM OR TRANSFERING ACC TO LUT:

Short I/O Cycle:



End of Long I/O Cycle:



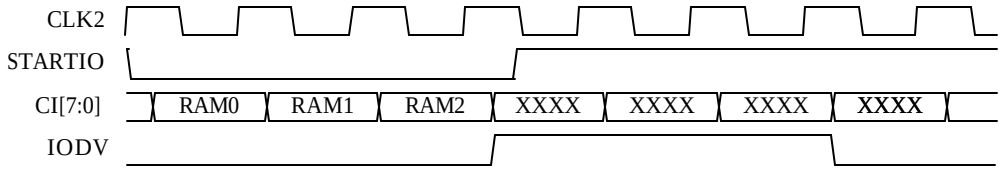
WRITE LUT

The writing of data into the LUT RAM is similar to the operations described above, except that the data to write into the RAM is placed on the CI bus when STARTIOn is low. However, as described above, the processor will not return to the pixel processing mode until IODV returns low.

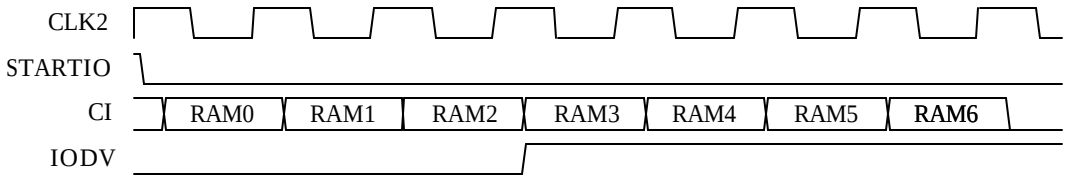
The net result of this is that the IA64250 enters the I/O mode as soon as the STARTIOn pin is pulled low and does not return to the pixel processing mode until IODV returns low. The I/O mode will last N + 3 CLK2 cycles, where N is the number of RAM elements written.

WRITING LUT RAM:

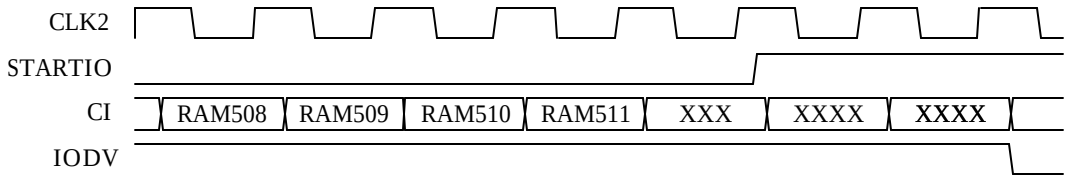
Short I/O Cycle:



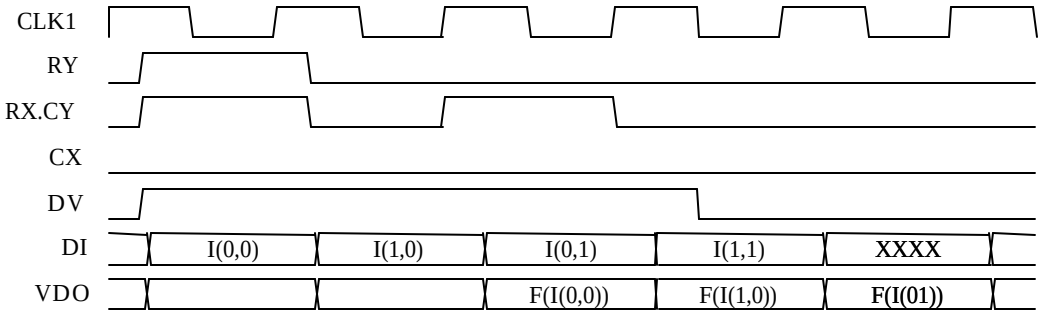
Start of Long I/O Cycle:



End of Long I/O Cycle:



PIXEL PROCESSING
(SMALL 2 x 2 IMAGE):



AC/DC Parameters:

Military (TA = -55 to 125 C, VDD = 4.5 to 5.5V). All times in ns.

SYMBOL	PARAMETER	MIN	MAX
tCYCLE	Minimum clock cycle time	60	
tPWH	Minimum clock pulse width HIGH	28	
tPWL	Minmum clock pulse width LOW	25	
tDIS	Input data setup time	25	0.38
tDIH	Input data hold time	7	2.28
tOD	Output delay		17.78
tWC	Minimum WE cycle time	180	
tPWW	Minimum WE pulse width LOW	75	
tAS	AT Address setup time	75	
tAH	AT Address hold time	75	
tCS	Coefficient setup time	75	
tCH	Coefficient hold time	75	
tADO	Output delay from address valid		24.53
tWD	Output Delay from WE		24.53

DC CHARACTERISTICS:

Specified at VDD = 5V over the specified temperature and voltage ranges[1].

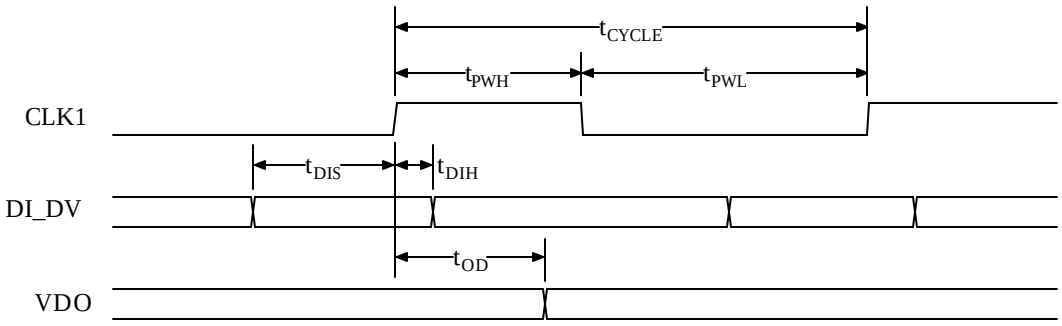
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIL	Low level input voltage				0.8	V
VIH	High level input voltage Military temperature range		2.25			V
IIN	Input current	VIN = VDD	-150		200	uA
VOH	High level output voltage	IOH = -3.2 mA	2.4	4.5		V
VOL	Low level output voltage	IOL = 3.2 mA		0.2	0.4	V
IOS	Output short circuit current[2]	VDD = Max, VO = VDD VDD = Max, VO = 0V	15 -5		130 -100	mA mA
IDDQ	Quiescent supply current[3]	VIN = VDD or VSS			15	mA
IDD	Operating supply current	tCYCLE = 50ns		200		mA
CIN	Input capacitance	Any input		5		pF
COUT	Output capacitance	Any output		10		pF

Notes:

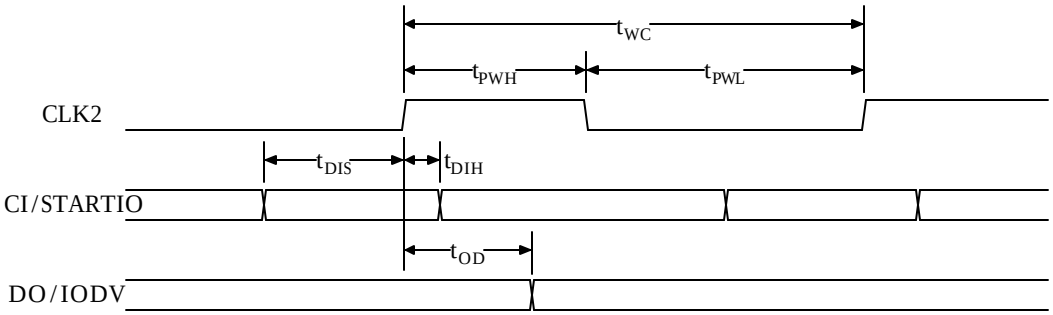
1. Military temperature range is –55 to 125 C, + / - 10% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. In power down mode.

AC Characteristics:

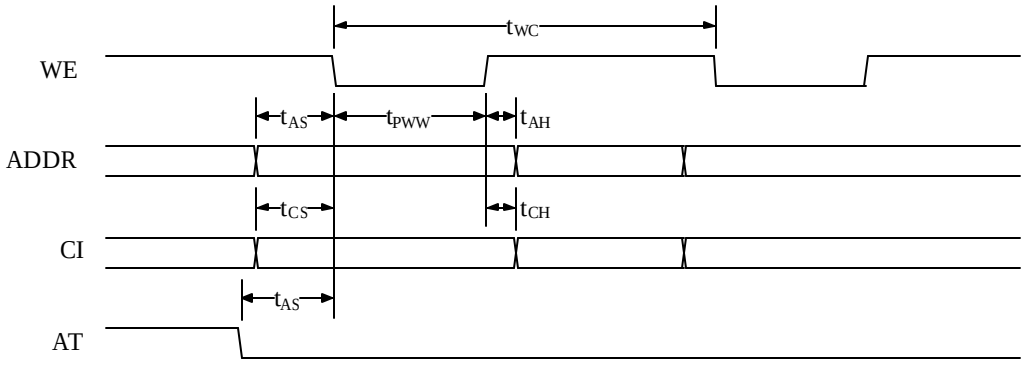
Pixel Processing Operation:



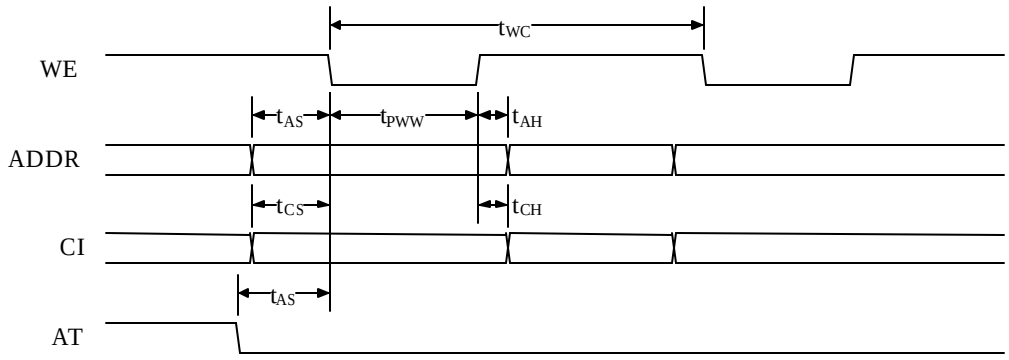
I/O Timing:



Control Memory Timing – Writing Mode Data:

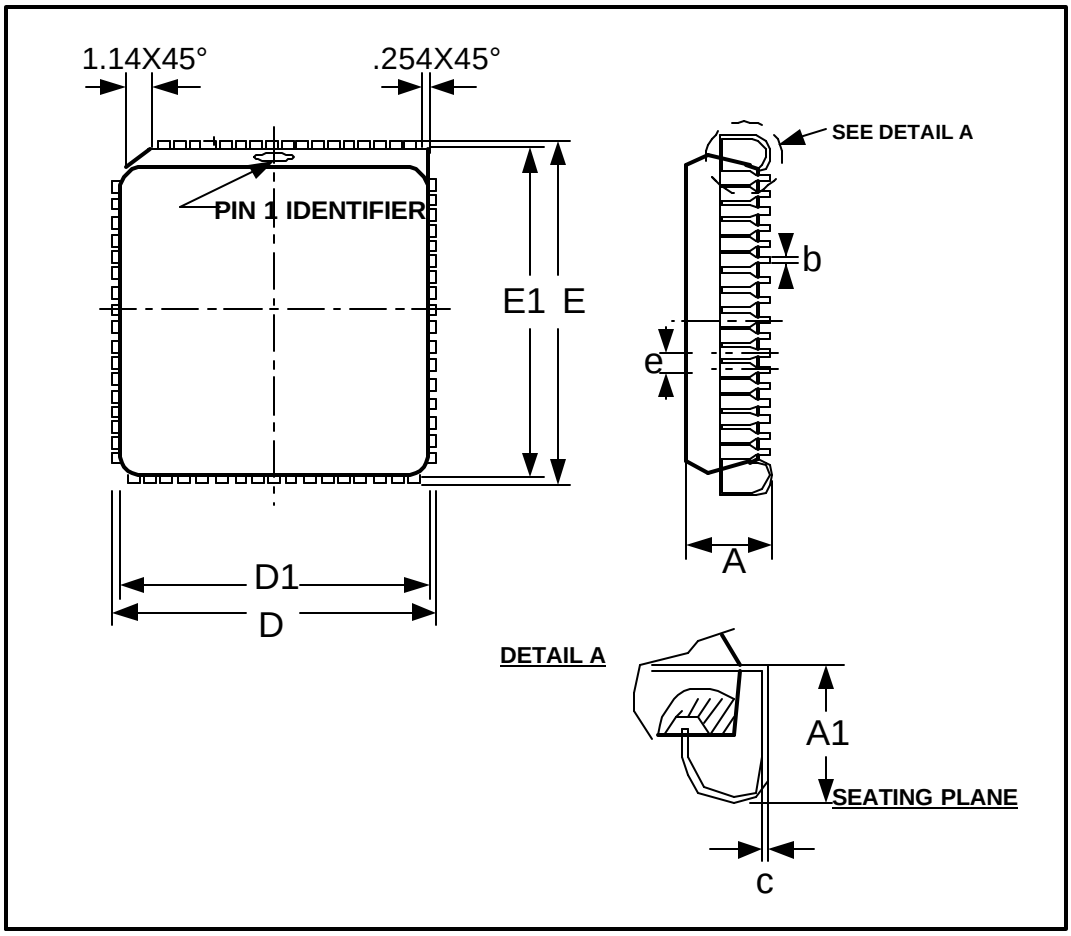


Control Memory Timing – Reading and Writing Markers:



Packaging Information

68 PLCC Package:



68 PLCC, (17X17 pins):

Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.02		5.08	0.165		0.2
A1	2.29		3.3	0.09		0.13
b	0.331		0.53	0.013		0.021
c		0.2			0.008	
D	25.02		25.27	0.985		0.995
D1	24.13		24.33	0.95		0.958
E	25.02		25.27	0.985		0.995
E1	24.13		24.33	0.95		0.958
e		1.27	BSC		0.05	

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Ordering Information:

Part Number	Temperature Grade	Package Description
IA64250-PLC68M	Military	68 lead Plastic Leaded Chip Carrier

Cross Reference to Original Manufacturer Part Numbers:

innovASIC Part Number	LSI Part Number
IA64250-PLC68M	❑ L64250JC15
	❑ L64250JC20