ILLUMINANT 北極光企業有限公司

PRODUCT SPECIFICATION FOR TFT LCM

CUSTOMER:	
MODEL NO:	I1101-6TJN0906C
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
LCM產品部 2009.09.30 Long	LCM產品部 2009.09.30 Vicky	LCM產品部 2009.09.30 Vicky

■Approval for Specifications Only

□Approval for Specifications and Sample

Note: 1. Version of Specifications : 1

2. Others: Rohs Compliment

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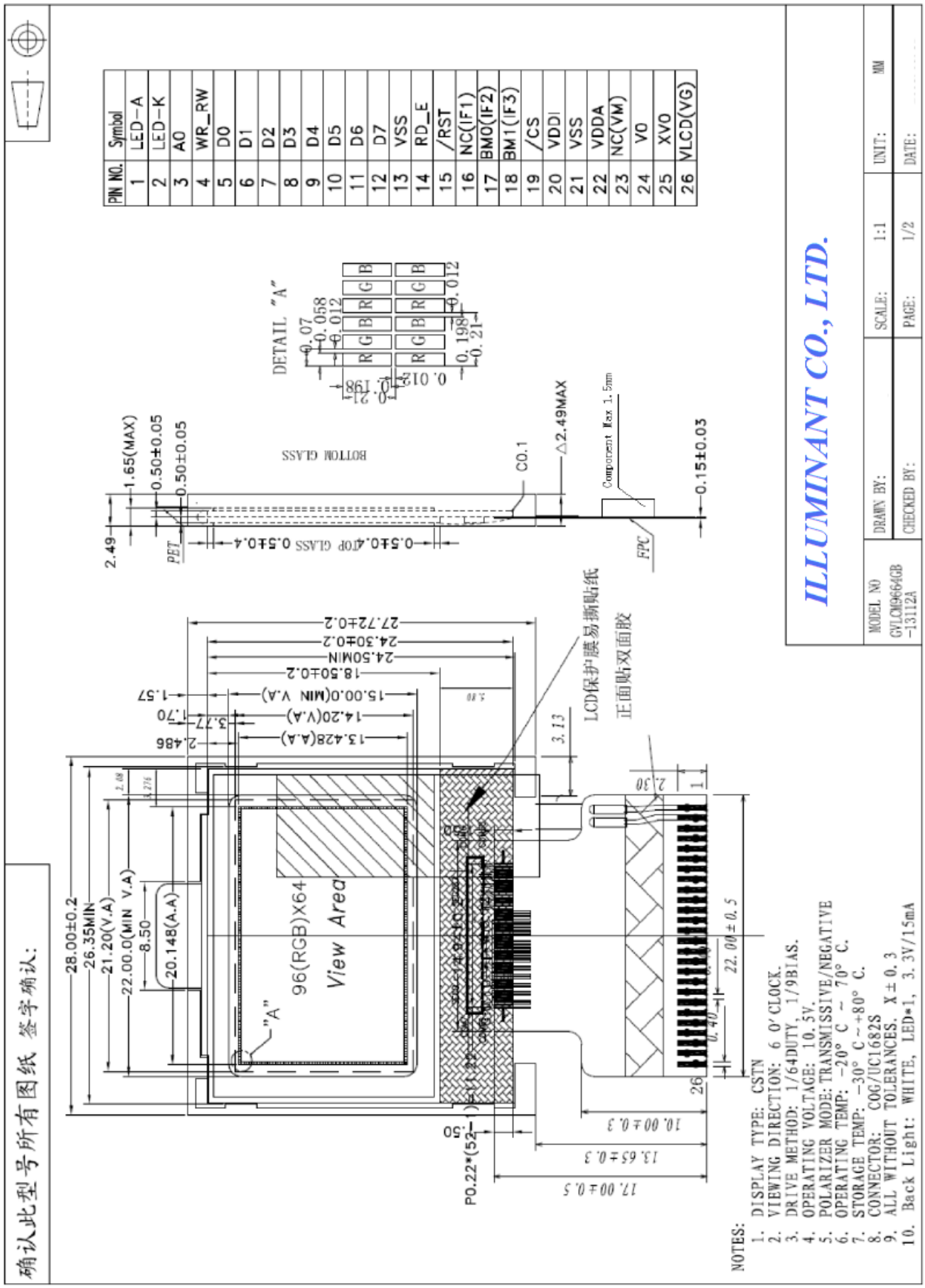
Version	Date	Contents
1	09/09/30	Initial Release

CONTENTS

1. Mechanical Specification:

Item	Standard Value	Unit
Display size	1.1	inch
Module Dimension	28(W)*27.72 (H)*2.49(T)	mm
Active Area	20.148(W)*13.428(H)	mm
Number of Dots	96RGB*64Dots	Dot
Pixel pitch	0.21(W)mm*0.21(H)mm	mm
LCD Type	CSTN / Transmissive / Negative	-
Viewing Direction	6H	-
Driver	UC1682S	-
Approx. Weight	TBD	g
Various color Display	65K	-
Backlight Type	1 LED	-
Backlight Color	White	-



2. Absolute Maximum Ratings:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	V_{DD}	-0.3		+3.3	V	Ta=25℃
	V_{LCD}	-0.3		+12.0		
Input Voltage	V_{IN}	V_{SS}-0.3		V_{DD}+0.3	V	Ta=25℃
Operating Temperature	T_{OP}	-20	-	+70	℃	Ta=25℃-
Storage Temperature	T_{ST}	-30	-	+80	℃	without dewing
Humidity	-	-		90	%RH	without dewing

3. Electrical Characteristics:

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{DD}	2.8	3.0	3.3	V	1
		V_{LCD}	-	10.5	-	V	
Input Voltage (VDD=3.0V)	'H'	Vih	0.7V_{DD}	-	V_{DD}	V	
	'L'	Vil	V_{SS}	-	0.3V_{DD}		
Output Voltage (VDD=3.0V)	'H'	Vih	0.7V_{DD}	-	V_{DD}	V	
	'L'	Vil	V_{SS}	-	0.3V_{DD}		
Current Consumption		Normal Mode	-	0.6	1.5	mA	
		Partial Mode	-	TBD	TBD	μA	2

*Note 1 : IC default setting, Duty: 1/64, Bias: 1/9.
*Note 2 : 'TBD' is determined from lowest power consumption for DC-DC converter.

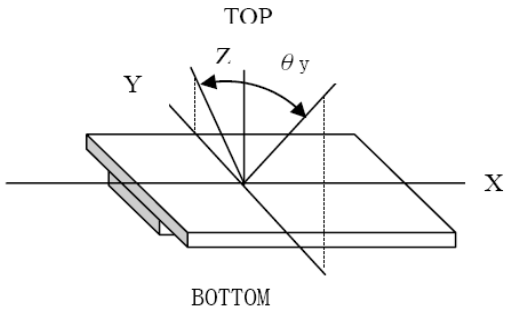
4. Optical Characteristics:

Item		Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle Cr≥10	Φ=0°	Θ	--	--	55	Deg.	T=25℃	1.2
	Φ=90°		--	--	40			
	Φ=180°		--	--	30			
	Φ=270°		--	--	40			
Contrast Ratio		Cr	5	10	--	--	T=25℃ Θ= Φ=0	3
Response Time		Rise Time(Tr)	--	--	--	msec	T=-20℃ Θ= Φ=0	4
		Decay Time(Td)	--	--	--	msec	T=-20℃ Θ= Φ=0	4
		Rise Time(Tr)	--	180	240	msec	T=+25℃ Θ= Φ=0	
		Decay Time(Td)	--	180	240	msec	T=+25℃ Θ= Φ=0	
		Rise Time(Tr)	--	--	--	msec	T=+70℃ Θ= Φ=0	
		Decay Time(Td)	--	--	--	msec	T=+70℃ Θ= Φ=0	

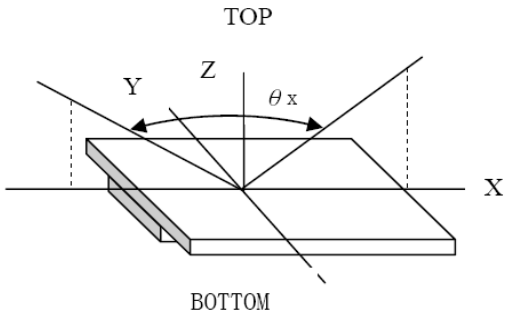
4.1 Optical Definitions

OPTICAL CHARACTERISTICS DEFINITION

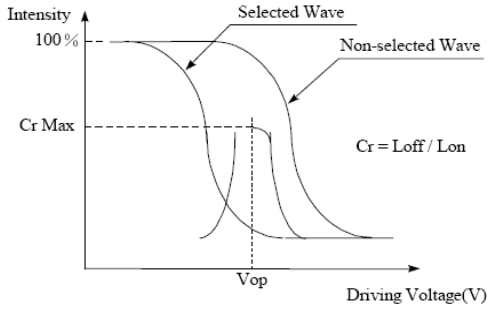
Note 1. Definition of angle θ_1 & θ_2



Note 2. Definition of angle θ_3 & θ_4



Note 3. Definition of contrast ratio (Cr)



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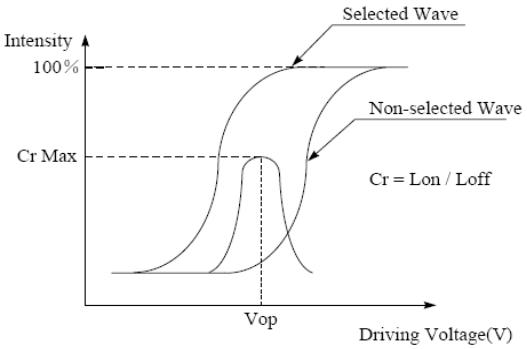
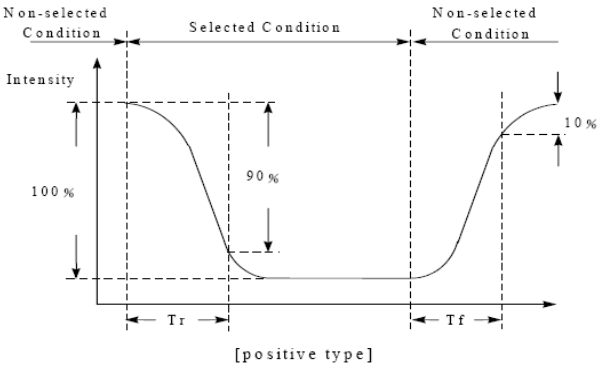
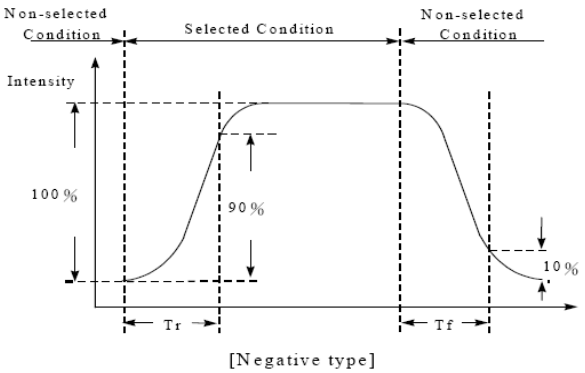


[Negative type]

Note 4. Definition of response time



[positive type]

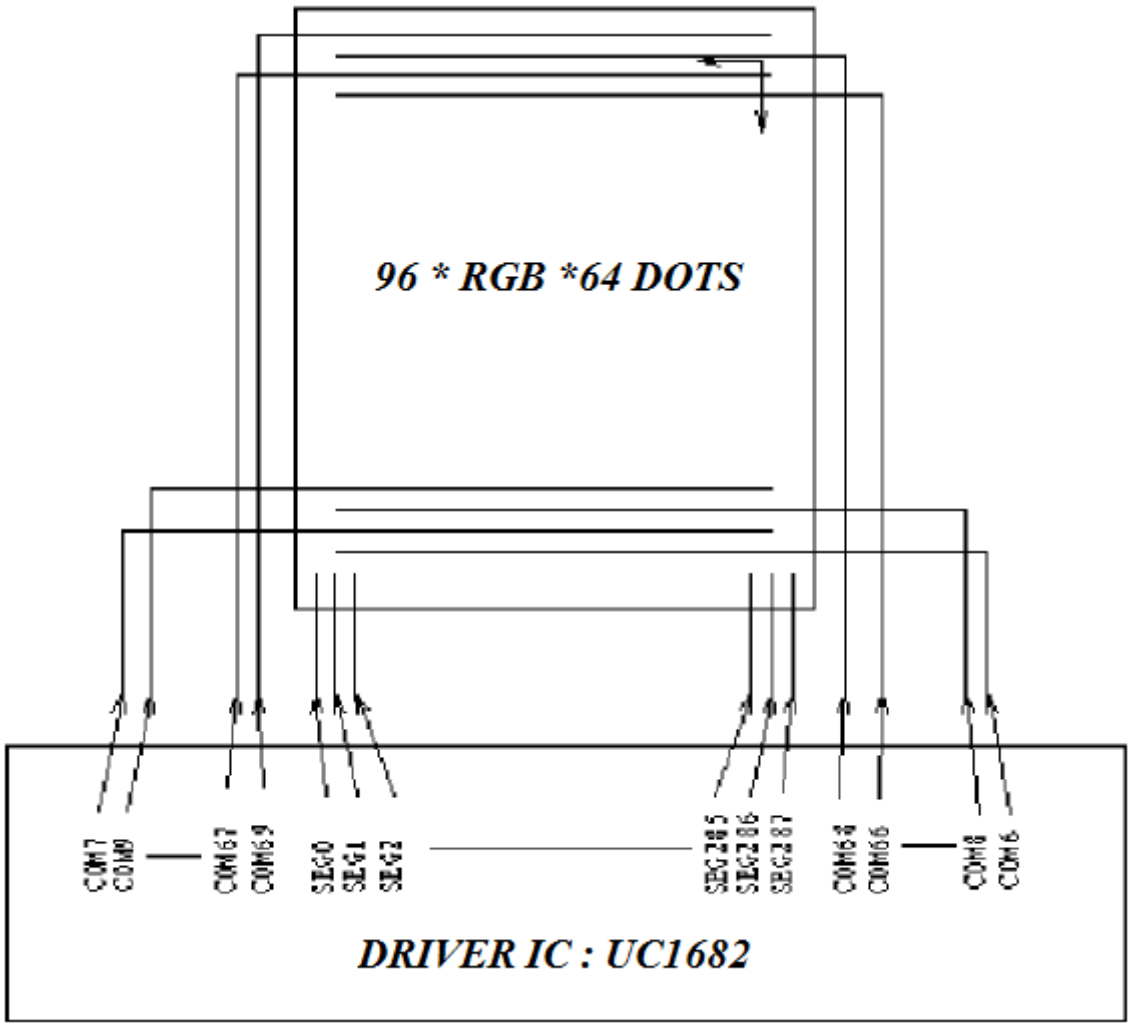


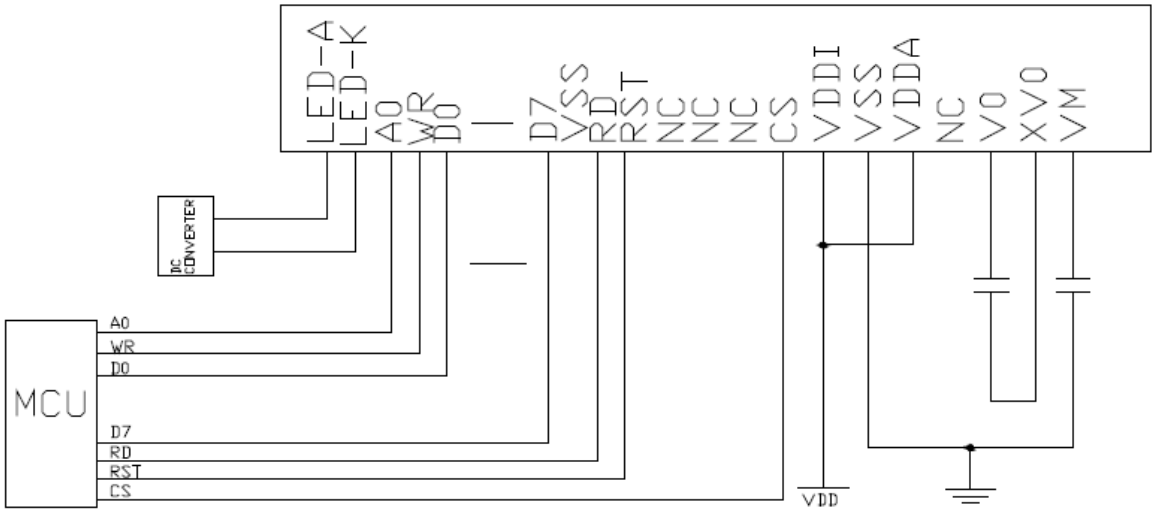
[Negative type]

5. Interface:

Pin No.	Symbol	Level	Description
1	LED_A	-	Backlight +
2	LED_K	-	Backlight -
3	A0	I	Register Selection Input Pin
4	WR	I	Read/Write Execution Control Pin
5	DB0	I/O	Data Bus
6	DB1	I/O	Data Bus
7	DB2	I/O	Data Bus
8	DB3	I/O	Data Bus
9	DB4	I/O	Data Bus
10	DB5	I/O	Data Bus
11	DB6	I/O	Data Bus
12	DB7	I/O	Data Bus
13	VSS	0V	Ground
14	RD	I	Read/Write Control Pin
15	/RST	I	Reset Input Pin
16	IF1	I	No Connect
17	IF2	I	No Connect
18	IF3	I	No Connect (Internal Bus Mode : 8080/8bit)
19	/CS	I	Chip Select Input Pin
20	VDDI	3.0V	Power Supply Voltage for Logic
21	VSS	0V	Ground
22	VDDA	O	Power Supply for Booster Circuit
23	VM	O	No Connect
24	V0	O	Positive LCD Driver Supply Voltage
25	XV0	O	Negative LCD Driver Supply Voltage
26	VLCD	O	Bias LCD Driver Supply Voltage

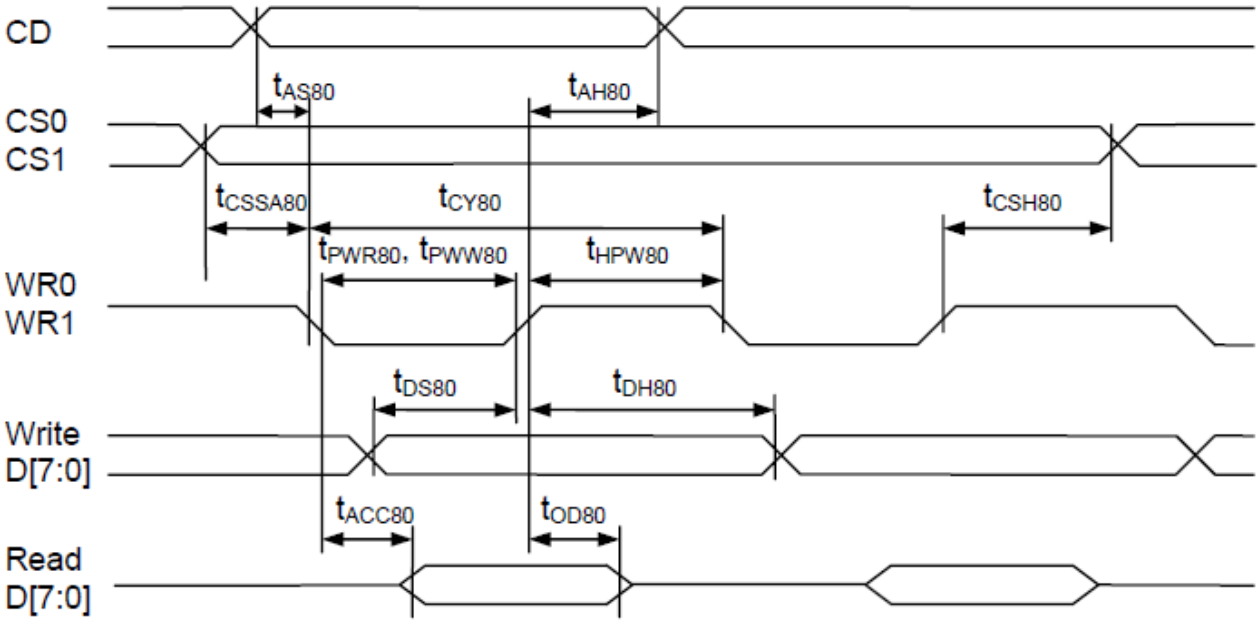
6. Block Diagram:





7. Timing Control:

7.1 Parallel Interface Characteristics Bus (8080-series MCU)



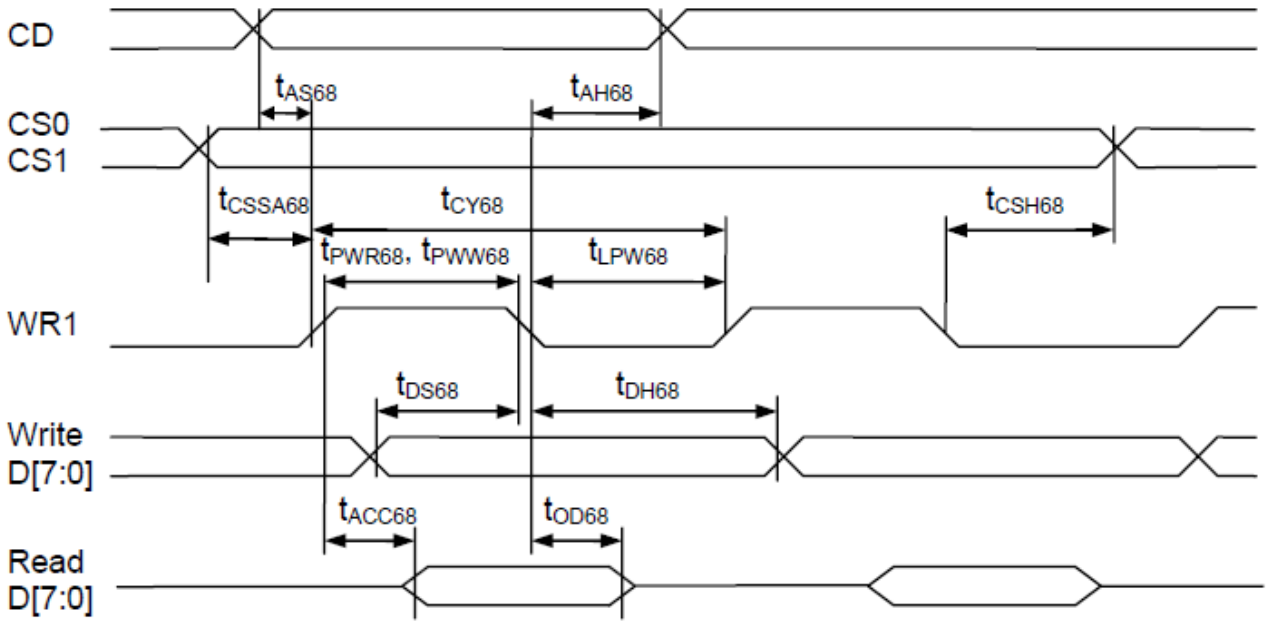
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 30	80 40	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0		nS

($1.65V \leq V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 280 160 280 160	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		140 140	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		80 80	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 40	160 80	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0		nS

7.2 Parallel Interface Characteristics Bus (6800-series MCU)



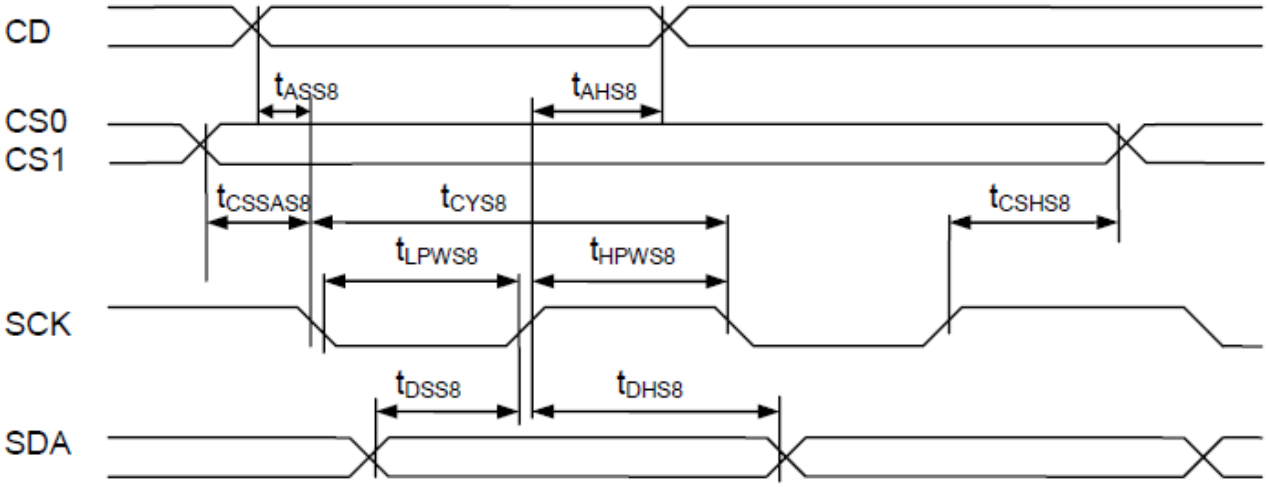
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 30	80 –	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 280 160 280 160	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		140 140	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		80 80	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 40	160 –	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0		nS

7.3 Serial Interface Characteristics (3-pin Serial)



(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

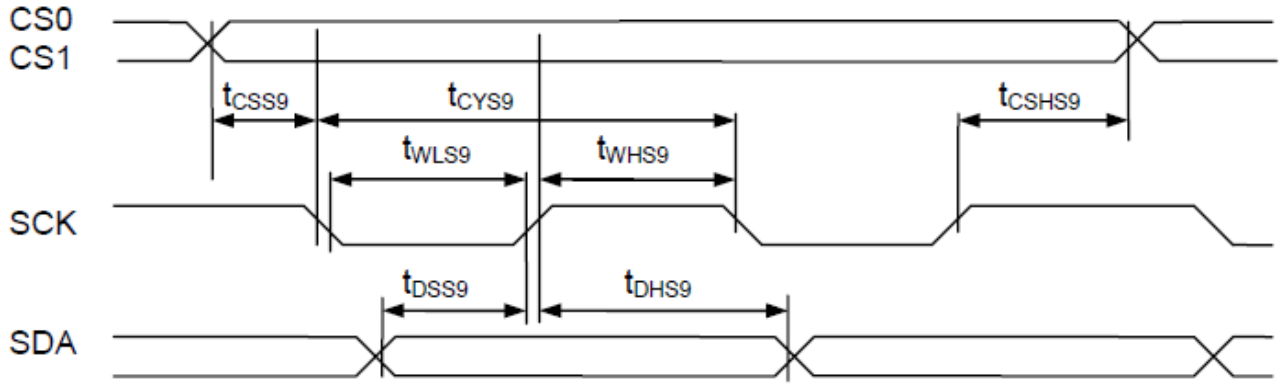
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		80	–	nS
t_{LPWS8}		Low pulse width		35	–	nS
t_{HPWS8}		High pulse width		35	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 17	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		0 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		160	–	nS
t_{LPWS8}		Low pulse width		70	–	nS
t_{HPWS8}		High pulse width		70	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		60 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		0 10		nS

Note: When V_{DD} < 2.0V, letting V_{IL}=0.1V_{DD} and V_{IH}=0.9V_{DD} is recommended.

7.4 Serial Interface Characteristics (4-pin Serial)



(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

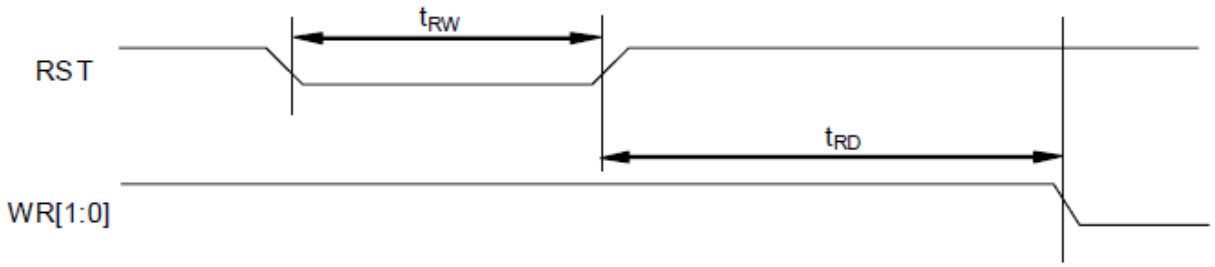
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		80	–	nS
t_{LPWS9}		Low pulse width		35	–	nS
t_{HPWS9}		High pulse width		35	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		0 0		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		160	–	nS
t_{LPWS9}		Low pulse width		70	–	nS
t_{HPWS9}		High pulse width		70	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		60 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		0 0		nS

Note: When V_{DD} < 2.0V, letting V_{IL}=0.1V_{DD} and V_{IH}=0.9V_{DD} is recommended.

7.5 Reset Timing



(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

8. Backlight:

1. Standard Lamp Styles (Edge Lighting Type)
   The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption :

2. The Main Advantages of the LED Backlight are as Following :
   The brightness of the backlight can simply be adjusted.
   By a resistor or a potentiometer.

3. Data About LED Backlight

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	Vf	-	3.0	3.3	V	If=15 mA
Forward Current	If	-	15	-	mA	
Luminance	Lv	1600	1800	2200	cd/m^2	If=15 mA
Color Coordinate	X	0.296		0.32	If=15 mA	
	Y	0.276		0.328		