October 2007

HYB39S128400F[E/T](L)
HY[B/I]39S128800F[E/T](L)
HY[B/I]39S128160F[E/T](L)
HYB39S128407FE

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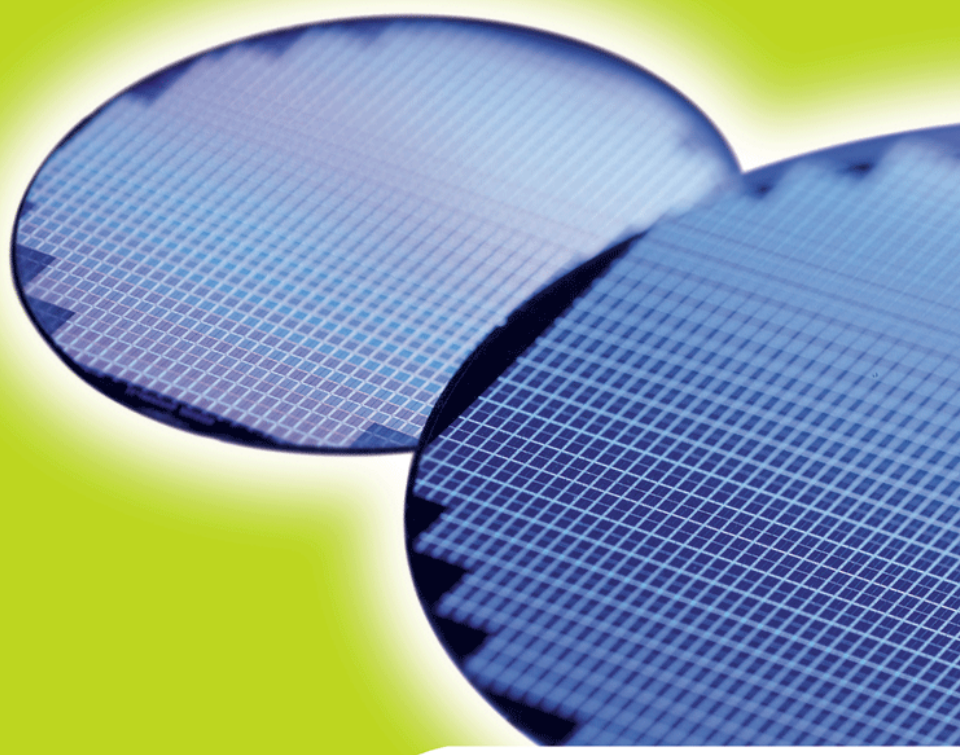
128-MBit Synchronous DRAM

Green Product

SDRAM



Data Sheet

Rev. 1.32

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HYB39S128400F[E/T](L), HY[B/I]39S128800F[E/T](L), HY[B/I]39S128160F[E/T](L) Revision History: 2007-10, Rev. 1.32	
Page	**Subjects (major changes since last revision)**
All	Adapted Internet Version
23	Corrected number of refresh cycles
Previous Revision: 2007-06, Rev. 1.31	
13	Corrected operation command "Power Down / Clock suspend ...” in truth table
15	Corrected text to "After the mode register is set a NOP command is required"
19	Corrected text to "One clock delay is required for mode entry and exit", chapter 3.5
19	Corrected the line "Input Capacitances: CK" in table 10, chapter 4
22	Corrected tCK MIN in table 14
22	Corrected CLE setup time in table 14
Previous Revision: 2007-03, Rev. 1.30	
15	Corrected mode register definition
21	IDD for low power option 0.8 mA
22	“Transition time” replaced by “Transition Time of Clock (Rise and Fall)”
4	Added HYI39S128800FT-7, HYI39S128800FE-7, HYI39S128160FT-7, HYI39S128160FE-7 and HYB39S128407FE-7
Previous Revision: 2006-10, Rev. 1.20	

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1 Overview

This chapter lists all main features of the product family HY[B/I]39S128[40/80/16][0/7]F[E/T](L) and the ordering information.

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1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C Standard Operating Temperature
- -40 to 85 °C Industrial Operating Temperature
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 4096 refresh cycles / 64 ms (15.6 µs)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface
- Plastic Packages: P(G)–TSOPII–54 400 mil width

TABLE 1
Performance

Product Type Speed Code			–7	Unit
Speed Grade			PC133–222	—
Max. Clock Frequency	@CL3	f_{CK3}	143	MHz
		t_{CK3}	7	ns
		t_{AC3}	5.4	ns
	@CL2	t_{CK2}	7.5	ns
		t_{AC2}	5.4	ns

1.2 Description

The HY[B/I]39S128[40/80/16][0/7]F[E/T](L) are four bank Synchronous DRAM's organized as 32 MBit x4, 16 MBit x8 and 8 Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with Qimonda's advanced 0.11 µm 128-MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 128-Mbit components are available in P(G)–TSOPII–54 packages.

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TABLE 2
Ordering Information for Lead-Containing Products

Product Type	Speed Grade	Description	Package
Standard Operating Temperature (0 to 70 °C)			
HYB39S128400FT-7	PC133–222–520	143MHz 32M x 4 SDRAM	P-TSOPII-54
HYB39S128400FTL-7			
HYB39S128800FT-7		143MHz 16M x 8 SDRAM	
HYB39S128800FTL-7			
HYB39S128160FT-7		143MHz 8M x 16 SDRAM	
HYB39S128160FTL-7			
Industrial Operating Temperature (-40 to 85 °C)			
HYI39S128800FT-7	PC133–222–520	143MHz 16M x 8 SDRAM	P-TSOPII-54
HYI39S128160FT-7		143MHz 8M x 16 SDRAM	

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TABLE 3
Ordering Information for RoHS Compliant Products

Product Type	Speed Grade	Description	Package	Note
Standard Operating Temperature (0 to 70 °C)				
HYB39S128400FE-7	PC133–222–520	143MHz 32M x 4 SDRAM	PG-TSOPII-54 green Product	1)
HYB39S128400FEL-7				
HYB39S128407FE-7				
HYB39S128800FE-7		143MHz 16M x 8 SDRAM		
HYB39S128800FEL-7				
HYB39S128160FE-7		143MHz 8M x 16 SDRAM		
HYB39S128160FEL-7				
Industrial Operating Temperature (-40 to 85 °C)				
HYI39S128800FE-7	PC133–222–520	143MHz 16M x 8 SDRAM	PG-TSOPII-54 green Product	1)
HYI39S128160FE-7		143MHz 8M x 16 SDRAM		

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

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2 Chip Configuration

This chapter contains the pin configuration table, the TSOP package drawing, and the block diagrams for the ×4, ×8, ×16 organization of the SDRAM.

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2.1 Pin Description

Listed below are the pin configurations sections for the various signals of the SDRAM

TABLE 4
Pin Configuration of the SDRAM

Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals ×4/×8/×16 Organization				
38	CLK	I	LVTTL	**Clock Signal CK**
37	CKE	I	LVTTL	**Clock Enable**
Control Signals ×4/×8/×16 Organization				
18	$\overline{RAS}$	I	LVTTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
17	$\overline{CAS}$	I	LVTTL	
16	$\overline{WE}$	I	LVTTL	
19	$\overline{CS}$	I	LVTTL	**Chip Select**
Address Signals ×4/×8/×16 Organization				
20	BA0	I	LVTTL	**Bank Address Signals 1:0**
21	BA1	I	LVTTL	
23	A0	I	LVTTL	**Address Signal, Address Signal 10/Auto precharge**
24	A1	I	LVTTL	
25	A2	I	LVTTL	
26	A3	I	LVTTL	
29	A4	I	LVTTL	
30	A5	I	LVTTL	
31	A6	I	LVTTL	
32	A7	I	LVTTL	
33	A8	I	LVTTL	
34	A9	I	LVTTL	
22	A10	I	LVTTL	
35	A11	I	LVTTL	

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Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals ×4 Organization				
5	DQ0	I/O	LVTTL	**Data Signal Bus**
11	DQ1	I/O	LVTTL	
44	DQ2	I/O	LVTTL	
50	DQ3	I/O	LVTTL	
Data Signals ×8 Organization				
2	DQ0	I/O	LVTTL	**Data Signal Bus**
5	DQ1	I/O	LVTTL	
8	DQ2	I/O	LVTTL	
11	DQ3	I/O	LVTTL	
44	DQ4	I/O	LVTTL	
47	DQ5	I/O	LVTTL	
50	DQ6	I/O	LVTTL	
53	DQ7	I/O	LVTTL	
Data Signals ×16 Organization				
2	DQ0	I/O	LVTTL	**Data Signal Bus**
4	DQ1	I/O	LVTTL	
5	DQ2	I/O	LVTTL	
7	DQ3	I/O	LVTTL	
8	DQ4	I/O	LVTTL	
10	DQ5	I/O	LVTTL	
11	DQ6	I/O	LVTTL	
13	DQ7	I/O	LVTTL	
42	DQ8	I/O	LVTTL	
44	DQ9	I/O	LVTTL	
45	DQ10	I/O	LVTTL	
47	DQ11	I/O	LVTTL	
48	DQ12	I/O	LVTTL	
50	DQ13	I/O	LVTTL	
51	DQ14	I/O	LVTTL	
53	DQ15	I/O	LVTTL	
Data Mask ×4/×8 Organization				
39	DQM	I/O	LVTTL	**Data Mask**
Data Mask ×16 Organization				
39	UDQM	I/O	LVTTL	**Data Mask Upper Byte**
15	LDQM	I/O	LVTTL	**Data Mask Lower Byte**

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Ball No.	Name	Pin Type	Buffer Type	Function
Power Supplies ×4/×8/×16 Organization				
9	V_{DDQ}	PWR	–	**Power Supply**
14	V_{DD}	PWR	–	**Power Supply**
46	V_{SSQ}	PWR	–	**Power Supply Ground for DQs**
41	V_{SS}	PWR	–	**Power Supply Ground**
Not connected ×4 Organization				
2, 4, 7, 8, 10, 13, 15, 36, 40, 42, 45, 47, 48, 51, 53	NC	NC	–	**Not connected**
Not connected ×8 Organization				
4, 7, 10, 13, 15, 36, 40, 42, 45, 48, 51	NC	NC	–	**Not connected**
Not connected ×16 Organization				
36, 40	NC	NC	–	**Not connected**

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2.2 Package P(G)–TSOPII–54

Listed below are the pin outs of the TSOP package.

FIGURE 1
Pin Configuration P(G)-TSOPII-54

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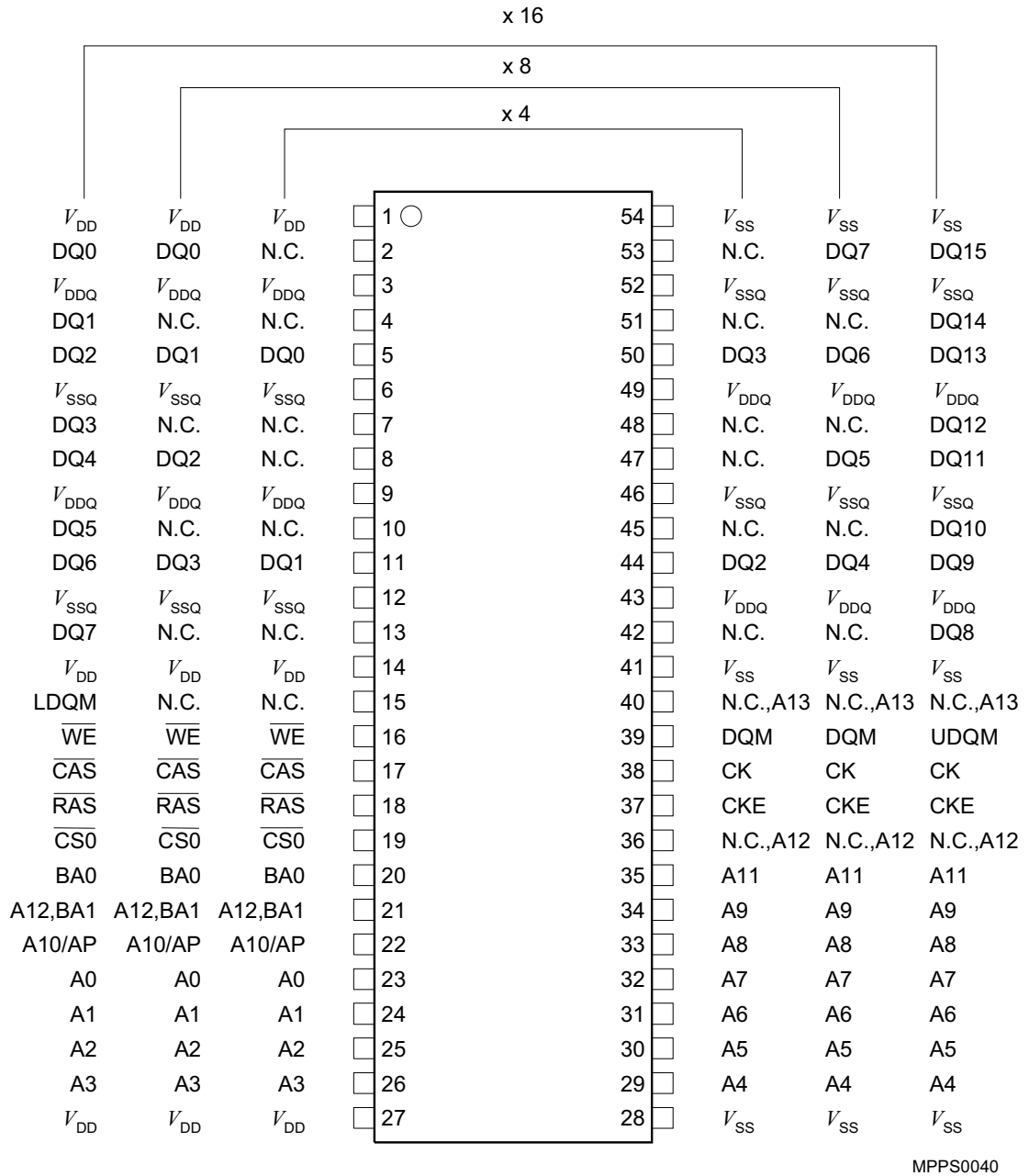

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3 Functional Description

This chapter list all defined commands and their usage for this Synchronous DRAM family.

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TABLE 5
Truth Table: Operation Command

Operation	Device State	CKE n-1[1)2)]	CKE n[1)2)]	DQM [1)2)]	BA0 BA1[1)2)]	AP= A10[1)2)]	Addr. [1)2)]	$\overline{CS}$[1)2)]	$\overline{RAS}$[1)2)]	$\overline{CAS}$[1)2)]	$\overline{WE}$[1)2)]
Bank Active	Idle[3)]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3)]	H	X	X	V	L	V	L	H	L	L
Write with Auto precharge	Active[3)]	H	X	X	V	H	V	L	H	L	L
Read	Active[3)]	H	X	X	V	L	V	L	H	L	H
Read with Auto precharge	Active[3)]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down/ Clock Suspend Entry	Active or Idle or Burst	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down/ Clock Suspend Exit	Active or Idle or Burst	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/ Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/ Output Disable	Active	H	X	H	X	X	X	X	X	X	X

1) V = Valid, x = Don't Care, L = Low Level, H = High Level
2) CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3) This is the state of the banks designated by BA0, BA1 signals.

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BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	WBL	TM		CL			BT	BL		
reg. addr					w				w		w		w	

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TABLE 6
Mode Register Definition ($BA_{1:0} = 00_B$)

Field	Bits	Type	Description
BL	2:0	w	**Burst Length** Number of sequential bits per DQ related to one read/write command *Note: All other bit combinations are RESERVED* 000_B **1** 001_B **2** 010_B **4** 011_B **8** 111_B **Full Page (Sequential burst type only)**
BT	3		**Burst Type** 0_B **Sequential** 1_B **Interleaved**
CL	6:4		**CAS Latency** Number of full clocks from read command to first data valid window. *Note: All other bit combinations are RESERVED.* 010_B **2** 011_B **3**
TM	8:7		**Test Mode** *Note: All other bit combinations are RESERVED.* 00_B **Mode register set**
WBL	9		**Write Burst Length** 0_B **Burst write** 1_B **Single bit write**
	12:10		Reserved, set to zero

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TABLE 7
Burst Length and Sequence

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type=Sequential	Type=Interleaved
2			0	0–1	0–1
			1	1–0	1–0
4		0	0	0–1–2–3	0–1–2–3
		0	1	1–2–3–0	1–0–3–2
		1	0	2–3–0–1	2–3–0–1
		1	1	3–0–1–2	3–2–1–0
8	0	0	0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0	0	1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0	1	0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0	1	1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1	0	0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1	0	1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1	1	0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1	1	1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0
FullPage	n			Cn, Cn+1, Cn+2	Not supported

Notes

1. *For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.*
3. *For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access with in the block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*

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4 Electrical Characteristics

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4.1 Operating Conditions

TABLE 8
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/ Test Condition
		Min.	Max.		
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 1.0	+4.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	– 1.0	+4.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	– 1.0	+4.6	V	–
Operating Temperature for HYB...	T_A	0	+70	°C	–
Operating Temperature for HYI...	T_A	-40	+85	°C	–
Storage temperature range	T_{STG}	-55	+150	°C	–
Power dissipation per SDRAM component	P_D	–	1	W	–
Data out current (short circuit)	I_{OUT}	–	50	mA	–

***Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

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TABLE 9
DC Characteristics

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Supply Voltage	V_{DD}	3.0	3.6	V	1)2)
I/O Supply Voltage	V_{DDQ}	3.0	3.6	V	1)2)
Input high voltage	V_{IH}	2.0	V_{DDQ}+0.3	V	1)2)3)
Input low voltage	V_{IL}	– 0.3	+0.8	V	1)2)3)
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V	1)2)
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V	1)2)
Input leakage current, any input(0 V < V_{IN} < V_{DD}, all other inputs = 0 V)	I_{IL}	– 5	+5	µA	1)
Output leakage current(DQs are disabled, 0 V < V_{OUT} < V_{DDQ})	I_{OL}	– 5	+5	µA	1)

1) T_A = 0 to 70 °C
2) All voltages are referenced to V_{SS}
3) V_{IH} may overshoot to V_{DDQ} + 2.0 V for pulse width of < 4ns with 3.3 V. V_{IL} may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

TABLE 10
Input and Output Capacitances

Parameter	Symbol	Values[1)]		Unit	Note
		Min.	Max.		
Input Capacitances: CK	C_{I1}	2.5	3.5	pF	2)
Input Capacitance (A0-A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	2.5	3.8	pF	2)
Input/Output Capacitance (DQ)	C_{I0}	4.0	6.0	pF	2)

1) Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF
2) T_A = 0 to 70 °C; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V, f = 1 MHz

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TABLE 11
IDD Conditions

Parameter	Symbol
Operating Current One bank active, Burst length = 1	I_{DD1}
Precharge Standby Current in Power Down Mode	I_{DD2P}
Recharge Standby Current in Non-Power Down Mode	I_{DD2N}
No Operating Current Active state (max. 4 banks)	I_{DD3N} I_{DD3P}
Burst Operating Current Read command cycling	I_{DD4}
Auto Refresh Current Auto Refresh command cycling	I_{DD5}
Self Refresh Current (standard components) Self Refresh Mode, CKE=0.2 V, t_{CK}=infinity	I_{DD6}
Self Refresh Current (low power components) Self Refresh Mode, CKE=0.2 V, t_{CK}=infinity	

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TABLE 12
I_{DD} Specifications and Conditions

Symbol		–7	Unit	Note/ Test Condition
		Max.		
I_{DD1}	$t_{RC} = t_{RC(min)}$, I_O = 0 mA	80	mA	1)2)3)4)
I_{DD2P}	$\overline{CS} = V_{IH\ (min.)}$, CKE $\leq V_{IL(max)}$	2	mA	1)2)
I_{DD2N}	$\overline{CS} = V_{IH\ (min.)}$, CKE$\geq V_{IH(min)}$	22	mA	1)2)
I_{DD3N}	CS = $V_{IH(min)}$, CKE $\geq V_{IH(min.)}$	35	mA	1)2)
I_{DD3P}	CS = $V_{IH(min)}$, CKE $\leq V_{IL(max.)}$	5	mA	1)2)
I_{DD4}		65	mA	1)2)4)
I_{DD5}	$t_{RFC} = t_{RFC(min)}$	146	mA	1)2)5)
	t_{RFC}= 15.6 µs	25	mA	1)2)
I_{DD6}		3	mA	1)2) Standard components
		0.8	mA	1) Low power components at 85 °C

1) Currents values will be added when available.
2) T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V
3) These parameters depend on the cycle rate. All values are measured at 133 MHz for -7 with the outputs open. Input signals are changed once during t_{CK}.
4) These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the V_{DDQ} current is excluded.
5) $t_{RFC} = t_{RFC(min)}$ "burst refresh", t_{RFC}= 15.6 µs "distributed refresh".

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4.2 AC Characteristics

TABLE 13
AC Timing - Absolute Specifications –7

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Parameter	Symbol	–7		Unit	Note
		PC133– 222			
		Min.	Max.		
Clock and Clock Enable					
Clock Frequency	t_{CK}	7 7.5	— —	ns ns	CL3 [1)2)3)] CL2 [1)2)3)]
Access Time from Clock	t_{AC}	— —	5.4 5.4	ns ns	CL3[1)2)3)] CL2[1)2)3)4)5)]
Clock High Pulse Width	t_{CH}	2.5	—	ns	[1)2)3)]
Clock Low Pulse Width	t_{CL}	2.5	—	ns	[1)2)3)]
Transition Time of Clock (Rise and Fall)	t_T	0.3	1.2	ns	[1)2)3)]
Setup and Hold Times					
Input Setup Time	t_{IS}	1.5	—	ns	[1)2)3)6)]
Input Hold Time	t_{IH}	0.8	—	ns	[1)2)3)6)]
CKE Setup Time	t_{CKS}	1.5	—	ns	[1)2)3)6)]
CKE Hold Time	t_{CKH}	0.8	—	ns	[1)2)3)6)]
Mode Register Set-up to Active delay	t_{RSC}	2	—	t_{CK}	[1)2)3)]
Power Down Mode Entry Time	t_{SB}	0	7	ns	[1)2)3)]
Common Parameters					
Row to Column Delay Time	t_{RCD}	15	—	ns	[1)2)3)7)]
Row Precharge Time	t_{RP}	15	—	ns	[1)2)3)7)]
Row Active Time	t_{RAS}	37	100k	ns	[1)2)3)7)]
Row Cycle Time	t_{RC}	60	—	ns	[1)2)3)7)]
Row Cycle Time during Auto Refresh	t_{RFC}	63	—	ns	[1)2)3)]
Activate(a) to Activate(b) Command period	t_{RRD}	14	—	ns	[1)2)3)7)]
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	—	t_{CK}	[1)2)3)]
Refresh Cycle					
Refresh Period (4096 cycles)	t_{REF}	–	64	ms	[1)2)3)]
Self Refresh Exit Time	t_{SREX}	1	—	t_{CK}	[1)2)3)]
Data Out Hold Time	t_{OH}	3	—	ns	[1)2)3)5)]
Read Cycle					
Data Out to Low Impedance Time	t_{LZ}	0	—	ns	[1)2)3)]
Data Out to High Impedance Time	t_{HZ}	3	7	ns	[1)2)3)]
DQM Data Out Disable Latency	t_{DQZ}	—	2	t_{CK}	[1)2)3)]

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Parameter	Symbol	–7		Unit	Note
		PC133– 222			
		Min.	Max.		
Write Cycle					
Last Data Input to Precharge (Write without Auto Precharge)	t_{WR}	14	—	ns	1)2)3)8)
Last Data Input to Activate(Write with Auto Precharge)	$t_{DAL(min.)}$			t_{CK}	1)2)3)9)
DQM Write Mask Latency	t_{DQW}	0	—	t_{CK}	1)2)3)

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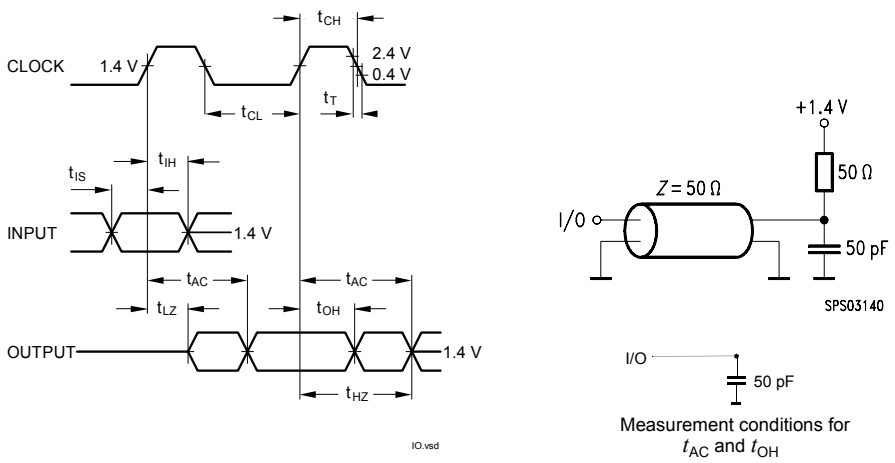
1) T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V, t_T = 1 ns
2) For proper power-up see the operation section of this data sheet.
3) AC timing tests for LV-TTL versions have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.
4) If clock rising time is longer than 1 ns, a time (t_T/2 - 0.5) ns has to be added to this parameter.
5) Access time from clock t_{ac} is 4.6 ns for PC133 components with no termination and 0 pF load,Data out hold time t_{oh} is 1.8 ns for PC133 components with no termination and 0 pF load.
6) If t_T is longer than 1 ns, a time (t_T - 1) ns has to be added to this parameter.
7) These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows:the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
8) It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times t_{CK} greater or equal the specified tWR value, where t_{ck} is equal to the actual system clock time.
9) When a Write command with Auto Precharge has been issued, a time of $t_{DAL(min)}$ has be fullfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. t_{CK} is equal to the actual system clock time.

FIGURE 2
Measurement conditions for t_{AC} and t_{OH}



Measurement conditions for t_{AC} and t_{OH}

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5 Package Outlines

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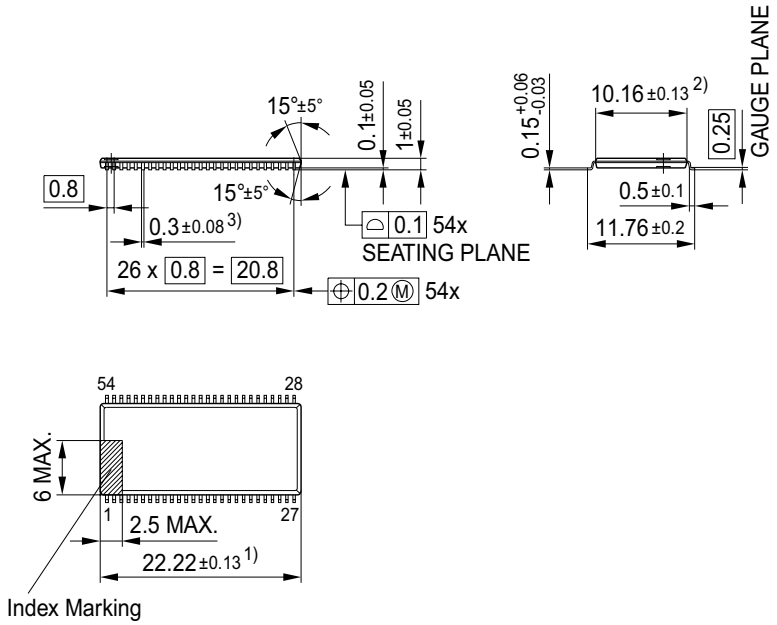
FIGURE 3
Package Outline PG-TSOPII-54-4 (top view)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include plastic protrusion of 0.25 max. per side
3) Does not include dambar protrusion of 0.13 max. per side

GPX01088

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

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List of Figures

Figure 1 Pin Configuration P(G)-TSOPII-54 8
Figure 2 Measurement conditions for t_{AC} and t_{OH} 16
Figure 3 Package Outline PG-TSOPII-54-4 (top view) 17

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List of Tables

Table 1 Performance . . . 3
Table 2 Ordering Information for Lead-Containing Products . . . 4
Table 3 Ordering Information for RoHS Compliant Products . . . 4
Table 4 Pin Configuration of the SDRAM . . . 5
Table 5 Truth Table: Operation Command . . . 9
Table 6 Mode Register Definition ($BA_{1:0} = 00_B$) . . . 10
Table 7 Burst Length and Sequence . . . 11
Table 8 Absolute Maximum Ratings . . . 12
Table 9 DC Characteristics . . . 13
Table 10 Input and Output Capacitances . . . 13
Table 11 IDD Conditions . . . 14
Table 12 I_{DD} Specifications and Conditions . . . 14
Table 13 AC Timing - Absolute Specifications –7 . . . 15

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Table of Contents

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1 Overview . . . 3
1.1 Features . . . 3
1.2 Description . . . 3
2 Chip Configuration . . . 5
2.1 Pin Description . . . 5
2.2 Package P(G)–TSOPII–54 . . . 8
3 Functional Description . . . 9
4 Electrical Characteristics . . . 12
4.1 Operating Conditions . . . 12
4.2 AC Characteristics . . . 15
5 Package Outlines . . . 17
List of Figures . . . 18
List of Tables . . . 19
Table of Contents . . . 20

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