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HYB18T256161AF–22/25/28/33
HYB18T256161AFL25/28/33

256-Mbit x16 GDDR2 DRAM

RoHS compliant

Memory Products

N e v e r s t o p t h i n k i n g.

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HYB18T256161AF–22/25/28/33 HYB18T256161AFL25/28/33

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Page	Subjects (major changes since last revision)
all	added speed sort L25, L28, L33

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1 Overview

This chapter gives an overview of the 256-Mbit x16 GDDR2 DRAM product family and describes its main characteristics.

1.1 Features

The 256-Mbit x16 GDDR2 DRAM is optimized for graphics applications and offers the following key features:

- 2.0V +/- 0.1V VDD core voltage (HYB18T256161AF-22/-25/-28/-33)
- 2.0V +/- 0.1V VDDQ IO voltage (HYB18T256161AF-22/-25/-28/-33)
- 1.8V +/- 0.1V VDD core voltage (HYB18T256161AFL25/28/33)
- 1.8V +/- 0.1V VDDQ IO voltage (HYB18T256161AFL25/28/33)
- DLL-off mode operation support
- DRAM organisations with 16 data in/outputs
- Double Data Rate architecture: two data transfers per clock cycle, internal banks for concurrent operation
- CAS Latency: 5 and 6
- Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Bi-directional, differential data strobes (DQS and $\overline{\text{DQS}}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- $\overline{\text{DQS}}$ can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality.
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Normal and Weak Strength Data-Output Drivers
- 1K page size
- Packages: PG-TFBGA 84

1.2 Ordering Information

Table 1 Ordering information

Part Number	Org.	Package
HYB18T256161AF-22/-25/-28/-33	16Mx16	PG-TFBGA 84
HYB18T256161AFL25/L28/L33		

1.3 Description

The 256-Mbit x16 GDDR2 DRAMis a high-speed Double-Data-Rate-2 CMOS Synchronous DRAM device containing 268,435,456 bits and internally configured as a q-bank DRAM. The 256-Mbit x16 GDDR2 DRAMis organized as hip. These synchronous devices achieve high speed transfer rates up to 900 Mb/sec/pin and is optimized for graphics performance.

The device is designed to comply with all DDR2 DRAM key features:

1. posted CAS with additive latency,
2. write latency = read latency - 1,
3. normal and weak strength data-output driver,
4. Off-Chip Driver (OCD) impedance adjustment and
5. an On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{\text{CK}}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS-$\overline{\text{DQS}}$ pair in a source synchronous fashion.

A 1is used to convey row, column and bank address information in a RAS-CAS multiplexing style.

The desktop DDR2 device operates at a 2.0V +/- 0.1V, the low power device at 1.8V +/- 0.1V power supply. An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The 256-Mbit x16 GDDR2 DRAM is available in P-TFBGA package.

1.4 Pin Configuration

The pin configuration of a 256-Mbit x16 GDDR2 DRAM is listed by function in **Table 2**. The abbreviations used in the Pin#/Buffer Type columns are explained in **Table 3** and **Table 4** respectively. The pin numbering for the FBGA package is depicted in **Figure 1**.

Table 2 Pin Configuration of 256-Mbit x16 GDDR2 DRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals organization				
J8	CK	I	SSTL	**Clock Signal**
K8	$\overline{CK}$	I	SSTL	**Complementary Clock Signal**
K2	CKE	I	SSTL	**Clock Enable Rank**
Control Signals organization				
K7	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
L7	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
K3	$\overline{WE}$	I	SSTL	**Write Enable**
L8	$\overline{CS}$	I	SSTL	**Chip Select**
L8	A13	I	SSTL	**Address Signal 13**
Address Signals organization				
L2	BA0	I	SSTL	**Bank Address Bus 1:0**
L3	BA1	I	SSTL	
L1	NC	–	–	
M8	A0	I	SSTL	**Address Signal 12:0**
M3	A1	I	SSTL	
M7	A2	I	SSTL	
N2	A3	I	SSTL	
N8	A4	I	SSTL	
N3	A5	I	SSTL	
N7	A6	I	SSTL	
P2	A7	I	SSTL	
P8	A8	I	SSTL	
P3	A9	I	SSTL	
M2	A10	I	SSTL	
	AP	I	SSTL	
P7	A11	I	SSTL	
R2	A12	I	SSTL	
Data Signals organization				
G8	DQ0	I/O	SSTL	**Data Signal 0**
G2	DQ1	I/O	SSTL	**Data Signal 1**
H7	DQ2	I/O	SSTL	**Data Signal 2**

Table 2 Pin Configuration of 256-Mbit x16 GDDR2 DRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
H3	DQ3	I/O	SSTL	Data Signal 3
H1	DQ4	I/O	SSTL	Data Signal 4
H9	DQ5	I/O	SSTL	Data Signal 5
F1	DQ6	I/O	SSTL	Data Signal 6
F9	DQ7	I/O	SSTL	Data Signal 7
C8	DQ8	I/O	SSTL	Data Signal 8
C2	DQ9	I/O	SSTL	Data Signal 9
D7	DQ10	I/O	SSTL	Data Signal 10
D3	DQ11	I/O	SSTL	Data Signal 11
D1	DQ12	I/O	SSTL	Data Signal 12
D9	DQ13	I/O	SSTL	Data Signal 13
B1	DQ14	I/O	SSTL	Data Signal 14
B9	DQ15	I/O	SSTL	Data Signal 15
Data Strobe organization				
B7	UDQS	I/O	SSTL	Data Strobe Upper Byte
A8	$\overline{UDQS}$	I/O	SSTL	Data Strobe Upper Byte
F7	LDQS	I/O	SSTL	Data Strobe Lower Byte
E8	$\overline{LDQS}$	I/O	SSTL	Data Strobe Lower Byte
Data Mask organization				
B3	UDM	I	SSTL	Data Mask Upper Byte
F3	LDM	I	SSTL	Data Mask Lower Byte
Power Supplies organization				
J2	V_{REF}	AI	–	I/O Reference Voltage
E9, G1, G3, G7, G9	V_{DDQ}	PWR	–	I/O Driver Power Supply
J1	V_{DDL}	PWR	–	Power Supply
E1, J9, M9, R1	V_{DD}	PWR	–	Power Supply
E7, F2, F8, H2, H8	V_{SSQ}	PWR	–	Power Supply
J7	V_{SSDL}	PWR	–	Power Supply
J3,N1,P9	V_{SS}	PWR	–	Power Supply
Not Connected organization				
A2, E2, L1, R3, R7, R8	NC	NC	–	Not Connected
Other Pins organization				
K9	ODT	–	–	On-Die Termination Control

Table 3 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 4 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	$\overline{UDQS}$	V_{DDQ}
DQ14	V_{SSQ}	UDM		B		UDQS	V_{SSQ}	DQ15
V_{DDQ}	DQ9	V_{DDQ}		C		V_{DDQ}	DQ8	V_{DDQ}
DQ12	V_{SSQ}	DQ11		D		UDQ2	V_{SSQ}	DQ13
V_{DD}	NC	V_{SS}		E		V_{SSQ}	$\overline{LDQS}$	V_{DDQ}
DQ6	V_{SSQ}	LDM		F		LDQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		G		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		H		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		J		V_{SSDL}	CK	V_{DD}
	CKE	$\overline{WE}$		K		$\overline{RAS}$	$\overline{CK}$	ODT
NC/BA2	BA0	BA1		L		$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1		M		A2	A0	V_{DD}
V_{SS}	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	V_{SS}
V_{DD}	A12	NC		R		NC	NC/A13	

MPPT0110

Figure 1 Pin Configuration PG-TFBGA 84 Top View, see the balls throught the package

Notes

1. *UDQS/$\overline{UDQS}$ is data strobe for upper byte, LDQS/$\overline{LDQS}$ is data strobe for lower byte*
2. *UDM is the data mask signal for the upper byte UDQ[7:0], LDM is the data mask signal for the lower byte DQ[7:0]*
3. *V_{DDL} and V_{DDSL} are power and ground respectively for the DLL. V_{DDL} connected to V_{DD}, and V_{DDSL} connected to V_{SS}.*

1.5 256Mbit DDR2 Addressing

Table 5 256 Mbit DDR2 Addressing

Configuration	16 x 16	Note
Number of Banks	4	
Bank Address	BA[0:1]]	
Auto-Precharge	A10 / AP	
Row Address	A[12:0]	
Column Address	A[8:0]	
Number of Column Address Bits	9	
Number of I/Os	16	
Page Size [Bytes]	1024 (1K)	

1.6 Input/Output Functional Description

Table 6 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{\text{CK}}$	Input	**Clock:** CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossing of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for self-refresh entry. Input buffers excluding CKE are disabled during self-refresh. CKE is used asynchronously to detect self-refresh exit condition. Self-refresh termination itself is synchronous. After VREF has become stable during power-on and initialisation sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during power-down.
$\overline{\text{CS}}$	Input	**Chip Select:** All commands are masked when $\overline{\text{CS}}$ is registered high. $\overline{\text{CS}}$ provides for external rank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered high) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, UDQS, $\overline{\text{UDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDM and LDM signal. The ODT pin will be ignored if the EMRS(1) is programmed to disable ODT.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	**Command Inputs:** $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered
DM, LDM, UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM and UDM are the input mask signals and control the lower or upper bytes.

Table 6 Input/Output Functional Description

Symbol	Type	Function
BA[1:0]	Input	**Bank Address Inputs:** define to which bank an Activate, Read, Write or Precharge command is being applied. BA[1:0] also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS(1) cycle.
A[12:0]	Input	**Address Inputs:** Provides the row address for Activate commands and the column address and Auto-Precharge bit A10 (=AP) for Read/Write commands to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, the bank is selected by BA[1:0]. The address inputs also provide the op-code during Mode Register Set commands.
DQ[0:15]	Input/ Output	**Data Inputs/Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) LDQS, ($\overline{LDQS}$), UDQS,($\overline{UDQS}$)	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. The data strobes DQS, LDQS, UDQS may be used in single ended mode or paired with the optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals.
NC	—	**No Connect:** no internal electrical connection is present
V_{DDQ}	Supply	**DQ Power Supply:** 2.0V +/- 0.1V for desktop 1.8V +/- 0.1V for low power
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** (internally connected to V_{DD}) 2.0V +/- 0.1V for desktop 1.8V +/- 0.1V for low power
V_{SSDL}	Supply	**DLL Ground** (internally connected to V_{SS})
V_{DD}	Supply	**Power Supply:** 2.0V +/- 0.1V for desktop 1.8V +/- 0.1V for low power
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference Voltage**

1.7 Block Diagrams

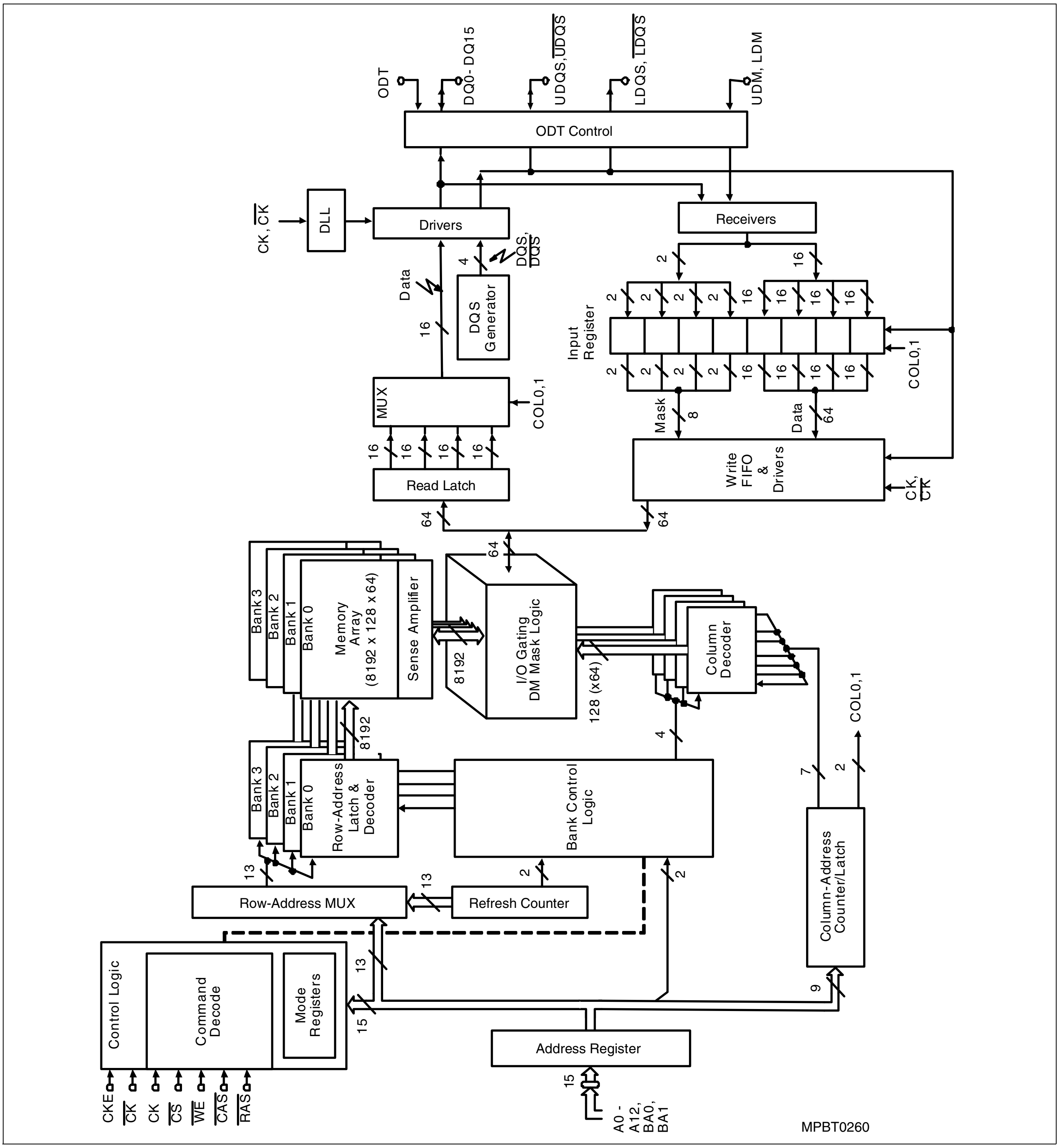


Figure 2 Block Diagram 4 Mbit × 16 I/O × 4 Internal Memory Banks

Note:

1. *16 Mb × 16 Organisation with 13 Row, 2 Bank and 10 Column External Adresses.*
2. *This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.*
3. *LDM, UDM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional LDQS and UDQS signals.*

2 Functional Description

2.1 Simplified State Diagram

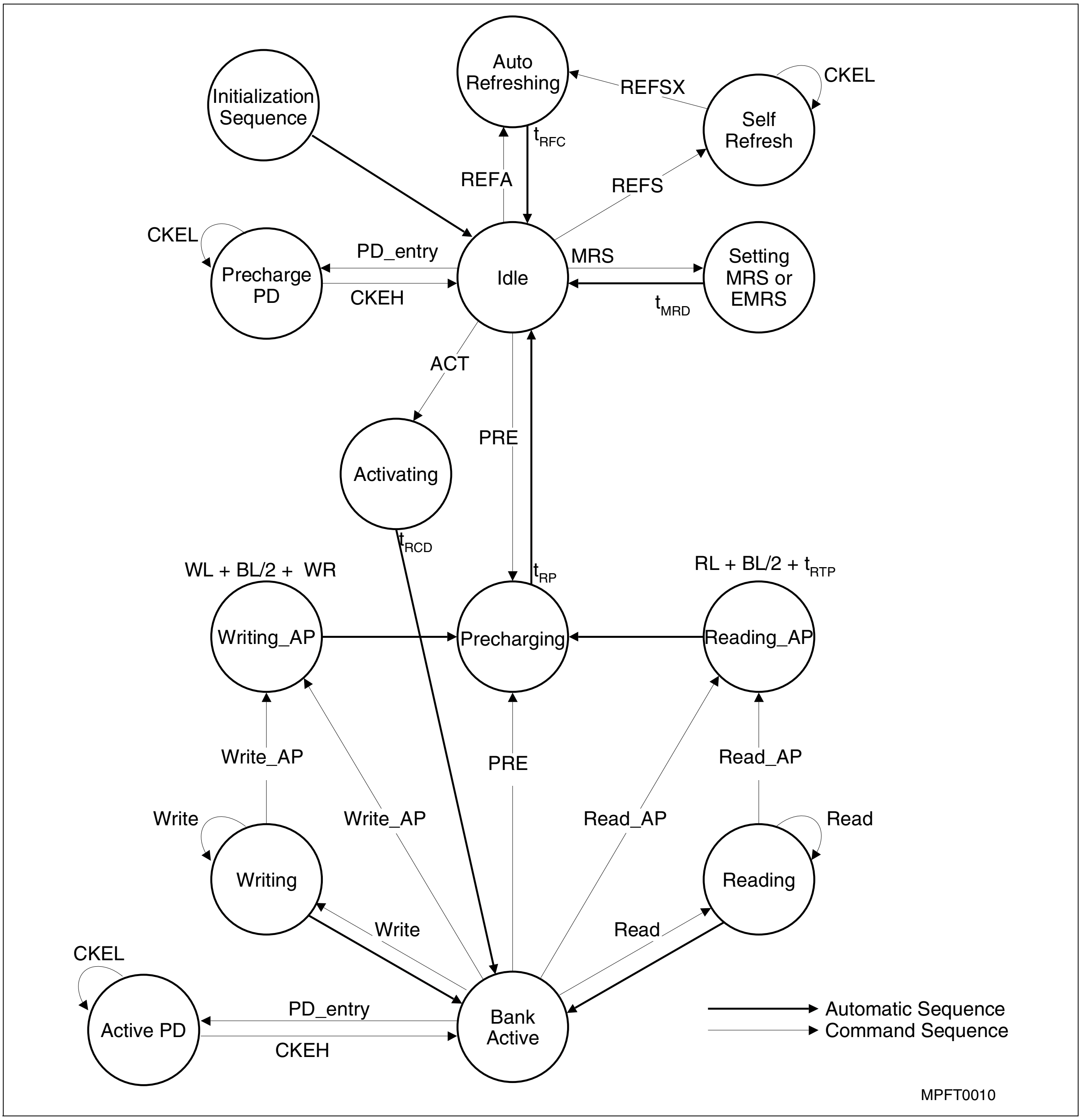


Figure 3 Simplified State Diagram

Note: This Simplified State Diagram is intended to provide a floorplan of the possible state transitions and thecommands to control them. In particular situations involving more than one bank, enabling / disabling on-die termination, Power-Down entry / exit - among other things - are not captured in full detail.

2.2 Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence.

Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accessed.

The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.2.1 Power On and Initialization

DDR2 SDRAM's must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2 ¥ VDDQ and ODT at a low state (all other inputs may be undefined). To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin. Maximum power up interval for VDD / VDDQ is specified as 10.0 ms. The power interval is defined as the amount of time it takes for VDD / VDDQ to power-up from 0 V to 2.0V +/- 0.1V for the desktop device and to 1.8 V +/- 0.1 V for the low power device. At least one of these two sets of conditions must be met:
   – V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output, AND
   – V_{TT} is limited to 0.95 V max, AND
   – V_{REF} tracks $V_{DDQ}/2$
   – or
   – Apply V_{DD} before or at the same time as V_{DDQ}.
   – Apply V_{DDQ} before or at the same time as V_{TT} & V_{REF}.
2. Start clock (CK, CK) and maintain stable power and clock condition for a minimum of 200 ms.
3. Apply NOP or Deselect commands and take CKE high.
4. Continue NOP or Deselect Commands for 400 ns, then issue a Precharge All command.
5. Issue EMRS(2) command.
6. Issue EMRS(3) command.
7. Issue EMRS(1) command to enable DLL.
8. Issue a MRS command for "DLL reset".
9. Issue Precharge-all command.
10. Issue 2 or more Auto-refresh commands.
11. Issue the final MRS command to turn the DLL on and to set the necessary operating parameter.
12. At least 200 clocks after step 8, issue EMRS(1) commands to either execute the OCD calibration or select the OCD default. Issue the final EMRS(1) command to exit OCD calibration mode and set the necessary operating parameters.
13. The DDR2 SDRAM is now ready for normal operation.

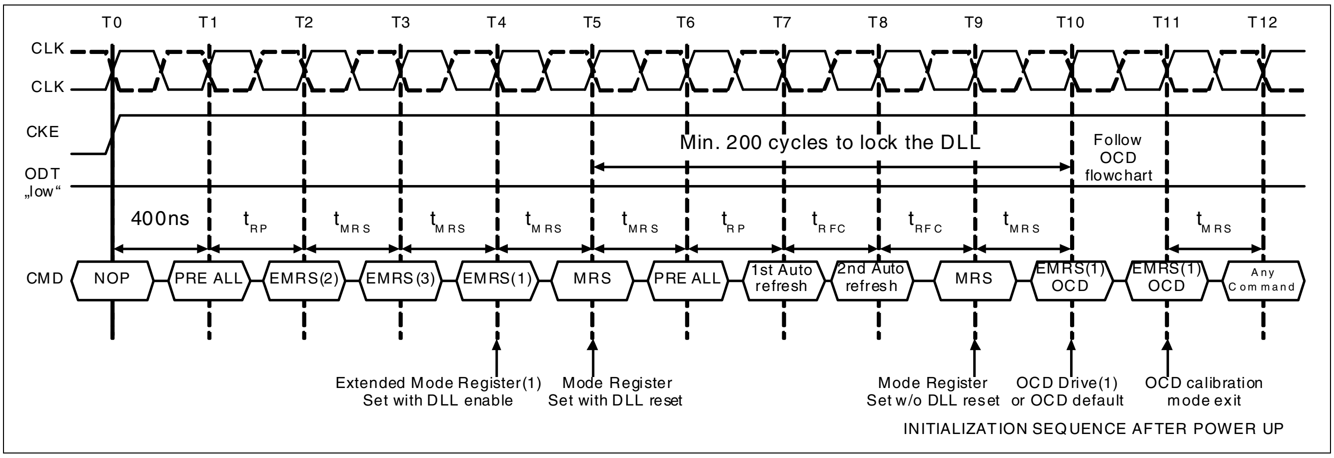


Figure 4 Initialization Sequence after Power Up

2.2.2 Programming the Mode Register and Extended Mode Registers

For application flexibility, burst length, burst type, CAS latency, DLL reset function, write recovery time (t_{WR}) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive CAS latency, driver impedance, On Die Termination (ODT), single-ended strobe and Off Chip Driver impedance adjustment (OCD) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command.

Contents of the Mode Register (MRS) or Extended Mode Registers (EMRS(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

Also any programming of EMRS(2) or EMRS(3) must be followed by programming of MRS and EMRS(1). After initial power up, all MRS and EMRS Commands must be issued before read or write cycles may begin. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Either MRS or EMRS Commands are activated by the low signals of CS, RAS, CAS and WE at the positive edge of the clock.

When all bank addresses BA[2:0] are low, the DDR2 SDRAM enables the MRS command. When the bank addresses BA0 is high and BA[2:1] are low, the DDR2 SDRAM enables the EMRS(1) command.

The address input data during this cycle defines the parameters to be set as shown in the MRS and EMRS table. A new command may be issued after the mode register set command cycle time (t_{MRD}).

MRS, EMRS and DLL Reset do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.2.3 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs CAS latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications.

The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS, RAS, CAS, WE, BA[0:1]BA[2:0], while controlling the state of address pins A[1213:0]. The DDR2 SDRAM should be in all bank precharged (idle) mode with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharged state. The mode register is divided into various fields depending on functionality.

Burst length is defined by A[2:0] with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and CAS latency is defined by A[6:4]. A7 is used for test mode and must be set to 0 for normal DRAM operation. A8 is used for DLL reset. A[11:9] are used for write recovery time (WR) definition for Auto-Precharge mode. With address bit A12 two Power-Down modes can be selected, a “standard mode” and a “low-power” Power-Down mode, where the DLL is disabled. Address bit A13 and all “higher” address bits (including BA2) have to be set to 0 for compatibility with other DDR2 memory products with higher memory densities.

MR
Mode Register Definition **(BA[1:0] = 000_B)**

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**0**[1]	**PD**	**WR**			**DLL**	**TM**	**CL**			**BT**	**BL**		
reg. addr			w	w			w	w	w			w	w		

1) A13 is only available for ×4 and ×8 configuration.

Field	Bits	Type[1]	Description
BL	[2:0]	w	**Burst Length** 010 4 011 8
BT	3	w	**Burst Type** 0 Sequential 1 Interleaved
CL	[6:4]	w	**CAS Latency** *Note: All other bit combinations are illegal.* 101 5 110 6
TM	7	w	**Test Mode** 0 Normal mode 1 Vendor specific test mode
DLL	8	w	**DLL Reset** 0 No 1 Yes
WR	[11:9]	w	**Write Recovery**[2] *Note: All other bit combinations are illegal.* 001 2 010 3 011 4 100 5 101 6
PD	12	w	**Active Power-Down Mode Select** 0 Fast exit 1 Slow exit

1) w = write only register bits
2) Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer:
WR[cycles] $\geq t_{WR}(ns) / t_{CK}(ns)$
The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing. $WR_{.MIN}$ is determined by $t_{CK.MAX}$ and $WR_{.MAX}$ is determined by $t_{CK.MIN}$.

2.2.4 DDR2 SDRAM Extended Mode Register Set (EMRS(1))

The Extended Mode Register EMR(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, OCD program, ODT, $\overline{\text{DQS}}$ and output buffers disable, RQDS and $\overline{\text{RDQS}}$ enable. The default value of the extended mode register EMR(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA[2:1] and high on BA0, while controlling the state of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMR(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state..

Table 7 Extended Mode Register Definition(BA[1:0] = 001_B)

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**0**1)	**Q_{off}**	**RDQS**	**$\overline{\text{DQS}}$**	**OCD Program**			**Rtt**	**AL**			**Rtt**	**DIC**	**DLL**
reg. addr				w	w	w			w		w		w	w	w

1) A13 is only available for x4 and x8 commodity configurations.

Field	Bits	Type1)	Description
DLL	0	w	**DLL Enable** 0 Enable 1 Disable
DIC	1	w	**Off-chip Driver Impedance Control** 0 Normal (Driver Size = 100%) 1 Weak (Driver Size = 60%)
R_{TT}	2,6	w	**Nominal Termination Resistance of ODT** *Note: All other bit combinations are illegal.* 00 ∞ (ODT disabled) 10 75 Ohm 01 150 Ohm
AL	[5:3]	w	**Additive Latency** *Note: All other bit combinations are illegal.* 000 0 001 1 010 2 011 3 100 4
OCD Program	[9:7]	w	**Off-Chip Driver Calibration Program** 000 OCD calibration mode exit, maintain setting 001 Drive (1) 010 Drive (0) 100 Adjust mode 111 OCD calibration default
$\overline{\text{DQS}}$	10	w	**Complement Data Strobe ($\overline{\text{DQS}}$, Output)** 0 Enable 1 Disable

Field	Bits	Type[1]	Description (cont'd)
RDQS	11	w	**Read Data Strobe Output (RDQS, $\overline{\text{RDQS}}$)** 0 Disable 1 Enable
Qoff	12	w	**Output Disable** 0 Output buffers enabled 1 Output buffers disabled

1) w = write only register bits

A0 is used for DLL enable or disable. A1 is used for enabling half-strength data-output driver. A2 and A6 enables On-Die termination (ODT) and sets the Rtt value. A[5:3] are used for additive latency settings and A[9:7] enables the OCD impedance adjustment mode. A10 enables or disables the differential DQS and RDQS signals, A11 disables or enables RDQS. Address bit A12 have to be set to 0 for normal operation. With A12 set to 1 the SDRAM outputs are disabled and in Hi-Z. 1 on BA0 and 0 for BA[2:1] have to be set to access the EMRS(1). A13 and all "higher" address bits (including BA2) have to be set to 0 for compatibility with other DDR2 memory products with higher memory densities. Refer to **Table 7**.

Single-ended and Differential Data Strobe Signals

Table 7 lists all possible combinations for DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RQDS}}$ which can be programmed by A[11:10] address bits in EMRS(1). RDQS and $\overline{\text{RDQS}}$ are available in ×8 components only.

If RDQS is enabled in ×8 components, the DM function is disabled. RDQS is active for reads and don't care for writes.

Table 8 Single-ended and Differential Data Strobe Signals

EMRS(1)		Strobe Function Matrix				Signaling
A11 (RDQS Enable)	**A10 ($\overline{\text{DQS}}$ Enable)**	**RDQS/DM**	**$\overline{\text{RDQS}}$**	**DQS**	**$\overline{\text{DQS}}$**	
0 (Disable)	0 (Enable)	DM	Hi-Z	DQS	$\overline{\text{DQS}}$	differential DQS signals
0 (Disable)	1 (Disable)	DM	Hi-Z	DQS	Hi-Z	single-ended DQS signals
1 (Enable)	0 (Enable)	RDQS	$\overline{\text{RDQS}}$	DQS	$\overline{\text{DQS}}$	differential DQS signals
1 (Enable)	1 (Disable)	RDQS	Hi-Z	DQS	Hi-Z	single-ended DQS signals

DLL Enable/Disable

The DLL must be enabled for high speed operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMR(1) is set to 0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current and external load currents.

2.2.5 EMRS(2)

The Extended Mode Registers EMRS(2) and EMRS(3) are reserved for future use and must be programmed when setting the mode register during initialization.

The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be written after Power-up for proper operation.

The extended mode register EMRS(2) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA2, BA0 and high on BA1,while controlling the states of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(2). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state.

EMRS(2) Programming
Extended Mode Register Definition (BA[1:0] = 01$_B$)

<table>
<tr><th>BA1</th><th>BA0</th><th>A13</th><th>A12</th><th>A11</th><th>A10</th><th>A9</th><th>A8</th><th>A7</th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th></tr>
<tr><td>1</td><td>0</td><td colspan="14">0 1)2)</td></tr>
</table>

reg.addr

1) A13 is only available for x4 and x8 commodity configurations.
2) Must be programmed to “0”

2.2.6 EMRS(3)

The Extended Mode Register EMR(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMR(3) Programming
Extended Mode Register Definition (BA[1:0] = 01$_B$)

<table>
<tr><th>BA1</th><th>BA0</th><th>A13</th><th>A12</th><th>A11</th><th>A10</th><th>A9</th><th>A8</th><th>A7</th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th></tr>
<tr><td>1</td><td>1</td><td colspan="14">0 1)2)</td></tr>
</table>

reg. addr

1) A13 is only available for x4 and x8 commodity configurations.
2) Must be programmed to “0”

2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and On Die Termination (ODT) should be carefully controlled depending on system environment.

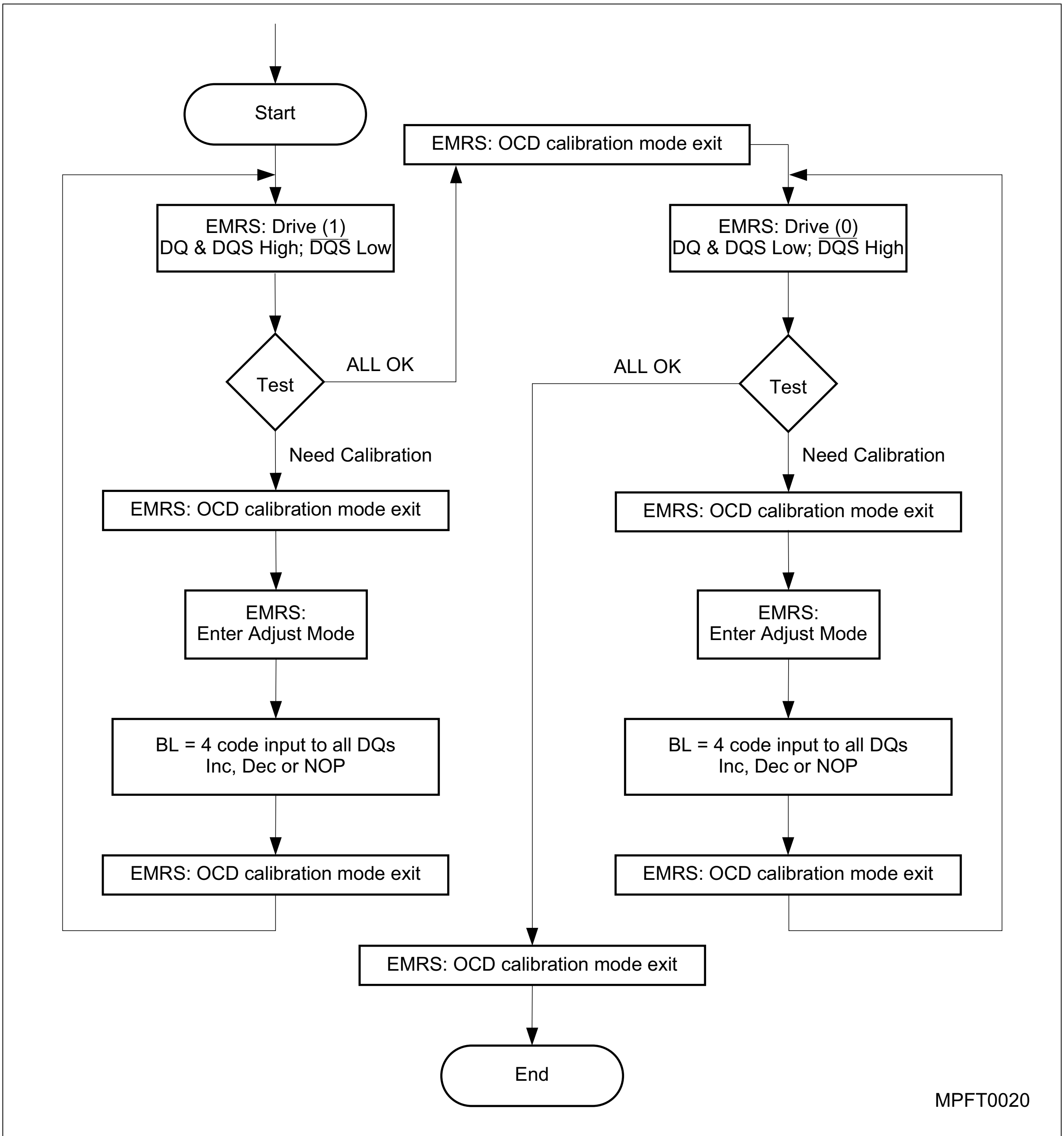


Figure 5 OCD Impedance Adjustment Flow Chart

Note

1. *MR should be set before entering OCD impedance adjustment ODT should be carefully controlled depending on system environment*

2.3.1 Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS(1) mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMR(1) bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven low. In Drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in **Table 10**. OCD applies only to normal full strength output drive setting defined by EMR(1) and if half strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS(1) commands not intended to adjust OCD characteristics must specify A[9:7] as ’000’ in order to maintain the default or calibrated value.

Table 9 Output driver characteristics for OCD calibration

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ ($\overline{RDQS}$) low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and DQS (RDQS) high
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS(1) command along with a 4 bit burst code to DDR2 SDRAM as in **Table 10**. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 in **Table 10** means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the maximum step count range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 10 Off- Chip-Driver Adjust Program

4 bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (no operation)	NOP (no operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Illegal	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and t_{DS} / t_{DH} should be met as Figure 6. Input data pattern for adjustment, DT[0:3] is fixed and not affected by MRS addressing mode (i.e. sequential or interleave). Burst length of 4 have to be programmed in the MRS for OCD impedance adjustment.

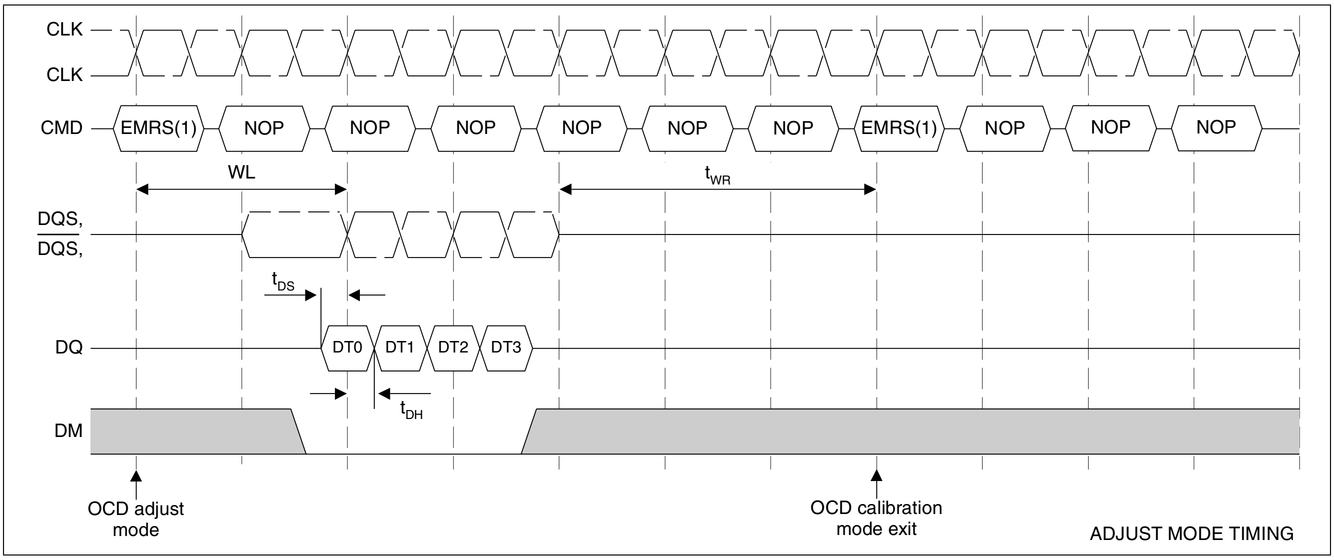


Figure 6 Adjust Mode Timing Diagram

Drive Mode

Both Drive(1) and Drive(0) are used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command. See Figure 7.

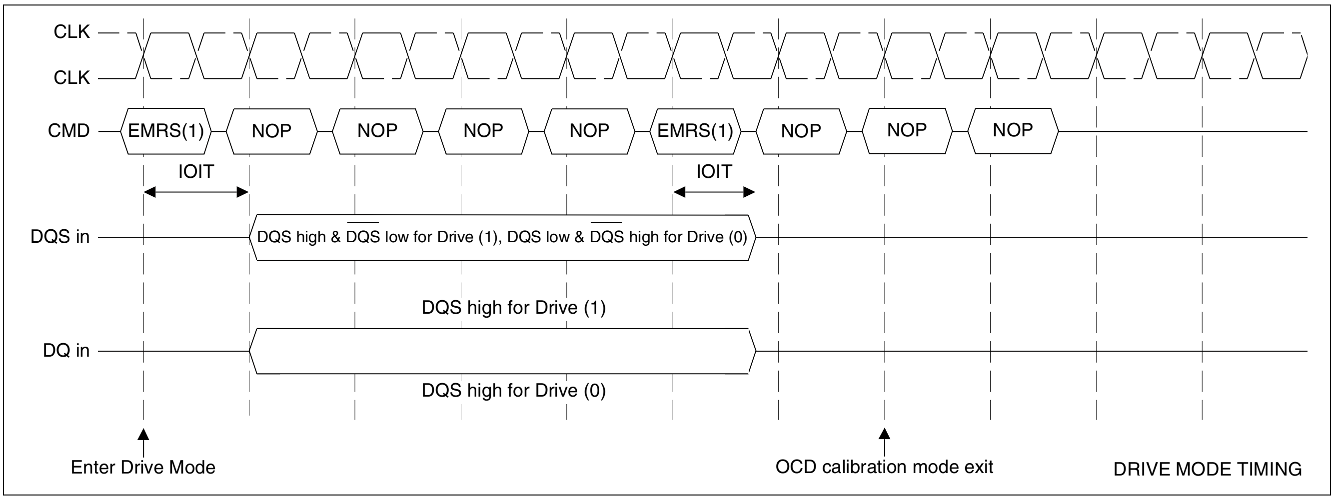


Figure 7 Drive Mode Timing Diagram

2.4 On-Die Termination (ODT)

On-Die Termination (ODT) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$, DM for ×4 and DQ, DQS, $\overline{\text{DQS}}$, DM, RDQS (DM/RDQS share the same pin) and $\overline{\text{RDQS}}$ for ×8 configuration via the ODT control pin. $\overline{\text{DQS}}$ and $\overline{\text{RDQS}}$ are only terminated when enabled by EMR(1).

For ×16 configuration ODT is applied to each DQ, UDQS, $\overline{\text{UDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDM and LDM signal via the ODT control pin. $\overline{\text{UDQS}}$ and $\overline{\text{LDQS}}$ are terminated only when enabled in the EMRS(1) by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

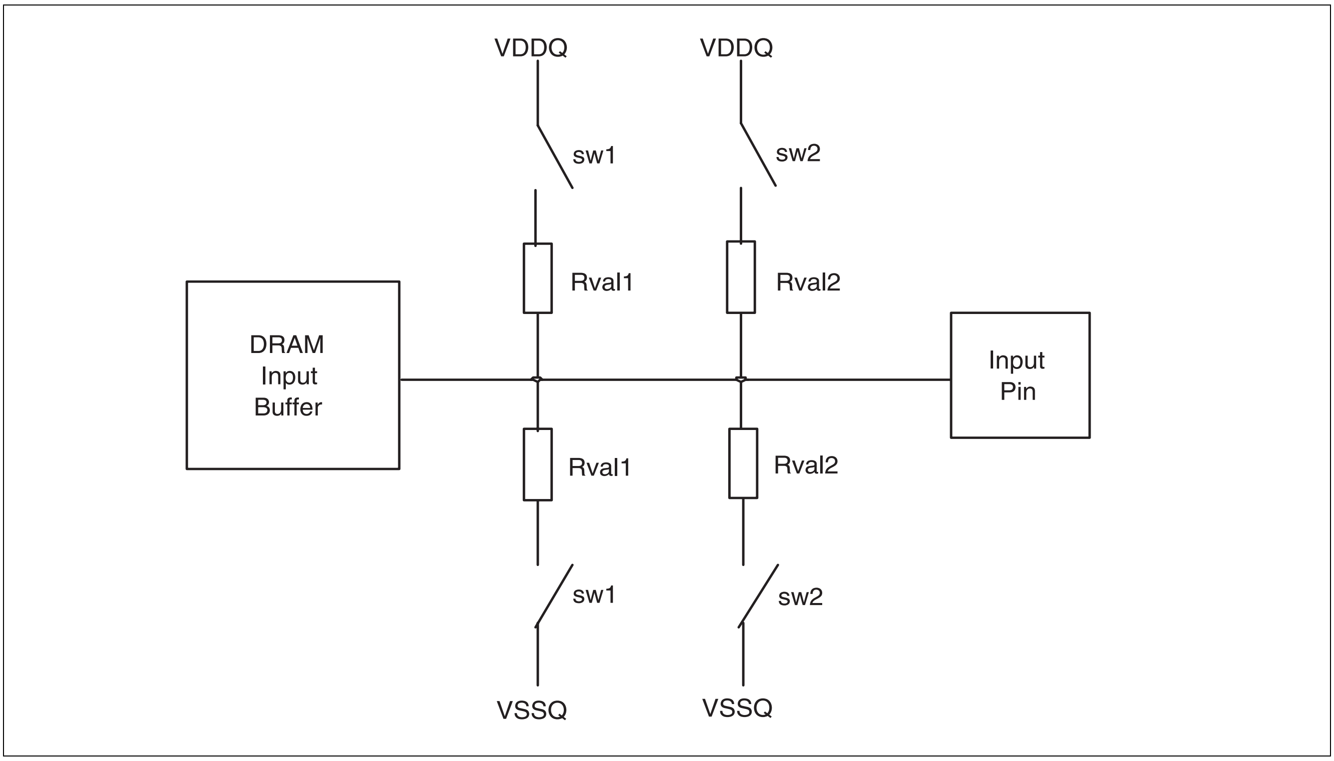


Figure 8 Functional Representation of ODT

Switch sw1 or sw2 is enabled by the ODT pin. Selection between sw1 or sw2 is determined by “Rtt (nominal)” in EMRS(1) address bits A6 & A2.

Target *Rtt = 0.5* × *Rval1* or *0.5* × *Rval2*.

The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.

ODT Truth Tables

The ODT Truth Table shows which of the input pins are terminated depending on the state of address bit A10 and A11 in the EMRS(1). To activate termination of any of these pins, the ODT function has to be enabled in the EMRS(1) by address bits A6 and A2.

Table 11 ODT Truth Table

Input Pin	EMRS(1) Address Bit A10	EMRS(1) Address Bit A11
×16 components		
DQ[15:0]	X	
LDQS	X	
LDQS	0	
UDQS	X	X
UDQS	0	
LDM	X	X
UDM	X	X

Note: X = don’t care; 0 = bit set to low; 1 = bit set to high

ODT timing modes

Depending on the operating mode synchronous or asynchronous ODT timings apply.

Asynchronous ODT timings (t_{AOFPD}, t_{AONPD}) apply when the on-die DLL is disabled.

These modes are:

- Slow Exit Active Power Down Mode (with MRS bit A12 is set to “1”)
- Precharge Power Down Mode

Synchronous ODT timings (t_{AOND}, t_{AOFD}, t_{AON}, t_{AOF}) apply for all other modes.

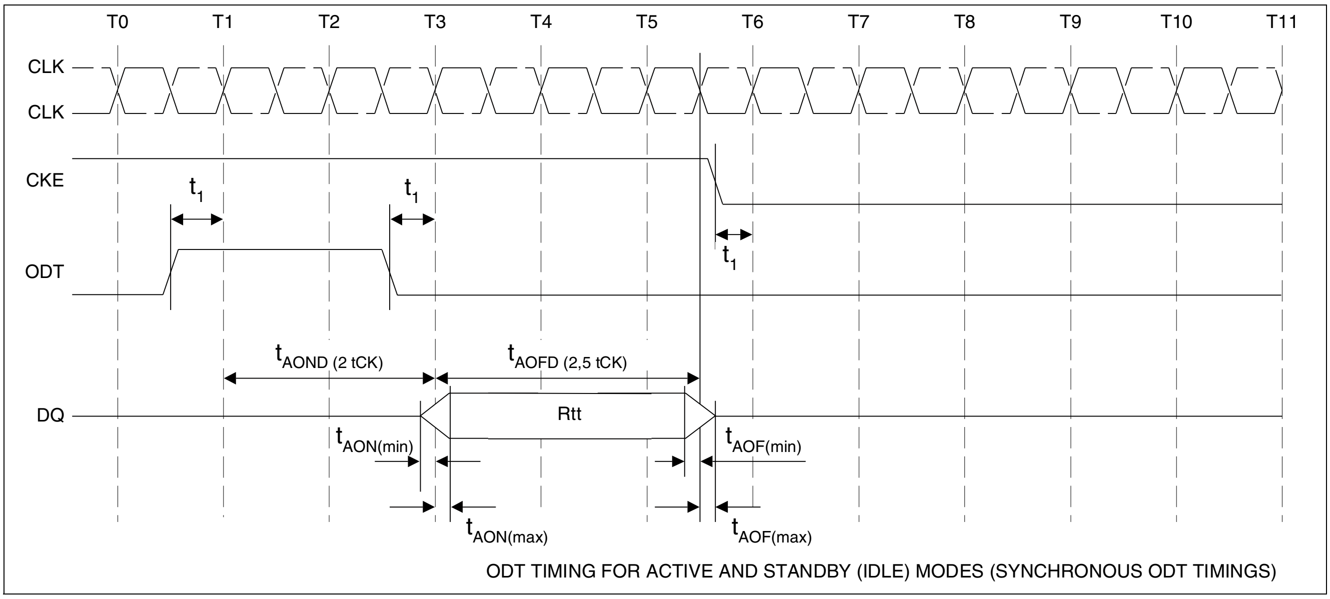


Figure 9 ODT Timing for Active and Standby (Idle) Modes (Synchronous ODT timings)

Note:

1. *Synchronous ODT timings apply for Active Mode and Standby Mode with CKE HIGH and for the "Fast Exit" Active Power Down Mode (MRS bit A12 set to "0"). In all these modes the on-die DLL is enabled.*
2. *ODT turn-on time ($t_{AON,min}$) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. ($t_{AON\,max}$) is when the ODT resistance is fully on. Both are measured from t_{AOND}.*
3. *ODT turn off time min. ($t_{AOF\,min}$) is when the device starts to turn off the ODT resistance.ODT turn off time max. ($t_{AOF\,max}$) is when the bus is in high impedance. Both are measured from t_{AOFD}.*

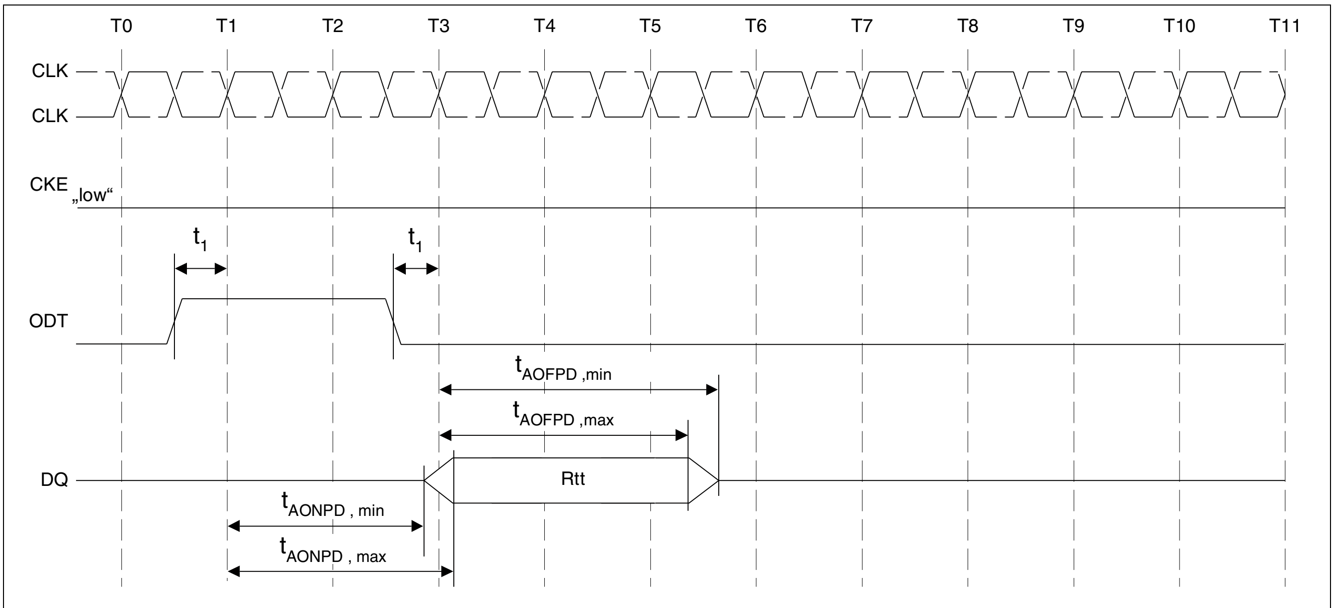


Figure 10 ODT Timing for Precharge Power-Down and Active Power-Down Mode (with slow exit) (Asynchronous ODT timings)

Note: Asynchronous ODT timings apply for Precharge Power-Down Mode and "Slow Exit" Active Power Down Mode (MRS bit A12 set to "1"), where the on-die DLL is disabled in this mode of operation.

Mode entry:

As long as the timing parameter $t_{ANPD,\,min}$ is satisfied when ODT is turned on or off before entering these power-down modes, synchronous timing parameters can be applied. If $t_{ANPD,\,min}$ is not satisfied, asynchronous timing parameters apply.

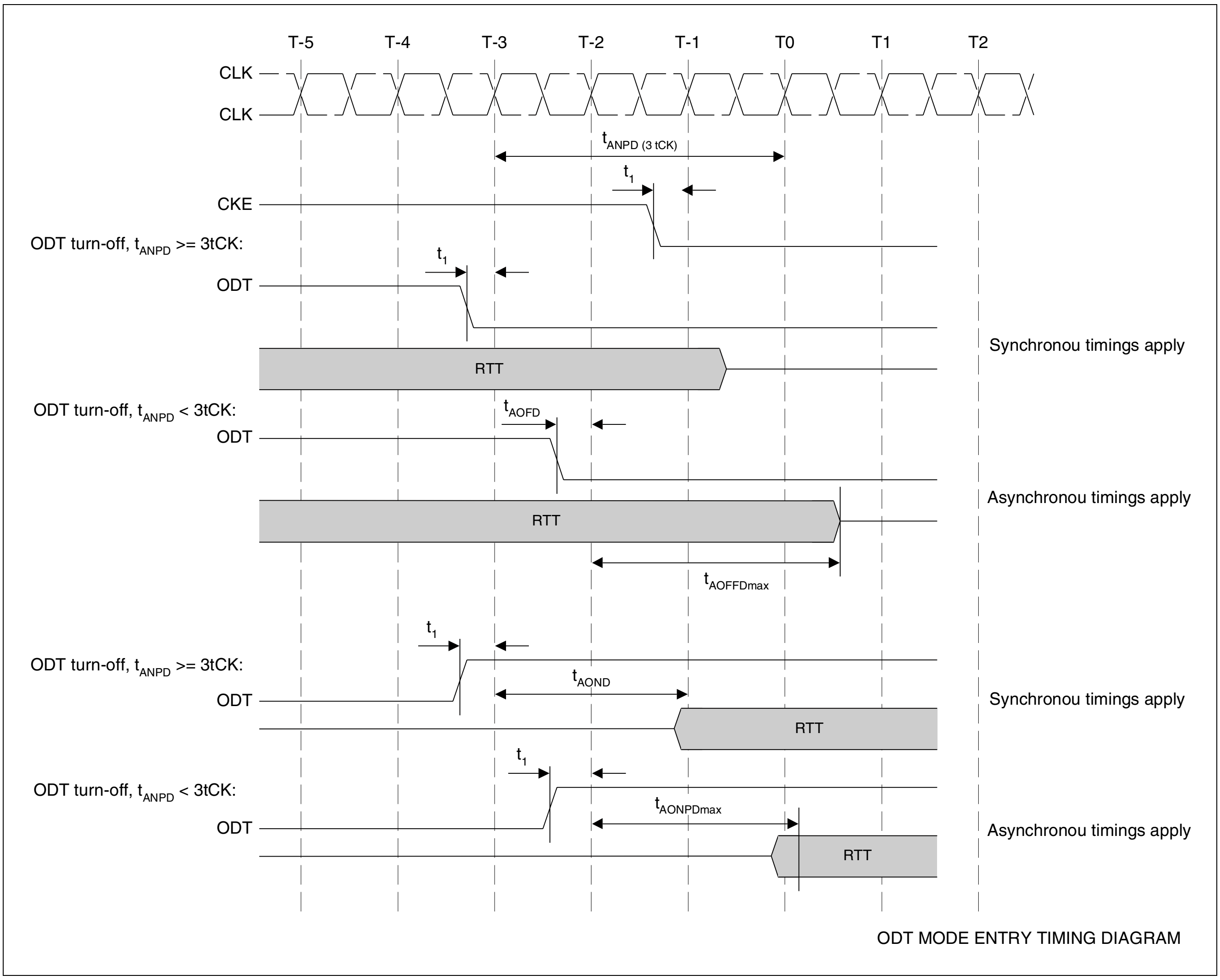


Figure 11 ODT Mode entry Timing Diagram

Mode exit:

As long as the timing parameter $t_{AXPD, min}$ is satisfied when ODT is turned on or off after exiting these power-down modes, synchronous timing parameters can be applied. If $t_{AXPD, min}$ is not satisfied, asynchronous timing parameters apply.

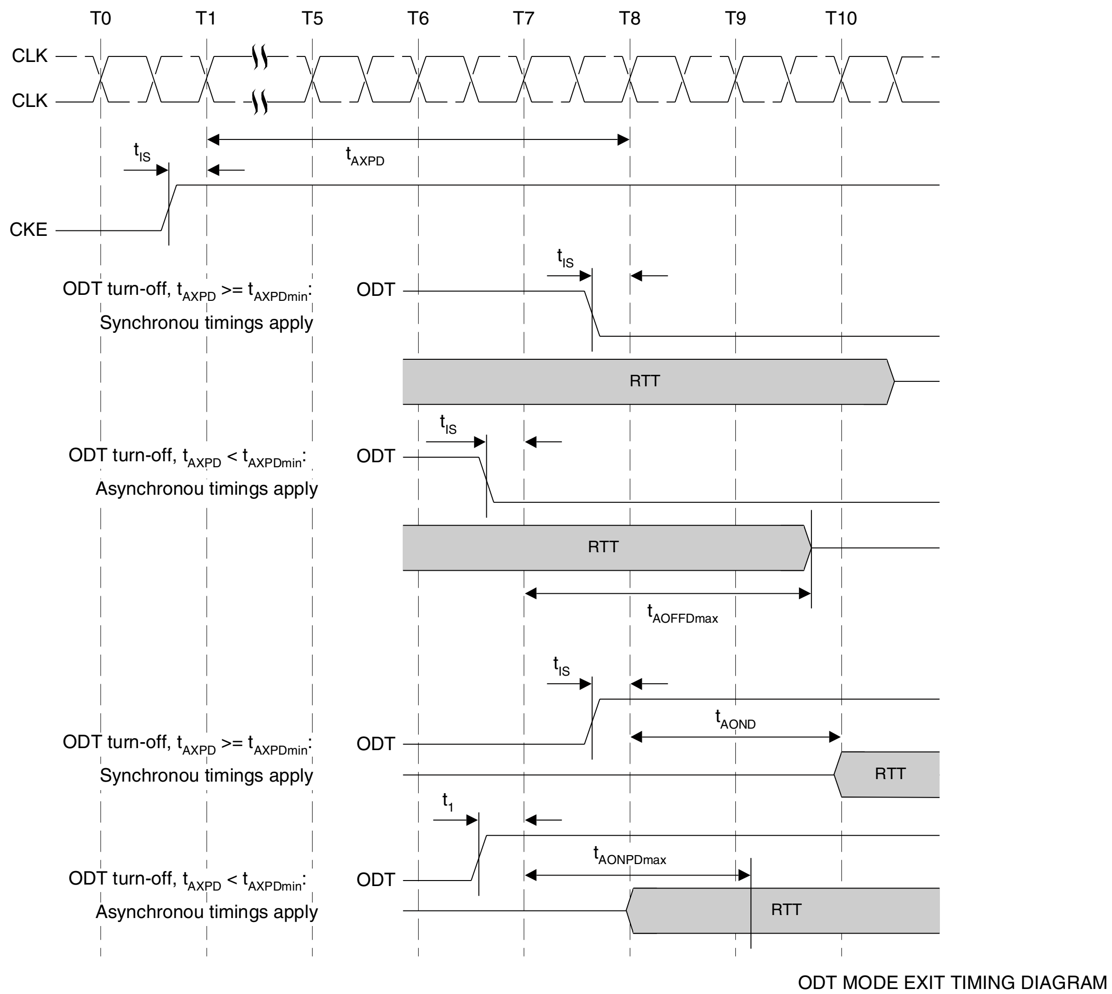


Figure 12 ODT Mode exit Timing Diagram

2.5 Bank Activate Command

The Bank Activate command is issued by holding CAS and WE HIGH with CS and RAS LOW at the rising edge of the clock. The bank addresses BA[1:0][2:0] are used to select the desired bank. The row addresses A0 through A1213 are used to determine which row to activate in the selected bank for ×4 and ×8 organized components. For ×16 components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the $t_{RCD.MIN}$ specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure $t_{RCD.MIN}$ is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by t_{RC}. The minimum time interval between Bank Active commands to different banks is t_{RRD}.

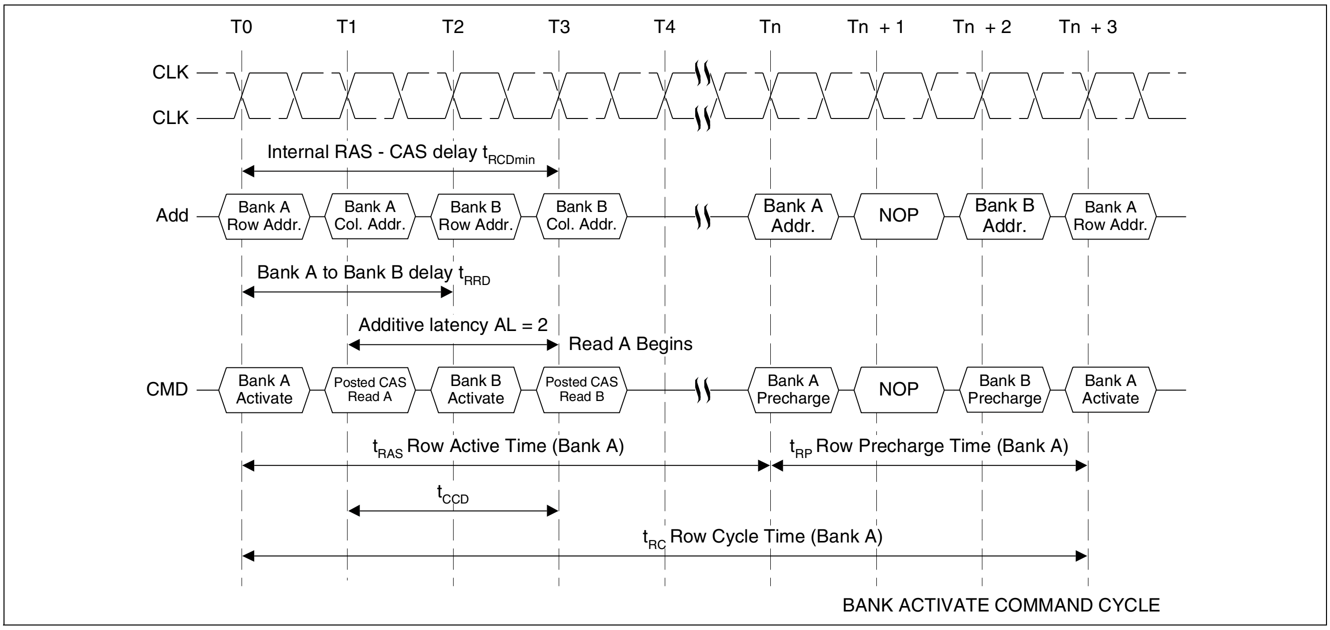


Figure 13 Bank Activate Command Cycle: t_{RCD} = 3, AL = 2, t_{RP} = 3, t_{RRD} = 2

2.6 Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting RAS HIGH, CS and CAS LOW at the clock's rising edge. WE must also be defined at this time to determine whether the access cycle is a read operation (WE HIGH) or a write operation (WE LOW). The DDR2 SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is restricted to specific segments of the page length.

For example, the 16Mbit × 16 chip has a page size of 20481024 kByte which corresponds to a page length of 1024512 bits (defined by CA[8:0]).

In case of a 4-bit burst operation (burst length = 4) the page length of 512 is divided into 128 uniquely addressable segments (4-bits × 1616 I/O each). The 4-bit burst operation will occur entirely within one of the 128 segments (defined by CA[6:0]) starting with the column address supplied to the device during the Read or Write Command (CA[8:0]). The second, third and fourth access will also occur within this segment, however, the burst order is a function of the starting address, and the burst sequence.

In case of a 8-bit burst operation (burst length = 8) the page length of 512 is divided into 64 uniquely addressable segments (8-bits × 16 I/O each). The 8-bit burst operation will occur entirely within one of the 64 segments (defined by CA[5:0]) beginning with the column address supplied to the device during the Read or Write Command (CA[8:0]).

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation (BL = 8) the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) is 4 clocks for read or write cycles.

Burst interruption is allowed with 8 bit burst operation. For details see **Chapter 2.6.6**.

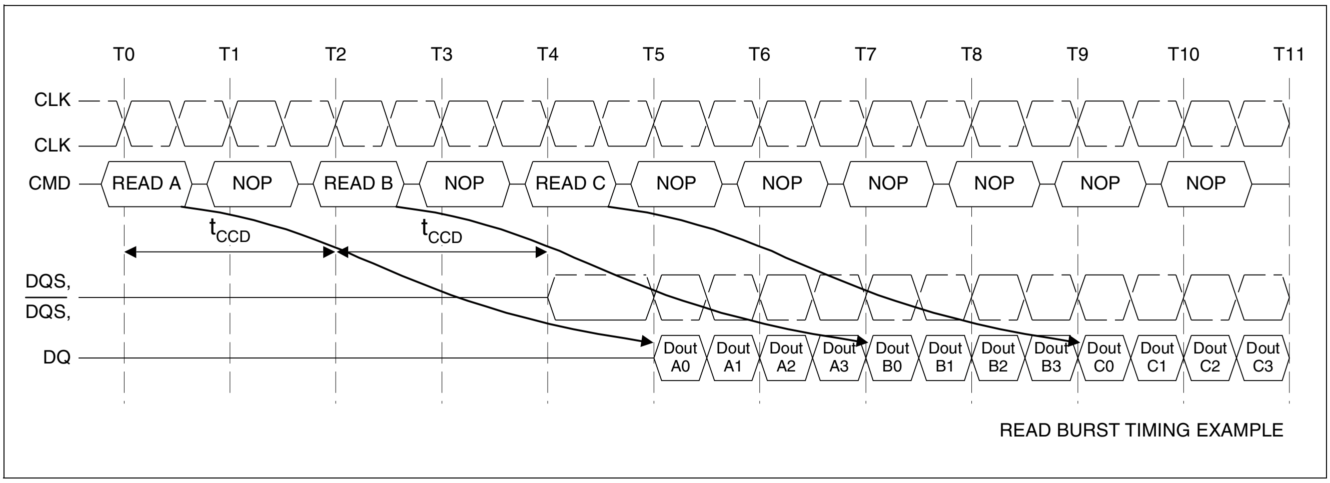


Figure 14 Read Burst Timing Example: (CL = 5, AL = 0, RL = 5, BL = 4)

2.6.1 Posted CAS

Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the RAS bank activate command (or any time during the RAS to CAS delay time, t_{RCD} period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a Read/Write command before the $t_{RCD,\ min}$, then AL greater than 0 must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus CAS latency (RL=AL+CL). If a user chooses to issue a Read command after the $t_{RCD,\ min}$ period, the Read Latency is also defined as RL = AL + CL.

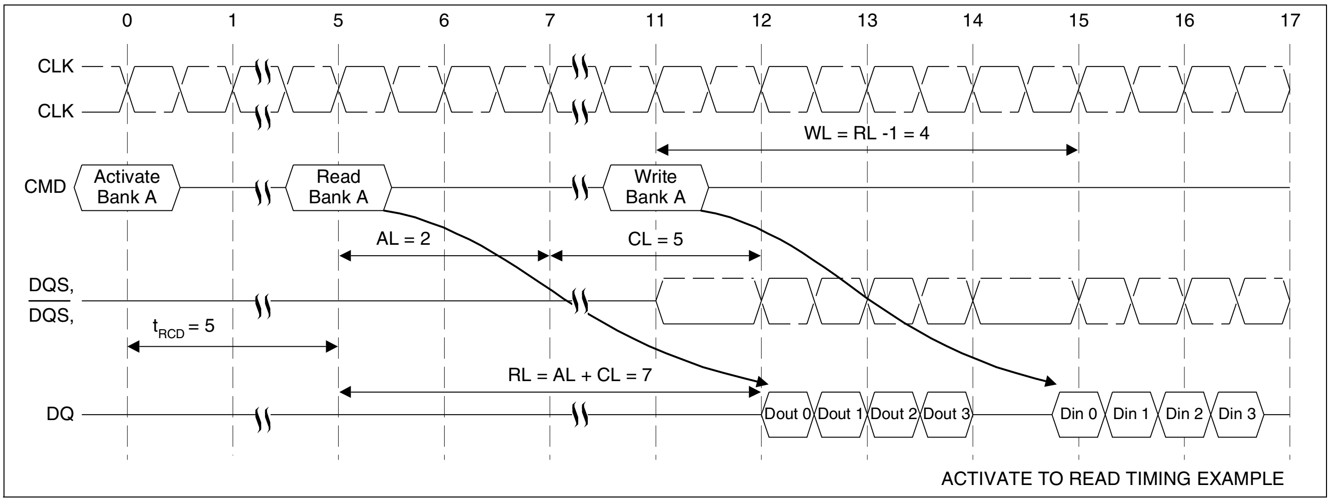


Figure 15 **Activate to Read Timing Example: Read followed by a write to the same bank, Activate to Read delay < t_{RCDmin}: AL = 2 and CL = 5, RL = (AL + CL) = 7, WL = (RL -1) = 6, BL = 4**

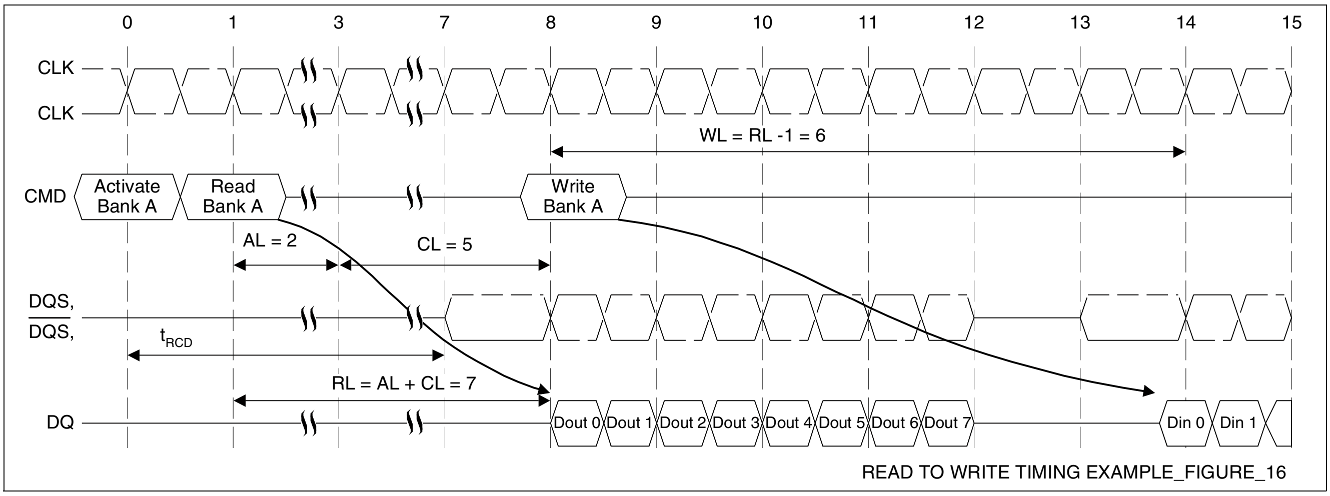


Figure 16 **Read to Write Timing Example: Read followed by a write to the same bank, Activate to Read delay < t_{RCDmin}: AL = 2 and CL = 5, RL = (AL + CL) = 7, WL = (RL -1) = 6, BL = 8**

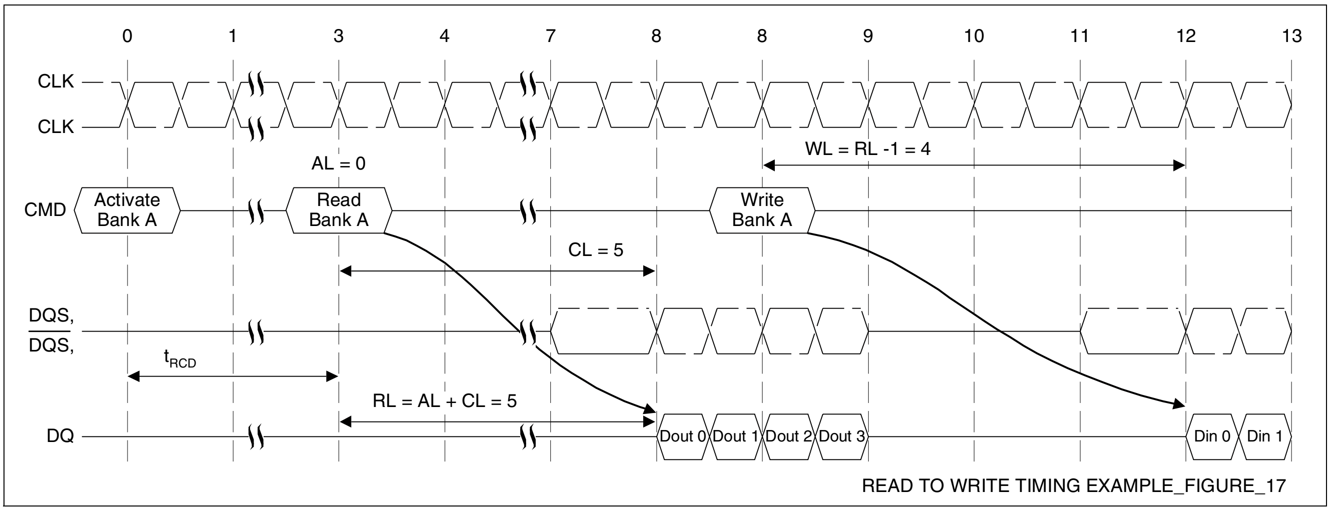


Figure 17 **Read to Write Timing Example: Read followed by a write to the same bank, Activate to Read delay = t_{RCDmin}: AL = 0, CL = 5, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4**

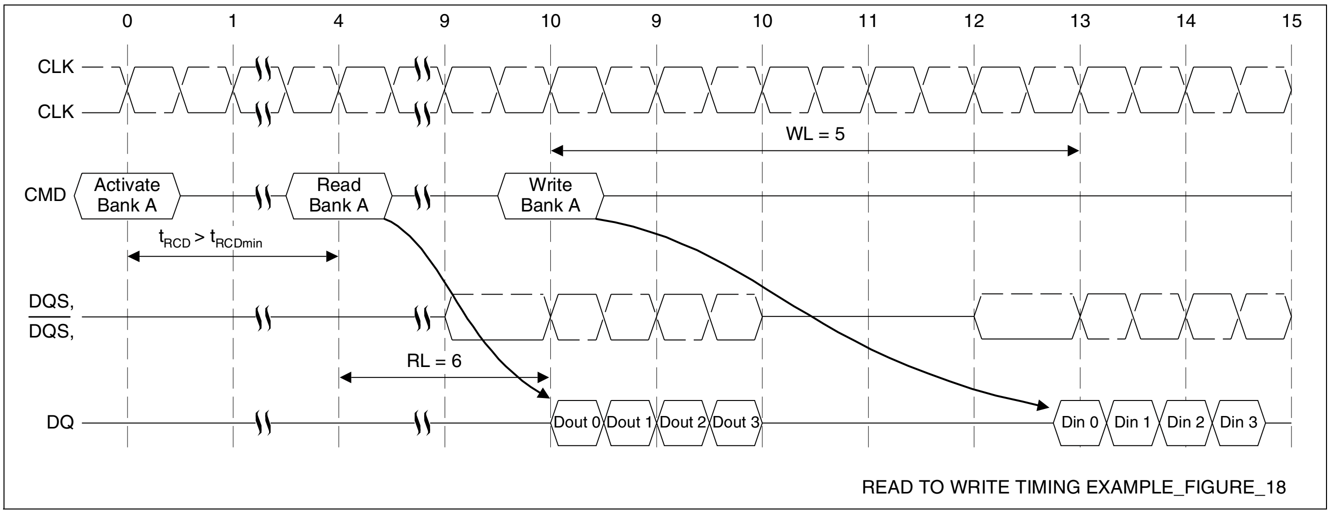


Figure 18 Read to Write Timing Example: Read followed by a write to the same bank, Activate to Read delay > t_{RCDmin}: AL = 1, CL = 5, RL = 6, WL = 5, BL = 4

2.6.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A[2:0] of the MR. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MR. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the **Chapter 2.6.6**. A Burst Stop command is not supported on DDR2 SDRAM devices.

Table 12 Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Notes

– Page size for all 256 Mbit components is 1 kByte*Page Size and Length is a function of I/O organization:* 64 Mb × 16 organization (CA[8:0]); Page Size = 1 kByte; Page Length = 512

4. *Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components*

2.6.3 Read Command

The Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS(1)).

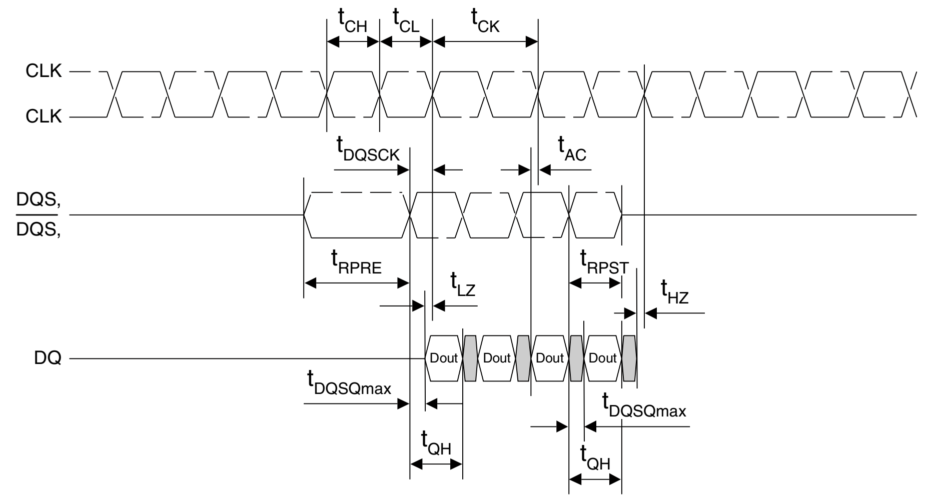


Figure 19 Basic Read Timing Diagram

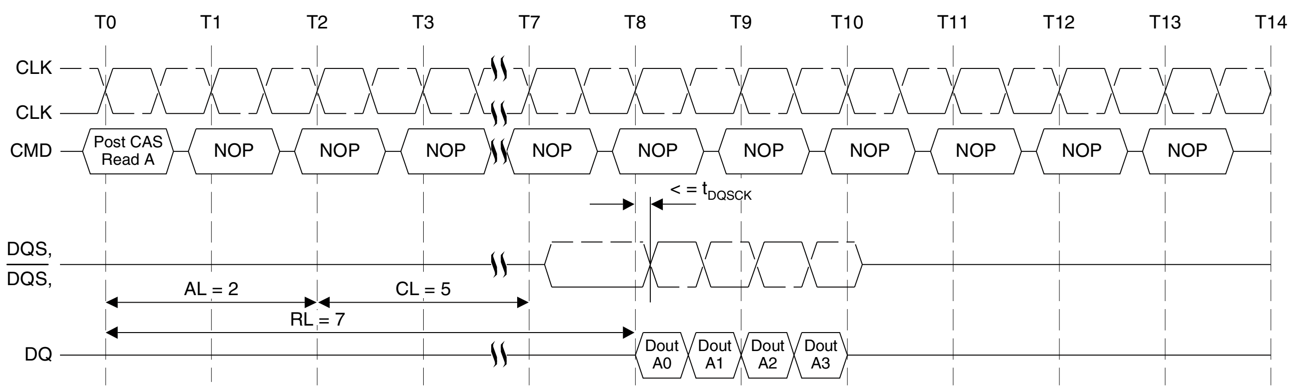


Figure 20 Read Operation Example 1: RL = 7 (AL = 2, CL = 5, BL = 4)

The seamless read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

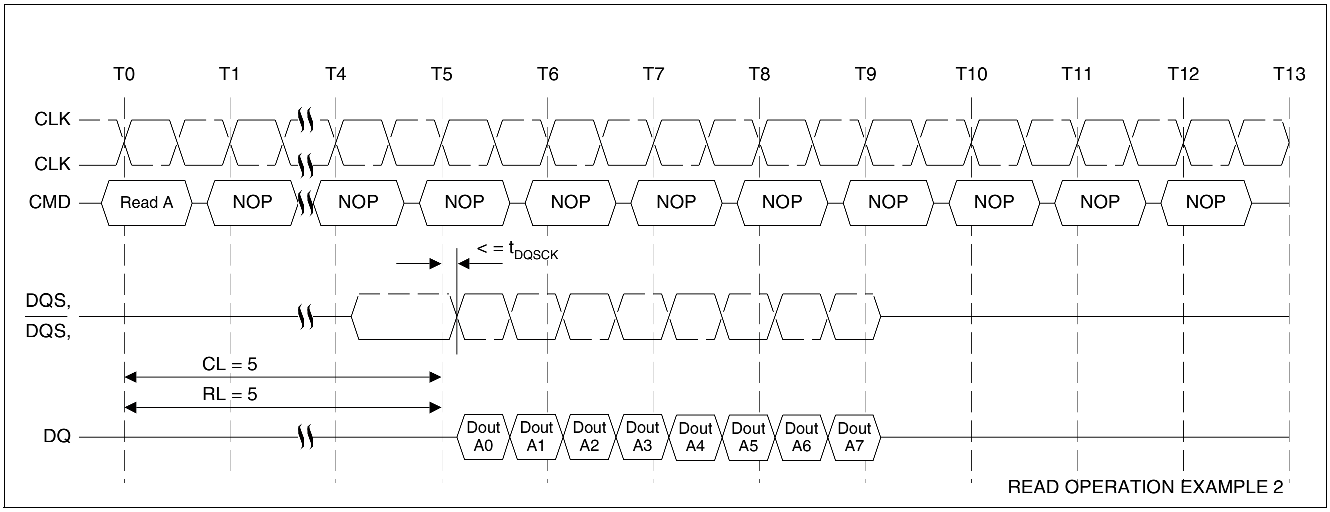


Figure 21 Read Operation Example 2: RL = 5 (AL = 0, CL = 5, BL = 8)

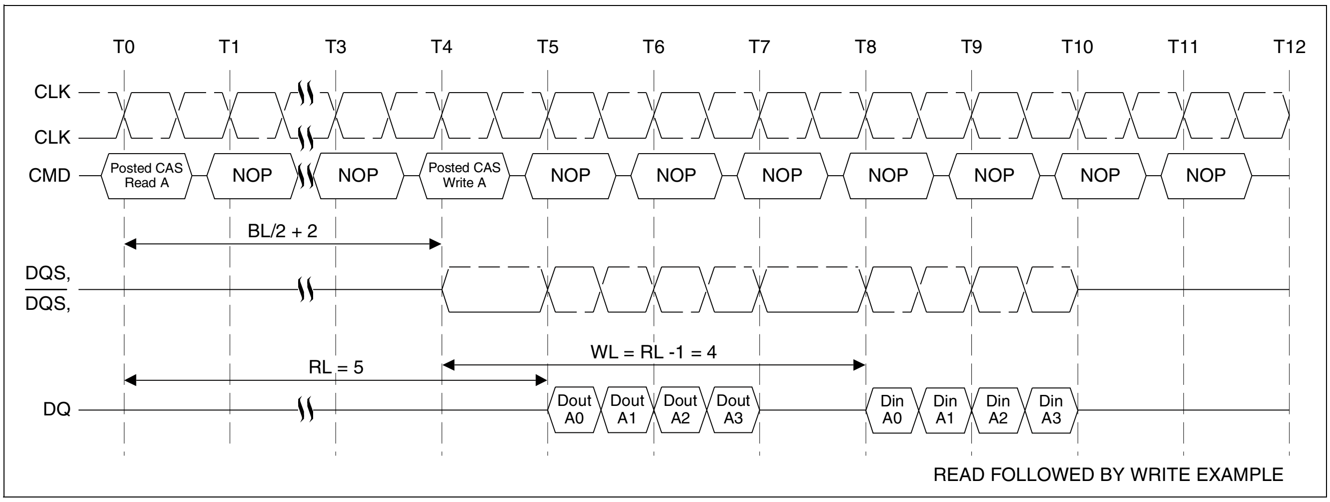


Figure 22 Read followed by Write Example: RL = 5, WL = (RL-1) = 4, BL = 4

The minimum time from the read command to the write command is defined by a read-to-write turn-around time, which is BL/2 + 2 clocks.

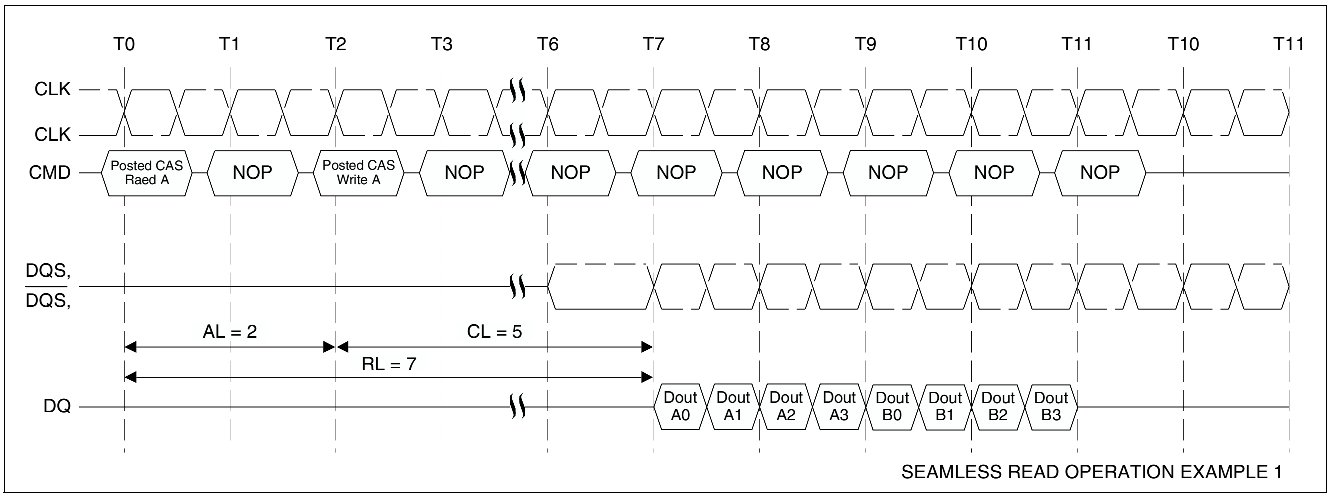


Figure 23 Seamless Read Operation Example 1: RL = 7, AL = 2, CL = 5, BL = 4

The seamless read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

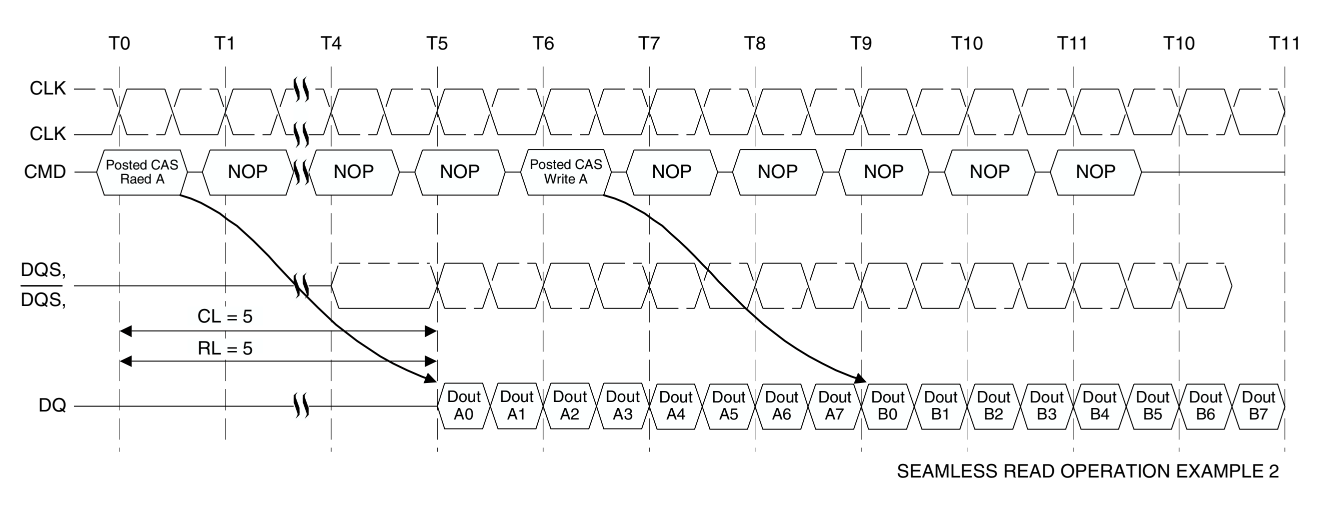


Figure 24 Seamless Read Operation Example 2: RL = 5, AL = 0, CL = 5, BL = 8 (non interrupting)

The seamless, non interrupting 8-bit read operation is supported by enabling a read command at every BL/2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.6.4 Write Command

The Write command is initiated by having CS, CAS and WE low while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL - 1). A data strobe signal (DQS) has to be driven low (preamble) a time t_{WPRE} prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named "write recovery time" (t_{WR}) and is the time needed to store the write data into the memory array. t_{WR} is an analog timing parameter (see **Electrical Characteristics**) and is not the programmed value for WR in the MRS.

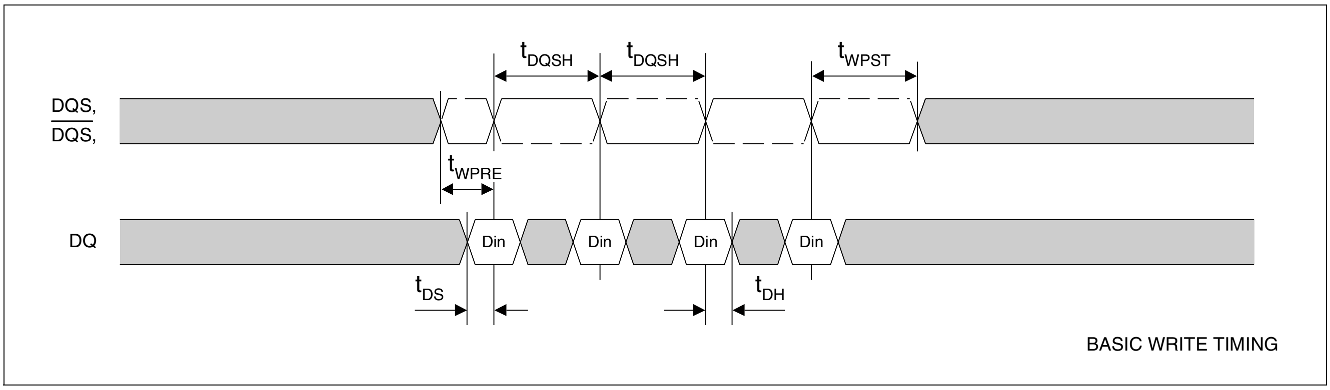


Figure 25 Basic Write Timing

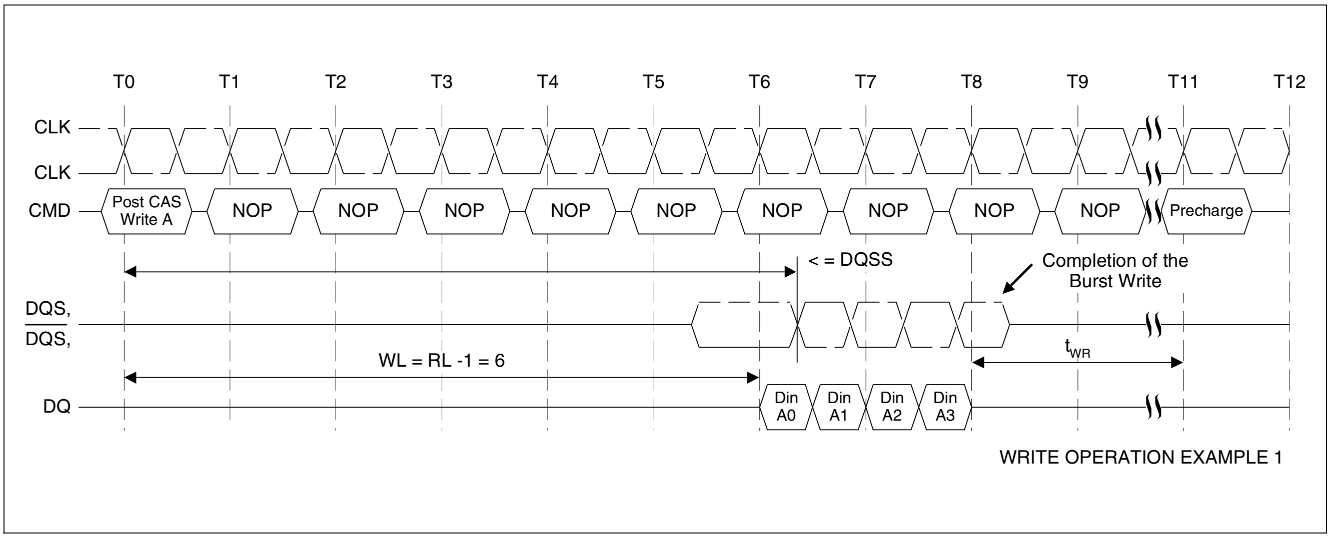


Figure 26 Write Operation Example 1: RL = 7 (AL = 2, CL = 5), WL = 4, BL = 4

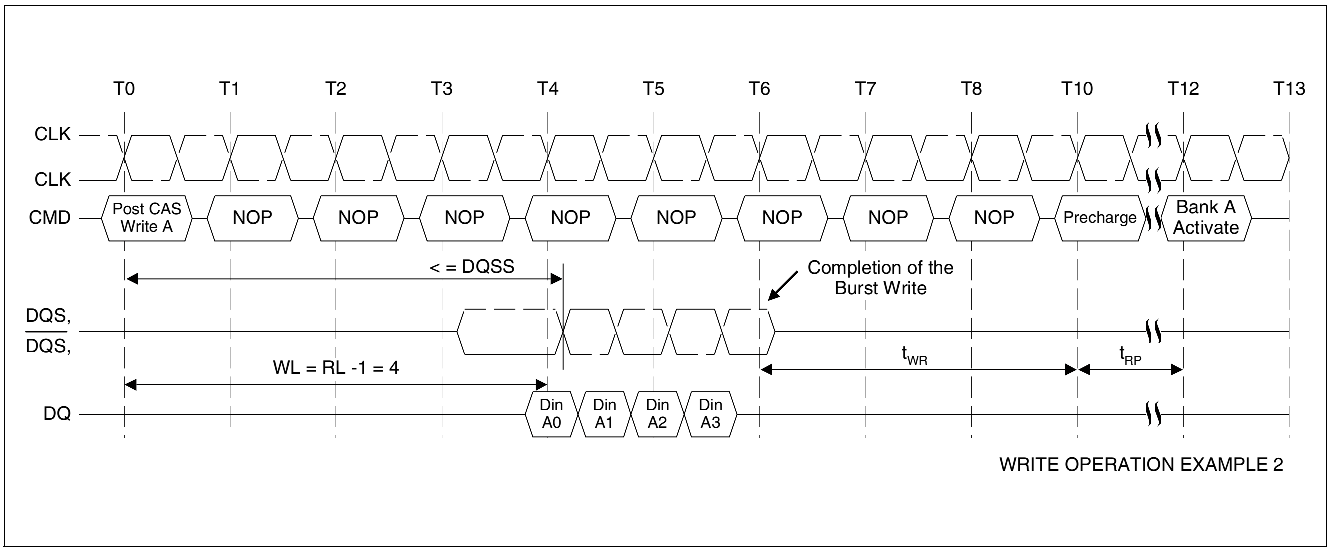


Figure 27 Write Operation Example 2: RL = 5 (AL = 0, CL = 5), WL = 2, BL = 4

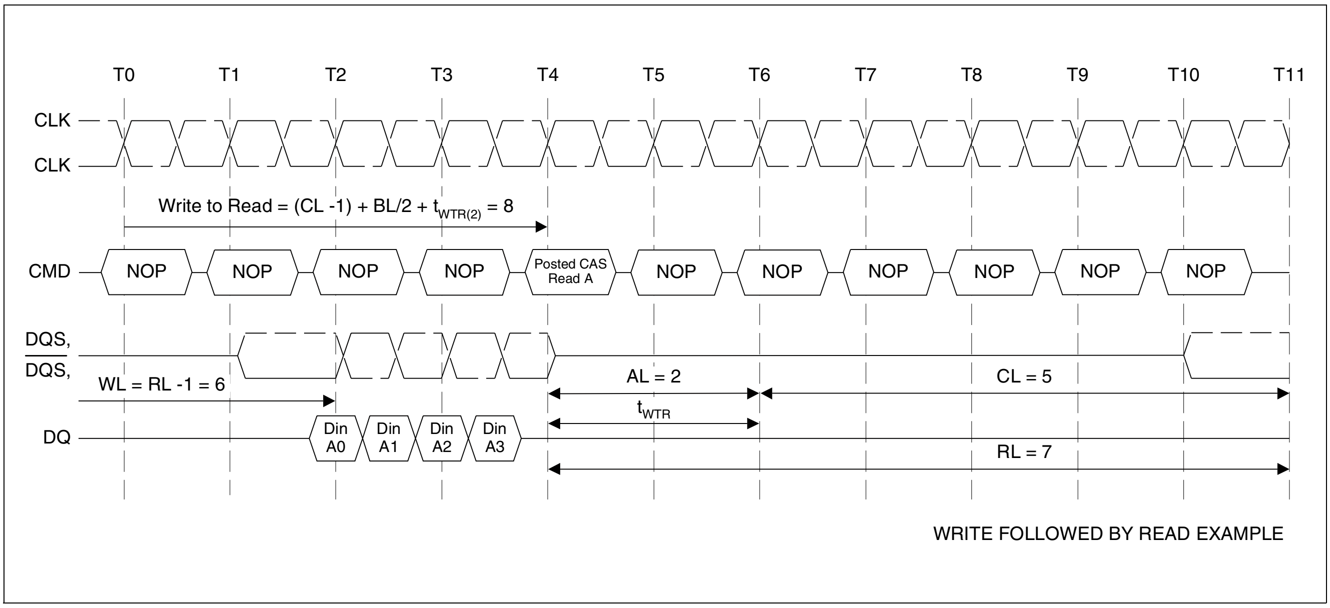


Figure 28 Write followed by Read Example: RL = 7 (AL = 2, CL = 5), WL = 4, t_{WTR} = 2, BL = 4

The minimum number of clocks from the write command to the read command is (CL - 1) +BL/2 + t_{WTR}, where t_{WTR} is the write-to-read turn-around time t_{WTR} expressed in clock cycles. The t_{WTR} is not a write recovery time (t_{WR}) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

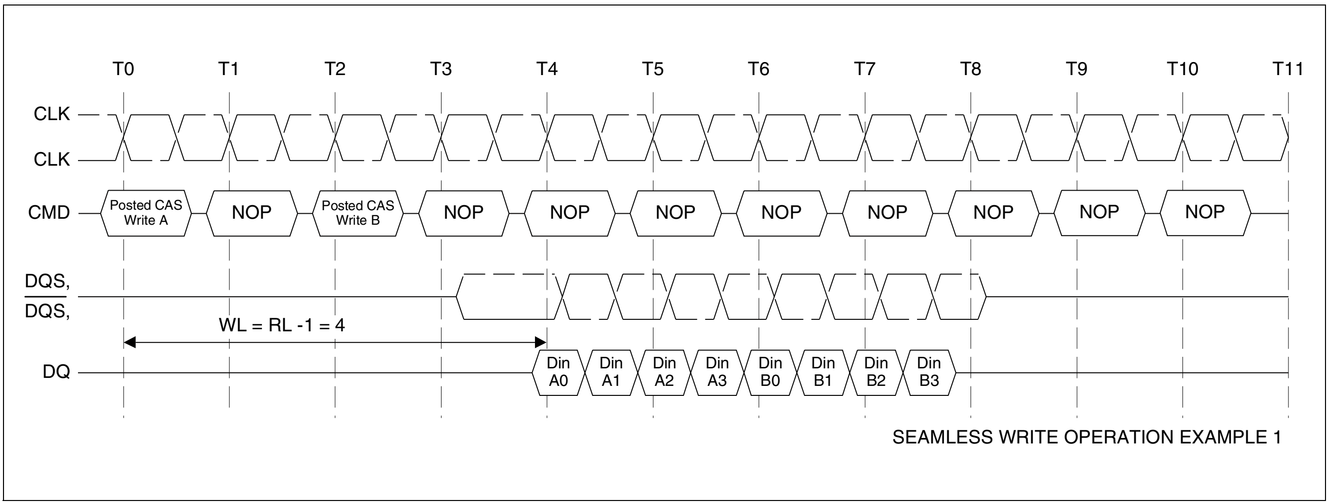


Figure 29 Seamless Write Operation Example 1: RL = 5, WL = 4, BL = 4

The seamless write operation is supported by enabling a write command every BL/2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

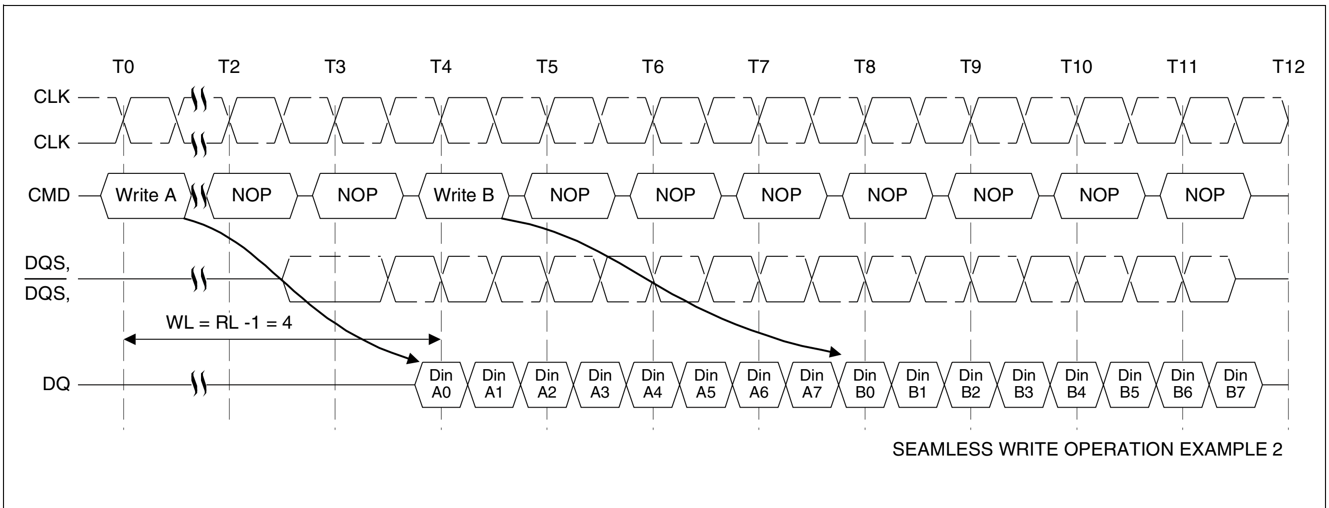


Figure 30 Seamless Write Operation Example 2: RL = 3, WL = 4, BL = 8, non interrupting

The seamless, non interrupting 8-bit burst write operation is supported by enabling a write command at every BL/2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.6.5 Write Data Mask

Two write data mask inputs (LDM, UDM)are supported on DDR2 SDRAM's , consistent with the implementation on DDR SDRAM's. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. Data mask is not used during read cycles. If DM is high during a write burst coincident with the write data, the write data bit is not written to the memory.

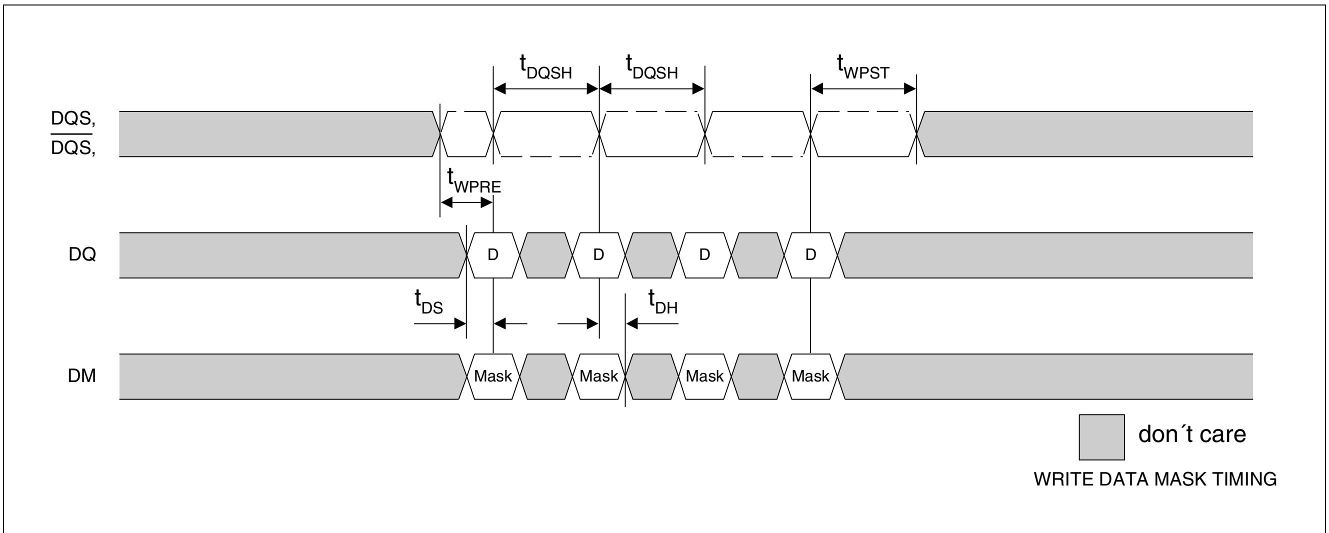


Figure 31 Write Data Mask Timing

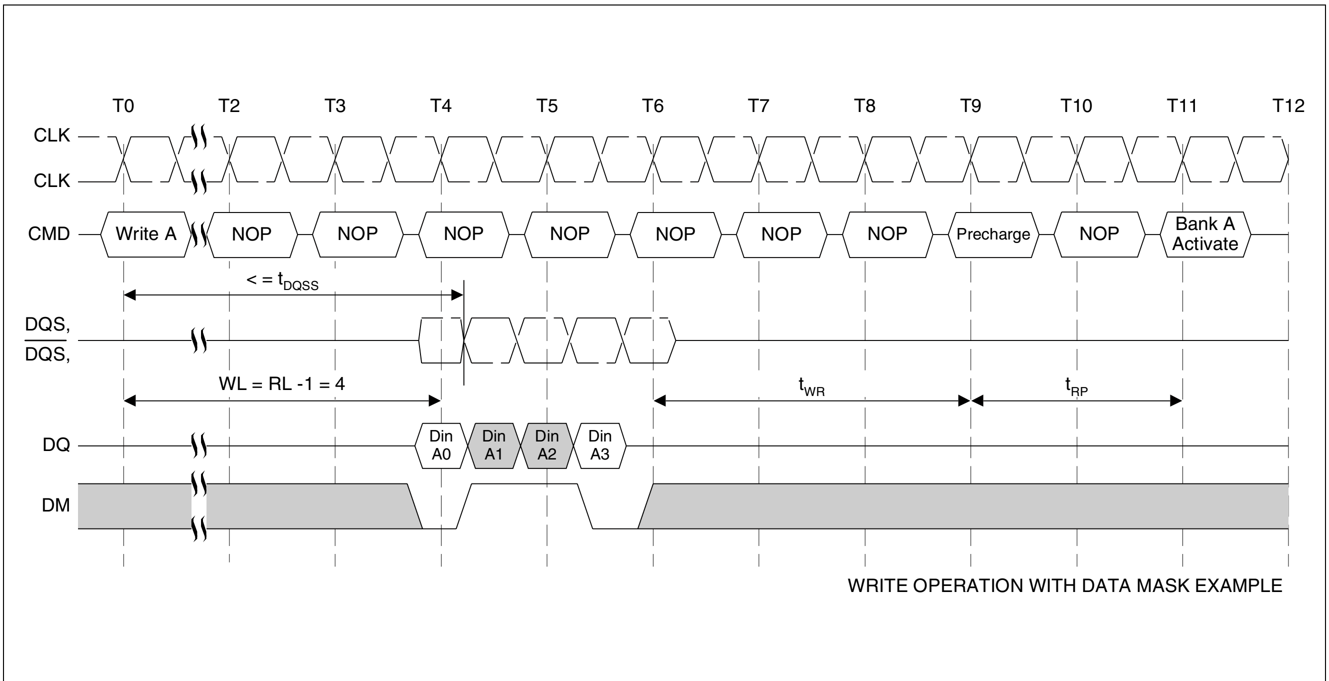


Figure 32 Write Operation with Data Mask Example: RL = 5 (AL = 0, CL = 5), WL = 4, t_{WR} = 3, BL = 4

2.6.6 Burst Interruption

Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. A Read Burst can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.
2. A Write Burst can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.
3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.
5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.
7. Read burst interruption is allowed by a Read with Auto-Precharge command.
8. Write burst interruption is allowed by a Write with Auto-Precharge command.
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + t_{WR}, where t_{WR} starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

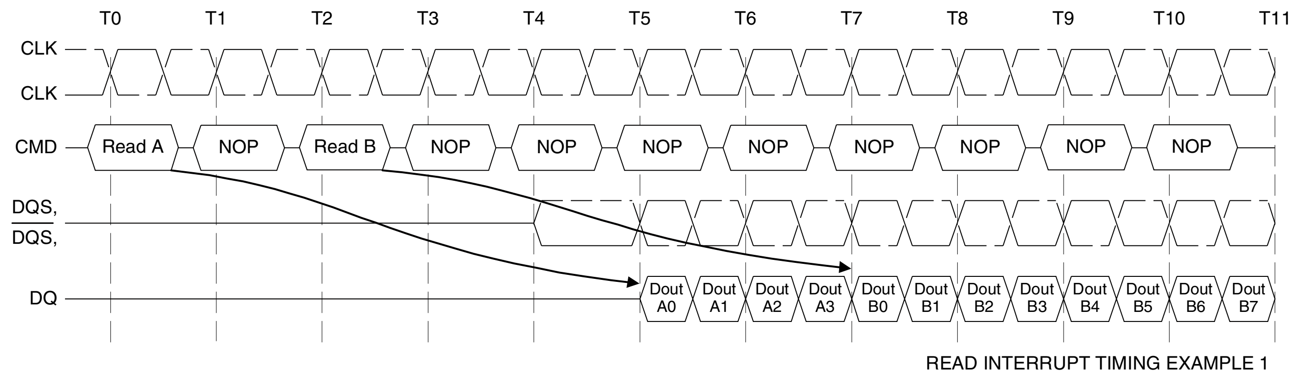


Figure 33 Read Interrupt Timing Example 1: (CL = 5, AL = 0, RL = 5, BL = 8)

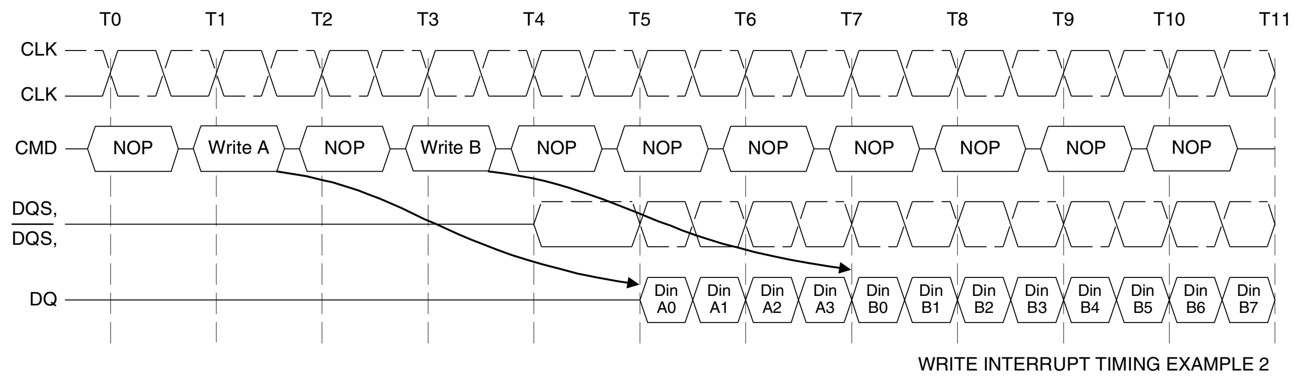


Figure 34 Write Interrupt Timing Example 2: (CL = 5, AL = 0, WL = 4, BL = 8)

2.7 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA[2:1] are used to define which bank to precharge when the command is issued.

Table 13 Bank Selection for Precharge by Address Bits

A10	BA0	BA1	Precharge Bank(s)
LOW	0	0	Bank 0 only
LOW	0	1	Bank 1 only
LOW	1	0	Bank 2 only
LOW	1	1	Bank 3 only
HIGH	Don't Care	Don't Care	all banks

Note: The bank address assignment is the same for activating and precharging a specific bank.

2.7.1 Read Operation Followed by a Precharge

The following rules apply as long as the t_{RTP} timing parameter - Internal Read to Precharge Command delay time - is less or equal two clocks, which is the case for operating frequencies less or equal 266 Mhz (DDR2 400 and 533 speed sorts):

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 clocks. For the earliest possible precharge, the Precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 clocks" after a Read Command, as long as the minimum t_{RAS} timing is satisfied.

A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The RAS precharge time (t_{RP}) has been satisfied from the clock at which the precharge begins.
2. The RAS cycle time ($t_{RC, min}$) from the previous bank activation has been satisfied.

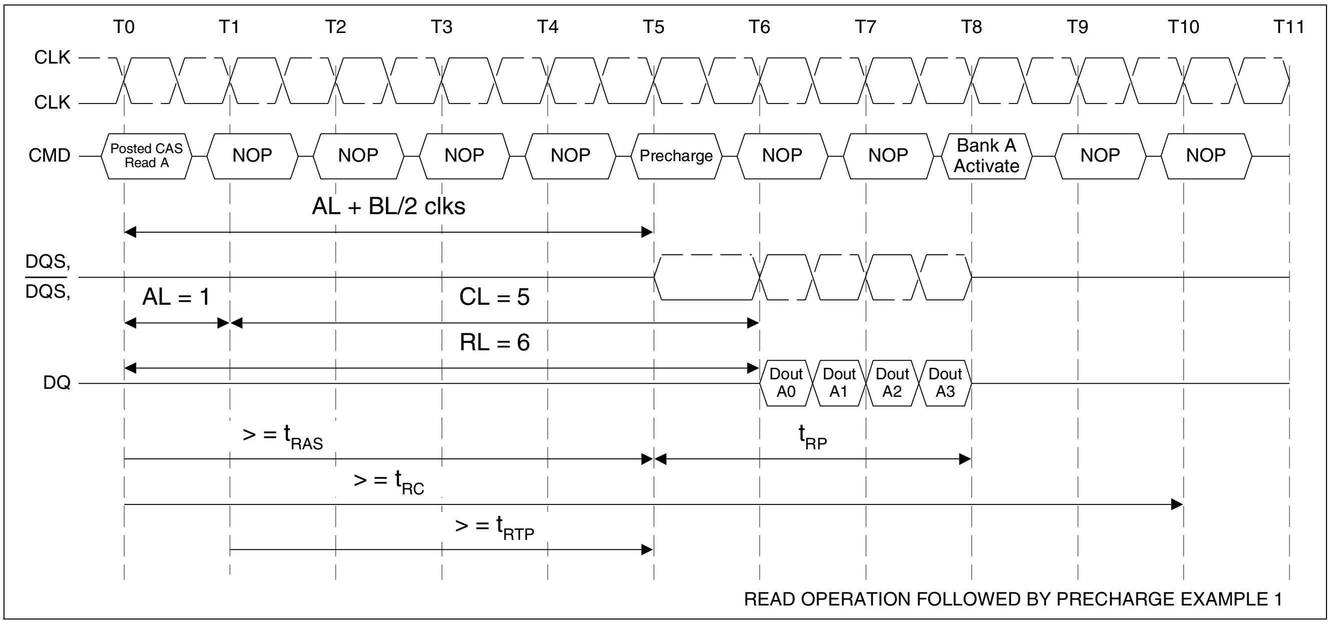


Figure 35 Read Operation Followed by Precharge Example 1: RL = 6 (AL = 1, CL = 5), BL = 4, $t_{RTP} \leq 2$ clocks

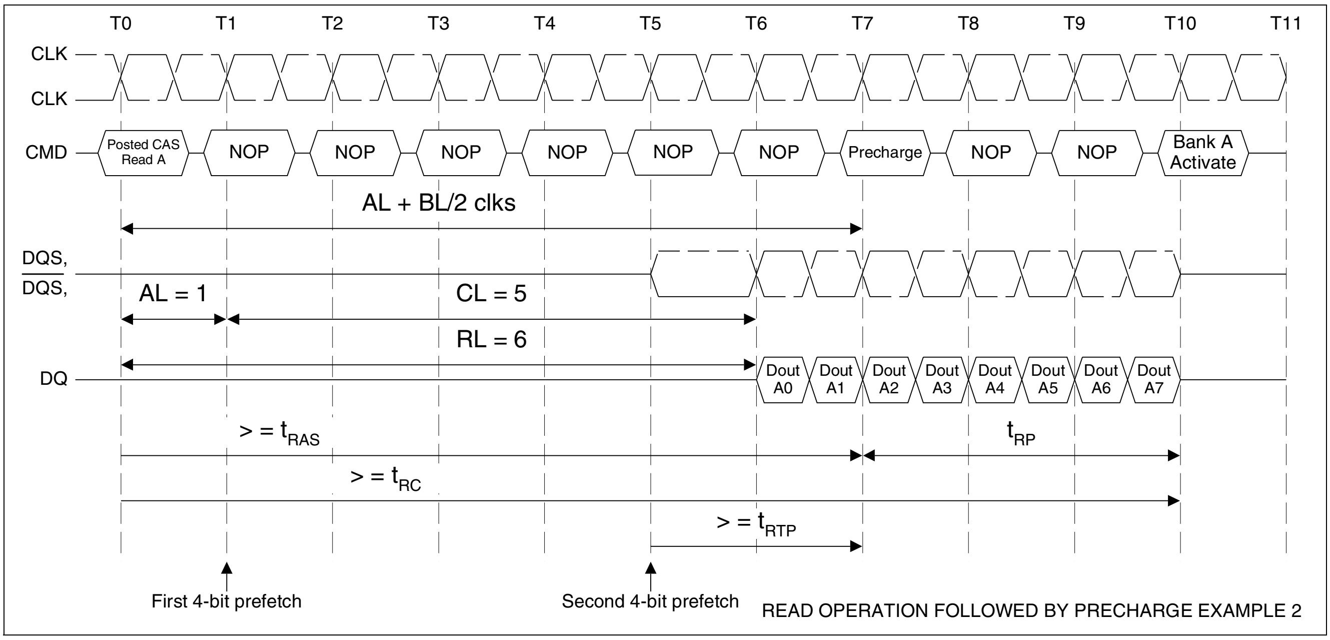


Figure 36 Read Operation Followed by Precharge Example 2: RL = 6 (AL = 1, CL = 5), BL = 8, $t_{RTP} \leq$ 2 clocks

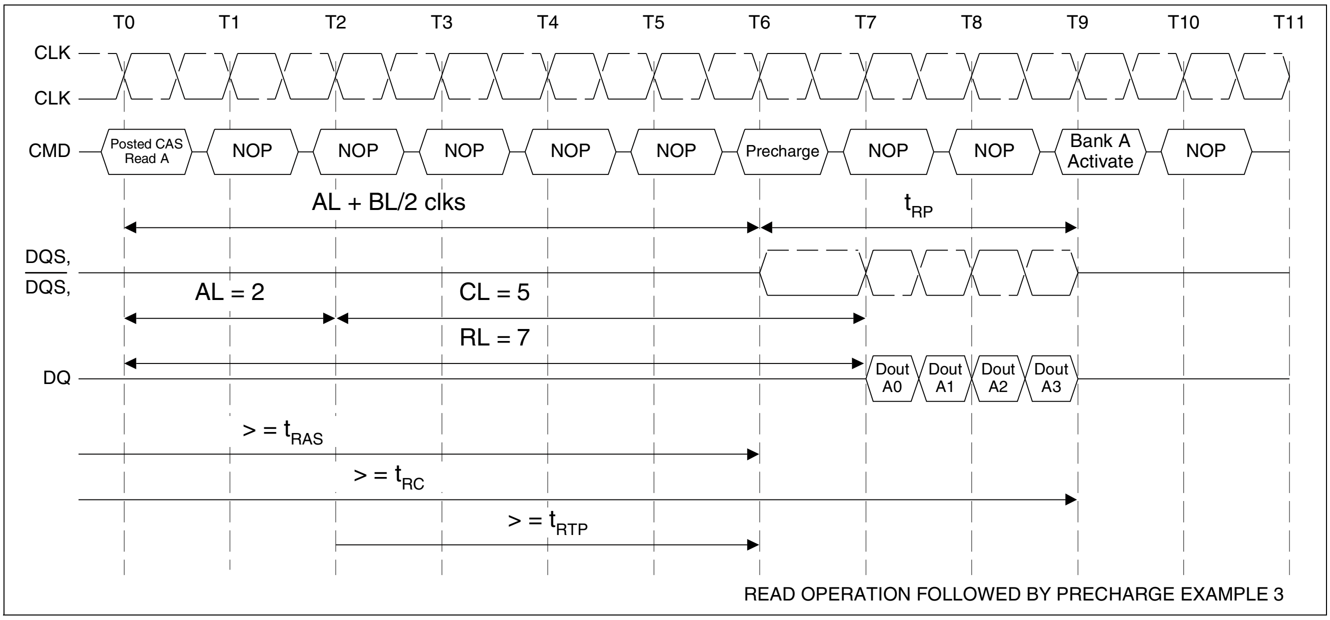


Figure 37 Read Operation Followed by Precharge Example 3: RL = 7 (AL = 2, CL = 5), BL = 4, $t_{RTP} \leq$ 2 clocks

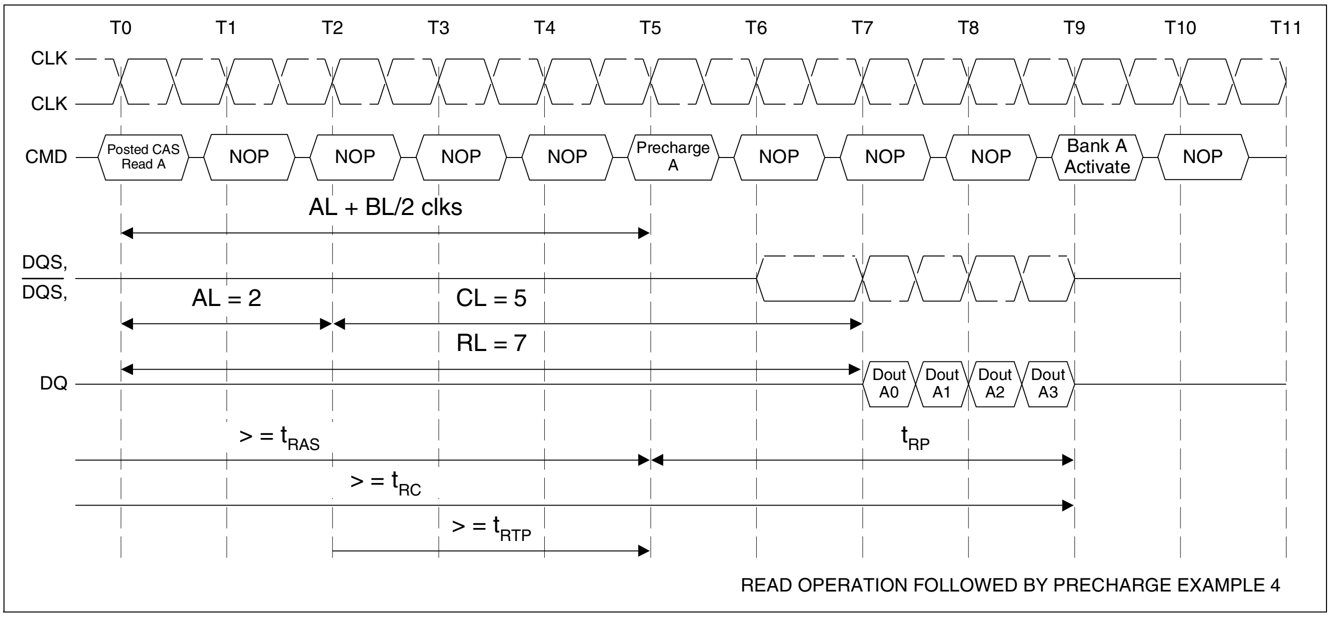


Figure 38 Read Operation Followed by Precharge Example 4: RL = 7, (AL = 2, CL = 5), BL = 4, $t_{RTP} \leq 2$ clocks

2.7.2 Write followed by Precharge

Minimum Write to Precharge command spacing to the same bank = WL + BL/2 + t_{WR}. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. t_{WR} is an analog timing parameter (see **Chapter 7**) and is not the programmed value for WR in the MRS.

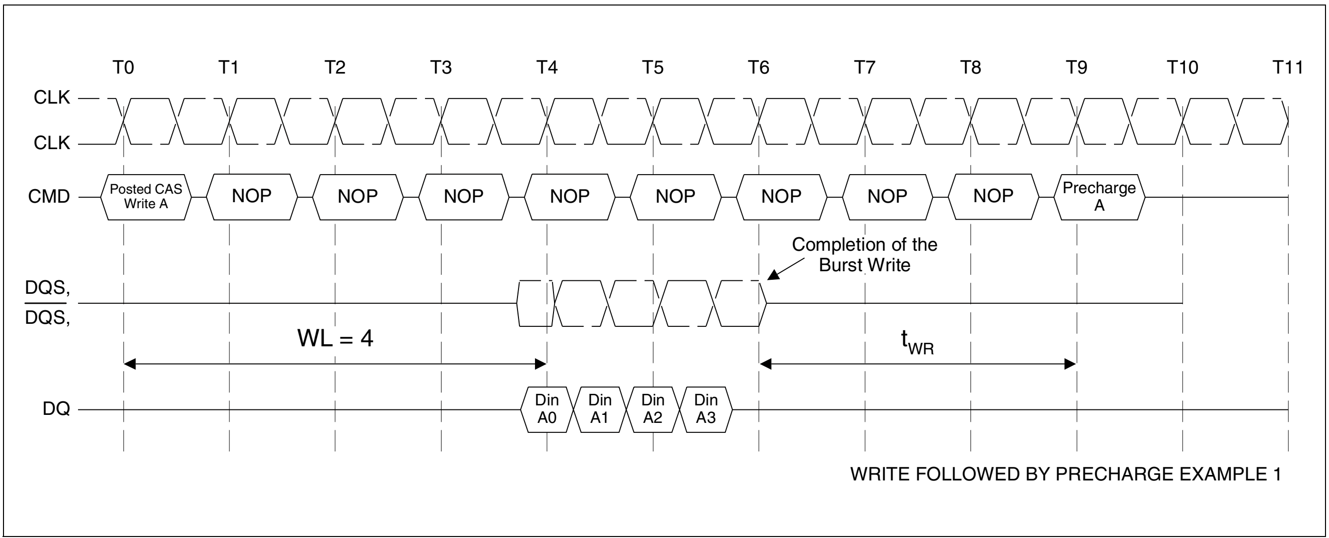


Figure 39 Write followed by Precharge Example 1: WL = (RL - 1) = 4, BL = 4, t_{WR} = 3

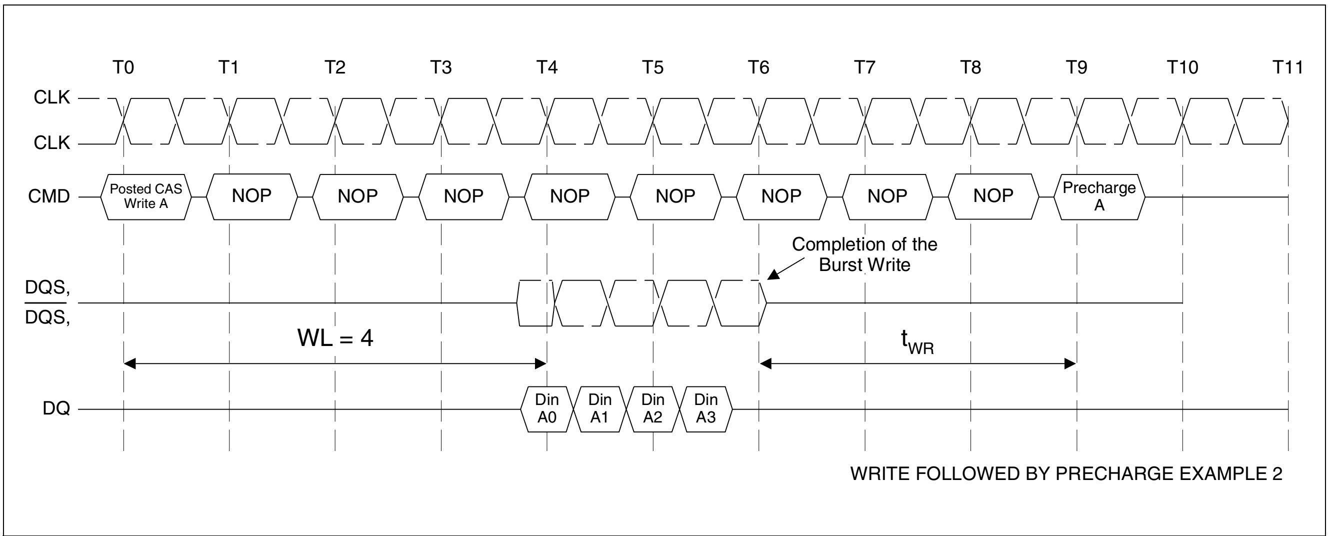


Figure 40 Write followed by Precharge Example 2: WL = (RL - 1) = 4, BL = 4, t_{WR} = 3

2.8 Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then the Auto-Precharge function is enabled.

During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is $\overline{CAS}$ Latency (CL) clock cycles before the end of the read burst.

Auto-Precharge is also implemented for Write Commands.The precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ Latency) thus improving system performance for random data access.

The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

2.8.1 Read with Auto-Precharge

If A10 is 1 when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if $t_{RAS(min)}$ and t_{RTP} are satisfied. If $t_{RAS(min)}$ is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until $t_{RAS(min)}$ is satisfied. If t_{RTPmin} is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RTPmin} is satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + t_{RTP} + t_{RP}. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + t_{RTP} + t_{RP}. Note that (t_{RTP} + t_{RP}) has to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The RAS precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.
2. The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

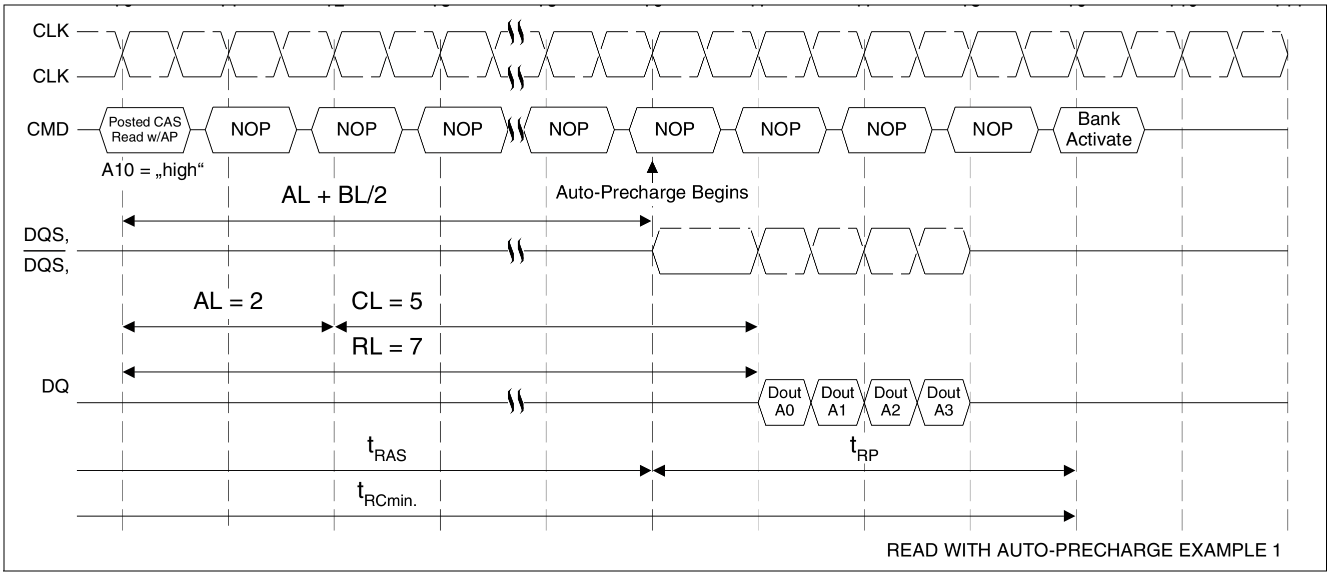


Figure 41 Read with Auto-Precharge Example 1, followed by an Activation to the Same Bank (t_{RC} Limit): RL = 7 (AL = 2, CL = 5), BL = 4, $t_{RTP} \leq 2$ clocks

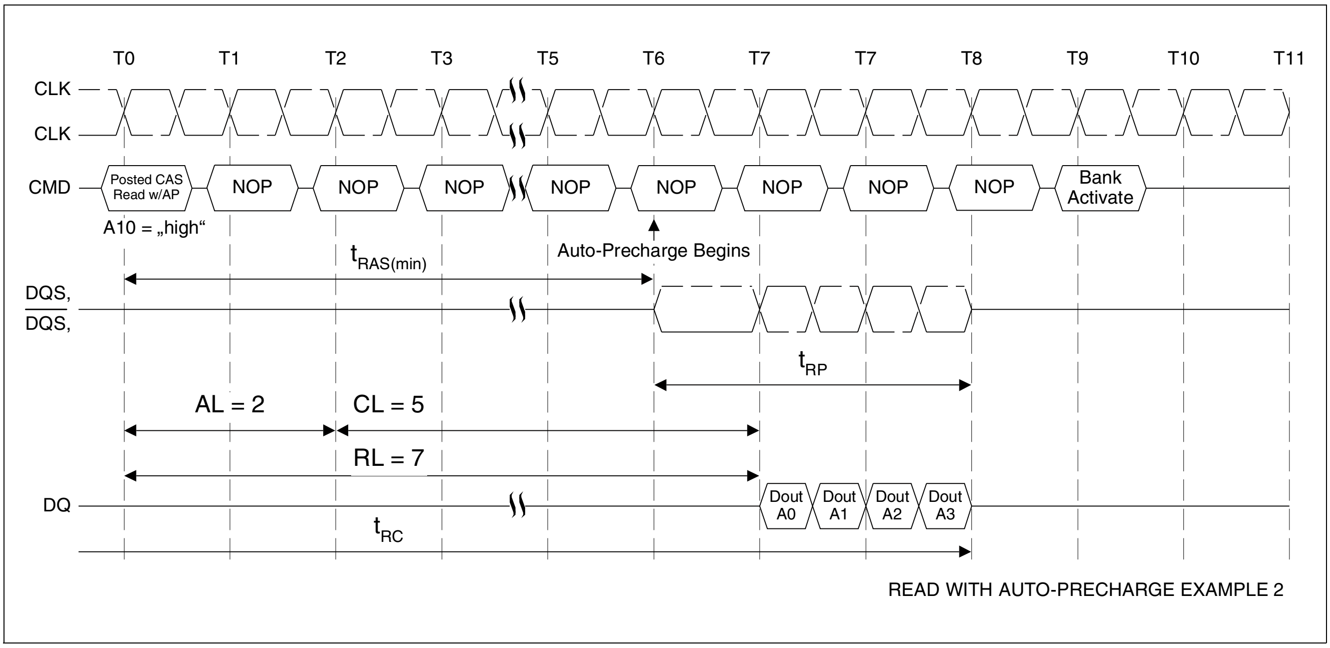


Figure 42 Read with Auto-Precharge Example 2, followed by an Activation to the Same Bank (t_{RAS} Limit): RL = 7 (AL = 2, CL = 5), BL = 4, $t_{RTP} \leq 2$ clocks

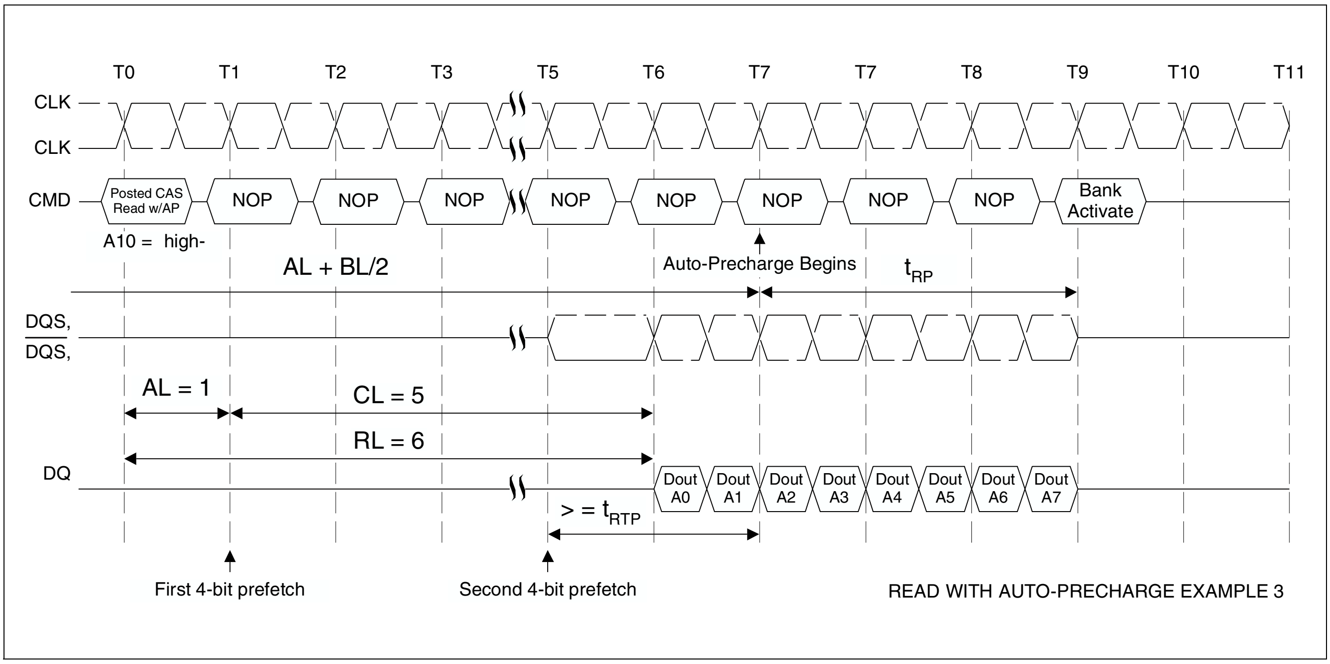


Figure 43 Read with Auto-Precharge Example 3, followed by an Activation to the Same Bank: RL = 6 (AL = 1, CL = 5), BL = 8, $t_{RTP} \leq$ 2 clocks

2.8.2 Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (t_{WR}), programmed in the MRS register, as long as t_{RAS} is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

1. The last data-in to bank activate delay time (t_{DAL} = WR + t_{RP}) has been satisfied.
2. The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

In DDR2 SDRAM's the write recovery time delay (t_{WR}) has to be programmed into the MRS mode register. As long as the analog t_{WR} timing parameter is not violated, WR can be programmed between 2 and 6 clock cycles. Minimum Write to Activate command spacing to the same bank = WL + BL/2 + t_{DAL}.

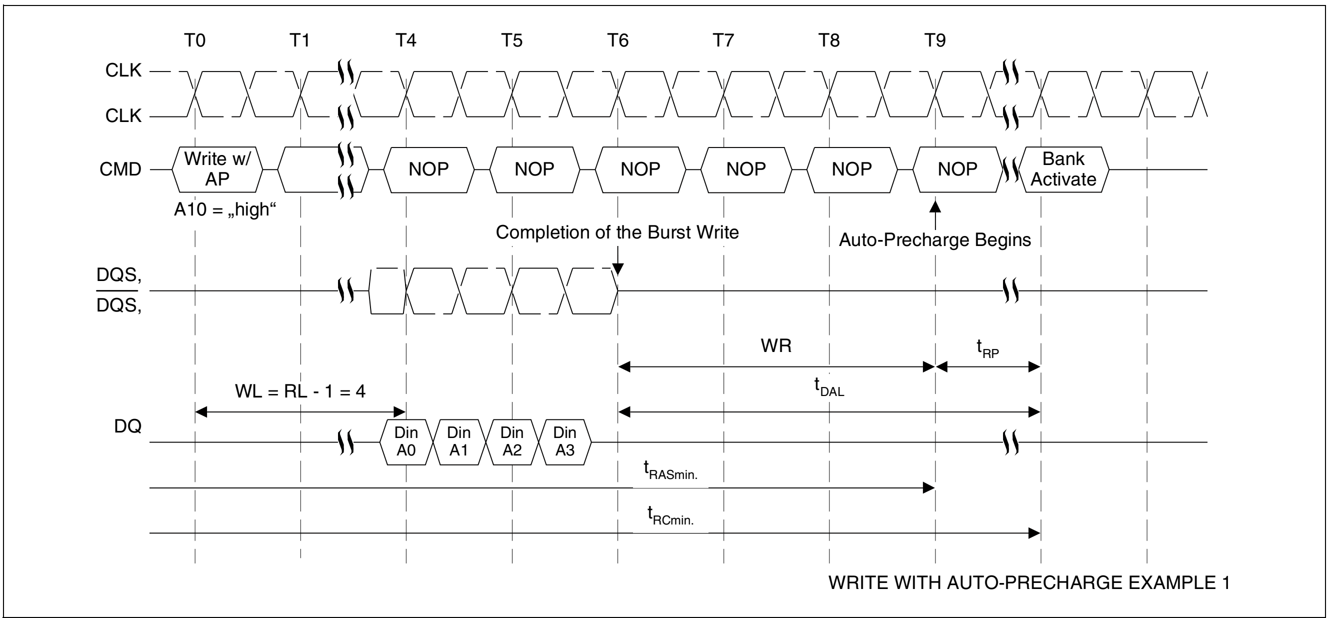


Figure 44 Write with Auto-Precharge Example 1 (t_{RC} Limit): WL = 4, t_{DAL} = 6 (WR = 3, t_{RP} = 3), BL = 4

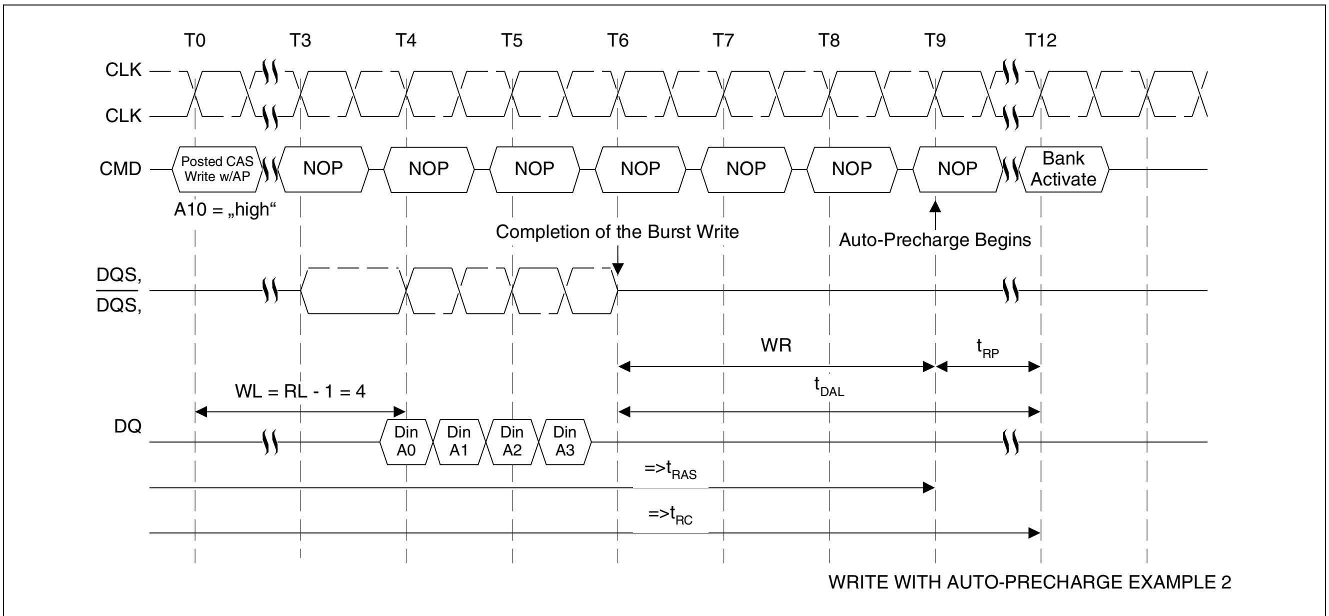


Figure 45 Write with Auto-Precharge Example 2 (WR + t_{RP} Limit): WL = 4, t_{DAL} = 6 (WR = 3, t_{RP} = 3), BL = 4

2.8.3 Read or Write to Precharge Command Spacing Summary

The following table summarizes the minimum command delays between Read, Read w/AP, Write, Write w/AP to the Precharge commands to the same banks and Precharge-All commands.

Table 14 Minimum Command Delays

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Units	Notes
READ	PRECHARGE (to same banks as READ)	AL + BL/2 + max(t_{RTP}, 2) - 2×t_{CK}	t_{CK}	1)2)
	PRECHARGE-ALL	AL + BL/2 + max(t_{RTP}, 2) - 2×t_{CK}	t_{CK}	1)2)
READ w/AP	PRECHARGE (to same banks as READ w/AP)	AL + BL/2 + max(t_{RTP}, 2) - 2×t_{CK}	t_{CK}	1)2)
	PRECHARGE-ALL	AL + BL/2 + max(t_{RTP}, 2) - 2×t_{CK}	t_{CK}	1)2)
WRITE	PRECHARGE (to same banks as WRITE)	WL + BL/2 + t_{WR}	t_{CK}	2)3)
	PRECHARGE-ALL	WL + BL/2 + t_{WR}	t_{CK}	2)3)
WRITE w/AP	PRECHARGE (to same banks as WRITE w/AP)	WL + BL/2 + WR	t_{CK}	2)
	PRECHARGE-ALL	WL + BL/2 + WR	t_{CK}	2)
PRECHARGE	PRECHARGE (to same banks as PRECHARGE)	1	t_{CK}	2)
	PRECHARGE-ALL	1	t_{CK}	2)
PRECHARGE-ALL	PRECHARGE	1	t_{CK}	2)
	PRECHARGE-ALL	1	t_{CK}	2)

1) RU{t_{RTP}(ns) / t_{CK}(ns)} must be used, where RU stands for "Round Up"
2) For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge-all, issued to that bank. The precharge period is satisfied after t_{RP} or $t_{RP, all}$ depending on the latest precharge command issued to that bank
3) RU{t_{WR}(ns) / t_{CK}(ns)} must be used, where RU stands for "Round Up"

2.8.4 Concurrent Auto-Precharge

DDR2 devices support the "Concurrent Auto-Precharge" feature. A Read with Auto-Precharge enabled, or a Write with Auto-Precharge enabled, may be followed by any command to the other bank, as long as that command does not interrupt the read or write data transfer, and all other related limitations (e.g. contention between Read data and Write data must be avoided externally and on the internal data bus.

The minimum delay from a Read or Write command with Auto-Precharge enabled, to a command to a different bank, is summarized in **Table 15**. As defined, the WL = RL - 1 for DDR2 devices which allows the command gap and corresponding data gaps to be minimized.

Table 15 Command Delay Table

From Command	To Command (different bank, non-interrupting command)	Minimum Delay with Concurrent Auto-Precharge Support	Units	Note
WRITE w/AP	Read or Read w/AP	(CL -1) + (BL/2) + t_{WTR}	t_{CK}	1)
	Write or Write w/AP	BL/2	t_{CK}	
	Precharge or Activate	1	t_{CK}	2)
Read w/AP	Read or Read w/AP	BL/2	t_{CK}	
	Write or Write w/AP	BL/2 + 2	t_{CK}	
	Precharge or Activate	1	t_{CK}	2)

1) RU{t_{WTR}(ns)/t_{CK}(ns)} must be used where RU stands for "Round Up"
2) This rule only applies to a selective Precharge command to another banks, a Precharge-All command is illegal

2.9 Refresh

DDR2 SDRAM requires a refresh of all rows of a bank within a time interval defined by 8192 (which represents the number of rows) x t_{REFI}. The necessary refresh can be generated in one of two ways: by explicit Auto-Refresh commands or by an internally timed Self-Refresh mode.

2.9.1 Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAM's. This command is non persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits "don't care" during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of $t_{REF(maximum)}$.

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is $9 \times t_{REFI}$.

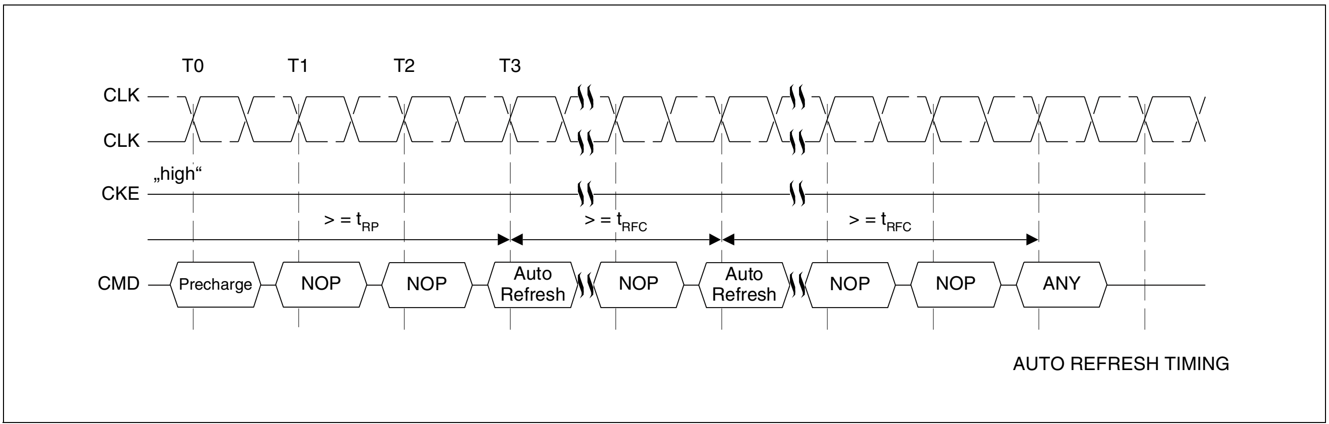


Figure 46 Auto Refresh Timing

2.9.2 Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS(1) command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are “don’t care”. The DRAM initiates a minimum of one Auto Refresh command internally within t_{CKE} period once it enters Self Refresh mode. The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is t_{CKE}. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self-Refresh Exit command is registered, a delay of at least t_{XSNR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain high for the entire Self-Refresh exit period t_{XSRD} for proper operation. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after t_{XSNR} expires. NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval t_{XSNR}. ODT should be turned off during t_{XSNR}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh Mode.

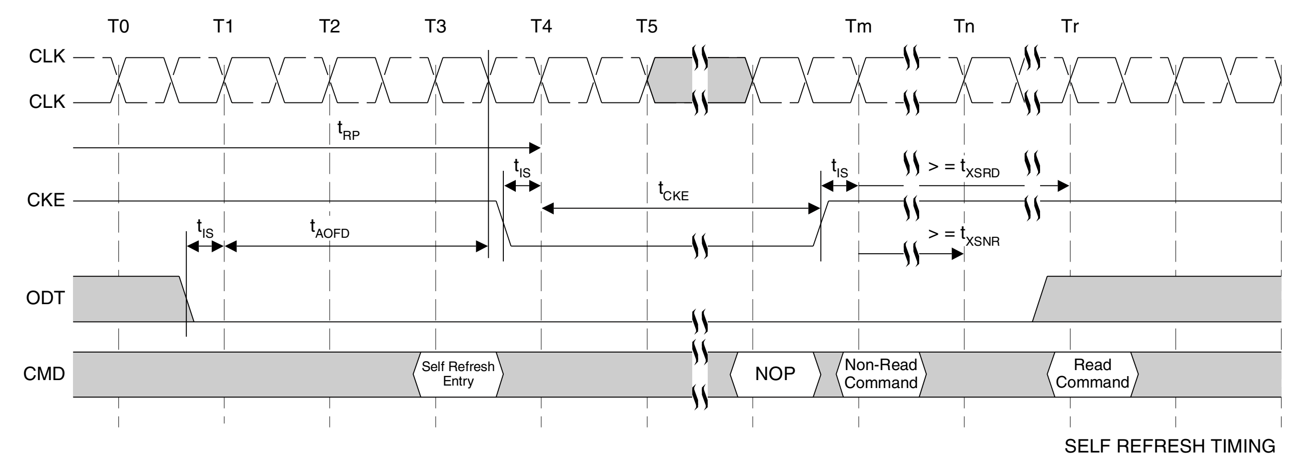


Figure 47 Self Refresh Timing

Note:

1. *Device must be in the “All banks idle” state before entering Self Refresh mode.*
2. t_{XSRD} ($\geq 200\ t_{CK}$) has to be satisfied for a Read or a Read with Auto-Precharge command.
3. *t_{XSNR} has to be satisfied for any command except a Read or a Read with Auto-Precharge command*
4. *Since CKE is an SSTL input, V_{REF} must be maintained during Self Refresh.*

2.10 Power-Down

Power-down is synchronously entered when CKE is registered low, along with NOP or Deselect command. CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any other operation such as row activation, Precharge, Auto-Precharge or Auto-Refresh is in progress, but power-down I_{DD} specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation. DRAM design guarantees it's DLL in a locked state with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

If power-down occurs when all banks are precharged, this mode is referred to as Precharge Power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as Active Power-down. For Active Power-down two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "low" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to "high" this mode is referred as a power saving "low power active power-down mode". This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE. Also the DLL is disabled upon entering Precharge Power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times t_{REFI} of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD} or t_{XARDS}, after CKE goes high. Power-down exit latencies are defined in **Table 44** and ff.

Power-Down Entry

Active Power-down mode can be entered after an Activate command. Precharge Power-down mode can be entered after a Precharge, Precharge-All or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when t_{MRD} is satisfied.

Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied.

Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed when WL + BL/2 + t_{WTR} is satisfied.

In case of a write command with Auto-Precharge, Power-down mode entry is allowed after the internal precharge command has been executed, which is WL + BL/2 + WR starting from the write with Auto-Precharge command. In this case the DDR2 SDRAM enters the Precharge Power-down mode.

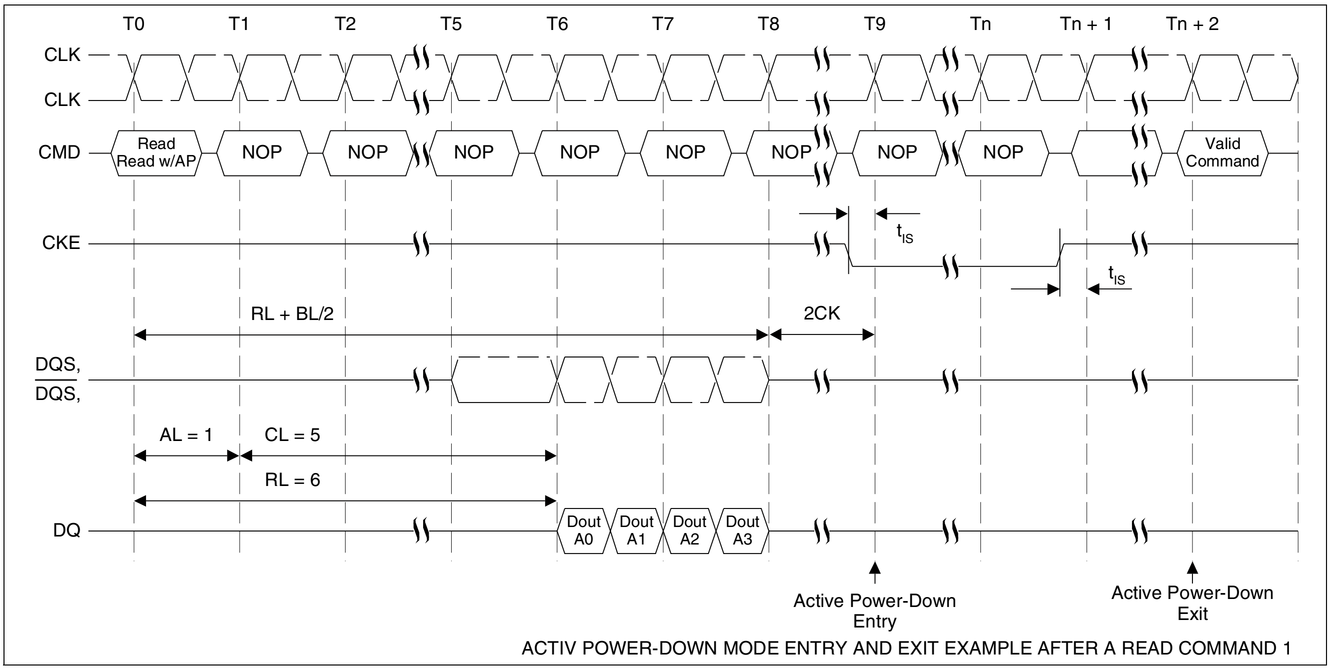


Figure 48 Active Power-Down Mode Entry and Exit after an Activate Command

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12.

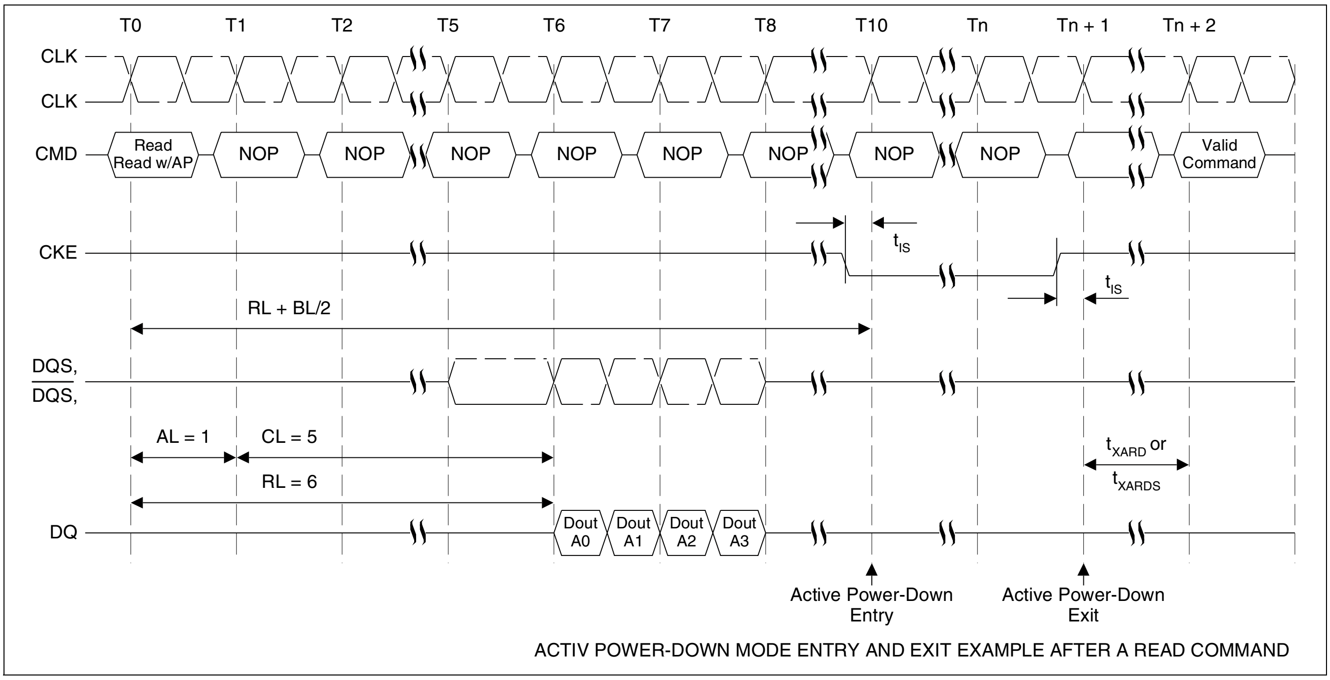


Figure 49 Active Power-Down Mode Entry and Exit Example after a Read Command: RL = 6 (AL = 1, CL =5), BL = 4

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12.

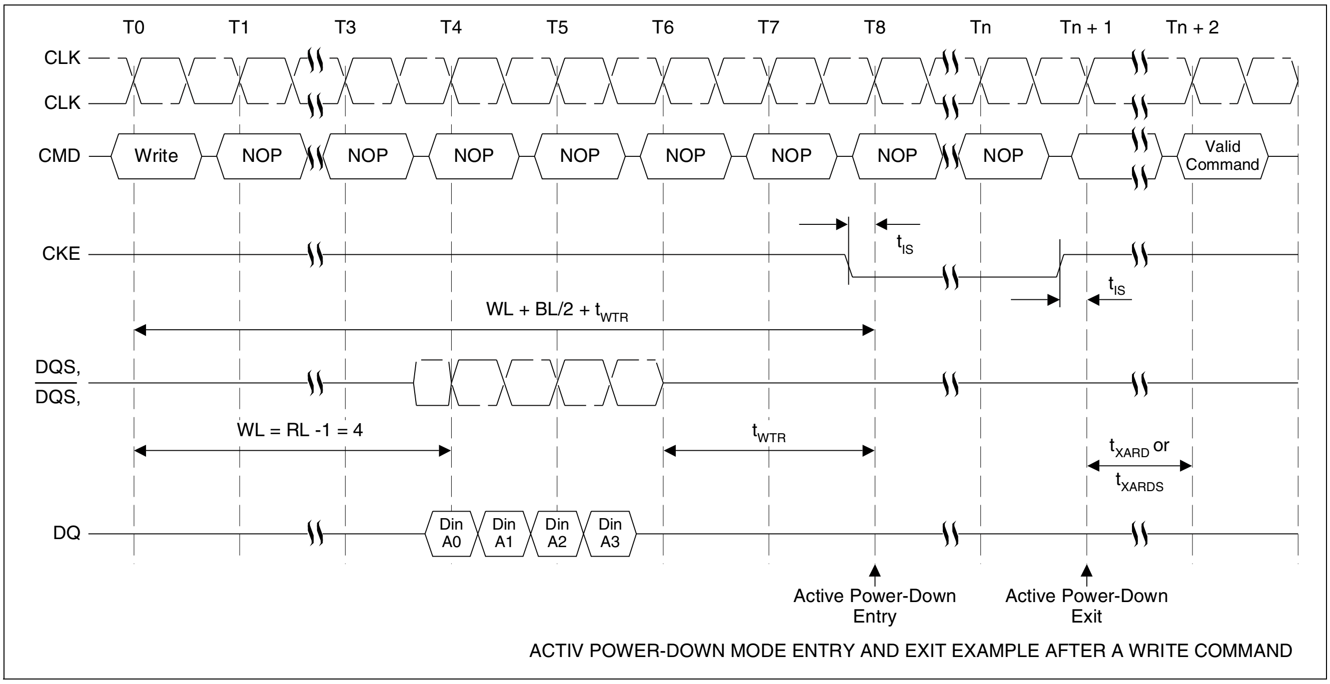


Figure 50 Active Power-Down Mode Entry and Exit Example after a Write Command: WL = 4, t_{WTR} = 2, BL = 4

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12.

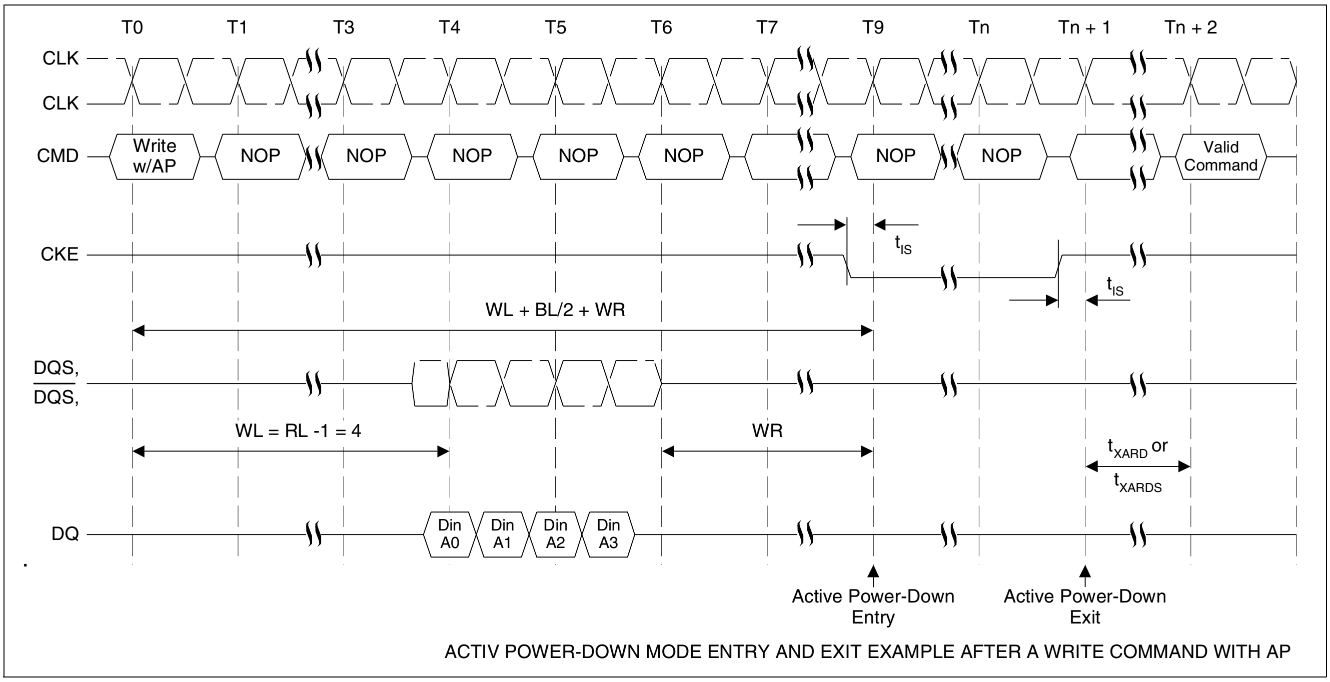


Figure 51 Active Power-Down Mode Entry and Exit Example after a Write Command with AP: WL = 4, WR = 3, BL = 4

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MRS, address bit A12. WR is the programmed value in the MRS mode register.

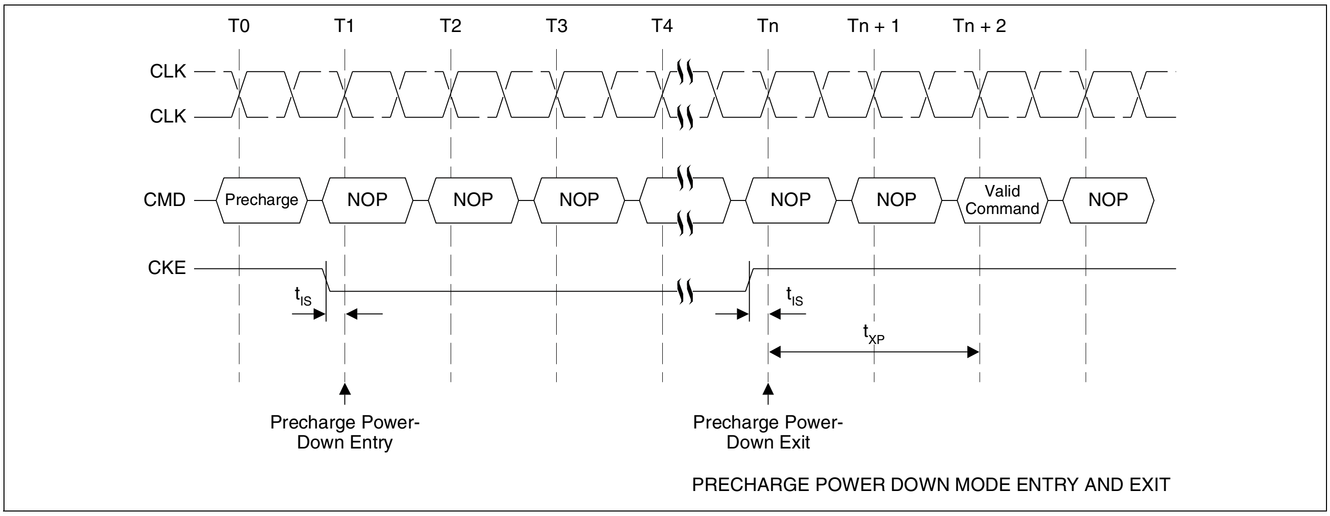


Figure 52 Precharge Power Down Mode Entry and Exit

Note: “Pre-charge” may be an external command or an internal precharge following Write with AP.

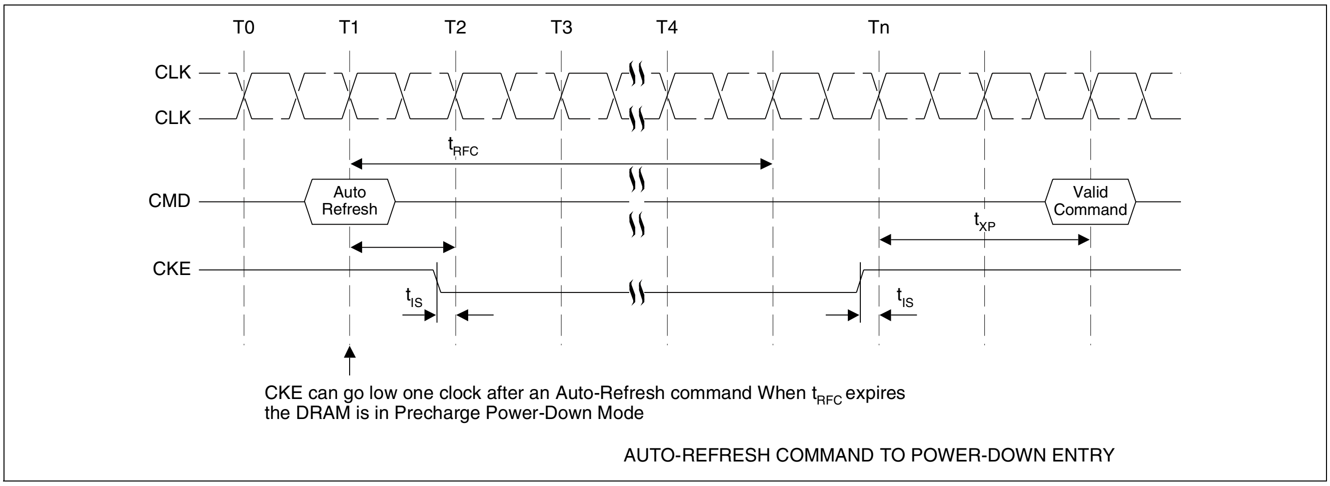


Figure 53 Auto-Refresh command to Power-Down entry

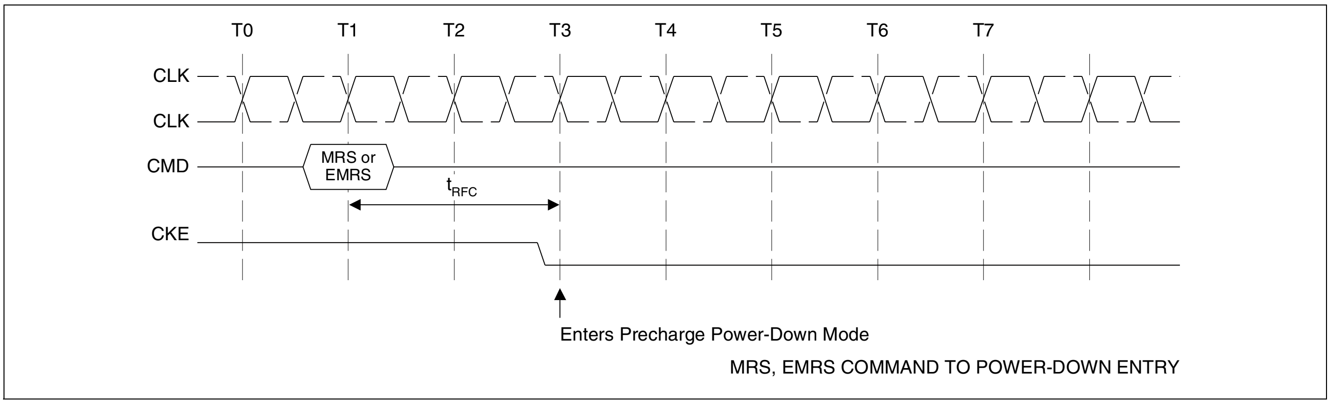


Figure 54 MRS, EMRS command to Power-Down entry

2.11 Other Commands

2.11.1 No Operation Command

The No Operation Command (NOP) should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.11.2 Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don’t care.

2.12 DLL-off Mode Clock Speed Operation Range

Table 16 DLL-off Mode Clock Speed Operation Range

Parameter	Product Name	Min	Max	Unit
Clock Frequency Range for DLL-OFF Mode	HYB18T256161AFL25	66	250	MHz
	HYB18T256161AFL28	66	250	MHz
	HYB18T256161AFL33	66	250	MHz

2.13 Input Clock Frequency Change

During operation the DRAM input clock frequency can be changed under the following conditions:

- During Self-Refresh operation
- DRAM is in Precharge Power-down mode and ODT is completely turned off.

The DDR2-SDRAM has to be in Precharged Power-down mode and idle. ODT must be already turned off and CKE must be at a logic “low” state. After a minimum of two clock cycles after t_{RP} and t_{AOFD} have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a “high” logic level again. After t_{XP} has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

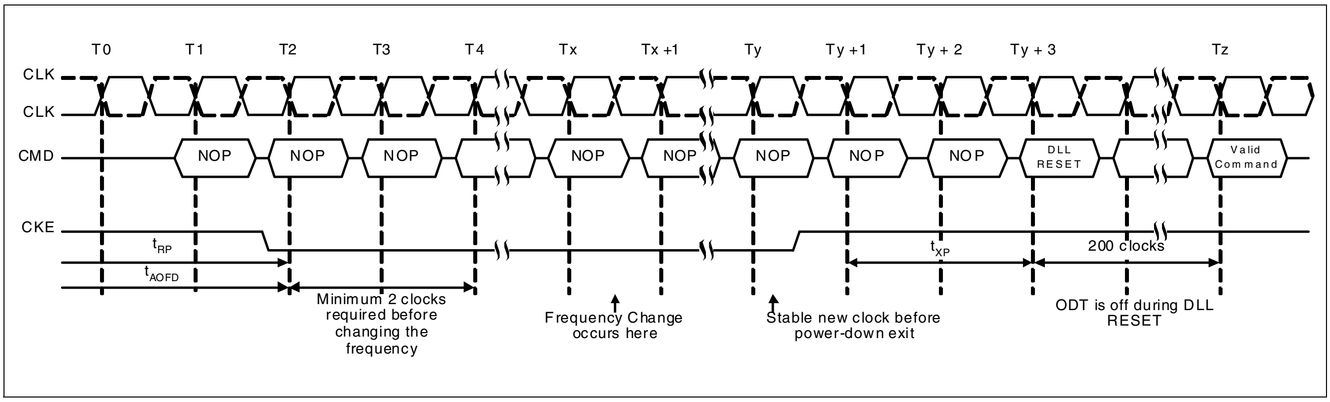


Figure 55 Input Frequency Change Example during Precharge Power-Down mode

2.14 Asynchronous CKE Low Reset Event

In a given system, Asynchronous Reset event can occur at any time without prior knowledge. In this situation, memory controller is forced to drop CKE asynchronously low, immediately interrupting any valid operation. DRAM requires CKE to be maintained "high" for all valid operations as defined in this data sheet. If CKE asynchronously drops "low" during any valid operation, the DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (t_{delay}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "high" again. The DRAM must be fully re-initialized as described the initialization sequence (section 2.2.1, step 4 thru 13). DRAM is ready for normal operation after the initialization sequence. See **Chapter 7**.

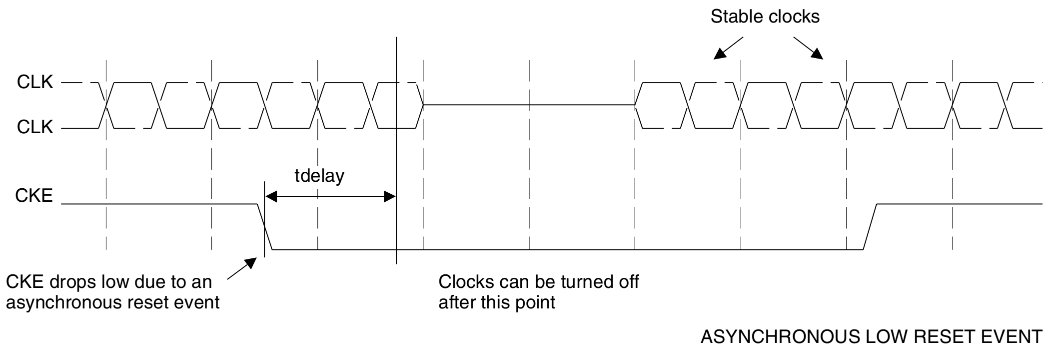


Figure 56 Asynchronous Low Reset Event

3 Truth Tables

Table 17 Command Truth Table

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A[12:11]	A10	A[9:0]	Notes [1][2][3][4]
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			[5]
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	[6]
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	[6][7]
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	[5]
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	
Bank Activate	H	H	L	L	H	H	BA	Row Address			[5]
Write	H	H	L	H	L	L	BA	Column	L	Column	[5][8]
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	[5][8]
Read	H	H	L	H	L	H	BA	Column	L	Column	[5][8]
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	[5][8]
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Power Down Entry	H	L	H	X	X	X	X	X	X	X	[9]
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	[4][9]
			L	H	H	H					

1) All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.
2) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
3) "X" means "H or L (but a defined logic level)".
4) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
5) Bank addresses (BAx) determine which bank is to be operated upon. For (E)MRS BAx selects an (Extended) Mode Register.
6) V_{REF} must be maintained during Self refresh Operation.
7) Self Refresh Exit is asynchronous.
8) Burst reads or writes at BL = 4 cannot be terminated. See **Chapter 2.6.6** for details.
9) The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in **Chapter 2.9**.

Table 18 Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State[1]	CKE		Command (N)[2) 3)]	Action (N)[2]	Notes[4)5)]
	Previous Cycle[6] (N-1)	Current Cycle[6] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power-Down	L	L	X	Maintain Power-Down	7)8)11)
	L	H	DESELECT or NOP	Power-Down Exit	9)10)11)7)
Self Refresh	L	L	X	Maintain Self Refresh	11)8)12)
	L	H	DESELECT or NOP	Self Refresh Exit	9)13)14)12)
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	9)10)15)11)7)
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	9)10)15)11)
	H	L	AUTOREFRESH	Self Refresh Entry	16)14)11)7)
Any State other than listed above	H	H	Refer to the Command Truth Table		17)

1) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
2) Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
3) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
4) CKE must be maintained high while the device is in OCD calibration mode.
5) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
6) CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
7) The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements
8) “X” means “don’t care (including floating around V_{REF})” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMRS(1)).
9) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
10) Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2\times t_{CKE} + t_{IH}$.
12) V_{REF} must be maintained during Self Refreh Operation
13) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
14) Valid commands for Self Refresh Exit are NOP and DESELCT only.
15) Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress. See **Chapter 2.10** and **Chapter 2.9.2** for a detailed list of restrictions.
16) Self Refresh mode can only be entered from the All Banks Idle state.
17) Must be a legal command as defined in the Command Truth Table.

Table 19 Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data; provided coincident with the corresponding data.

4 Absolute Maximum Ratings

Table 20 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0 to +2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5 to +2.3	V	1)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5 to +2.3	V	1)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5 to +2.3	V	1)
T_{STG}	Storage Temperature	-55 to +150	°C	1)2)
T_J	Junction Temperature	+125	°C	1)

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

5 Electrical Characteristics

Table 21 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 85	°C	1)2)3)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2) The Operating temperature covers the temperature range where the full DRAM specification is supported.
3) Above 85 °C case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.

5.1 DC Characteristics

Table 22 Rating for HYB18T256161AF-22/-25/-28/-33

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.9	2.0	2.1	V	1)
V_{DDL}	Supply Voltage for DLL	1.9	2.0	2.1	V	1)
V_{DDQ}	Supply Voltage for Output	1.9	2.0	2.1	V	1)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	4)

1) V_{DDQ} tracks with V_{DD}, V_{DDDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDDL} tied together.
2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
3) Peak to peak ac noise on V_{REF} may not exceed ± 2% V_{REF} (dc)
4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}.

Table 23 Rating for HYB18T256161AFL25/L28/L33

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1)
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	4)

1) V_{DDQ} tracks with V_{DD}, V_{DDDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDDL} tied together.
2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
3) Peak to peak ac noise on V_{REF} may not exceed ± 2% V_{REF} (dc)
4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}.

Table 24 ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Units	Notes
Termination resistor impedance value for EMRS(1)[A6,A2]= [0,1]; 75 Ω	$Rtt1_{(eff)}$	60	75	95	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2]=[1,0]; 150 Ω	$Rtt2_{(eff)}$	120	150	180	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2]=[1,1]; 50 Ω	$Rtt3_{(eff)}$	40	50	65	Ω	1)
Deviation of V_M with respect to V_{DDQ} / 2	delta VM	–6.00	—	+ 6.00	%	2)

1) Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IHac})$ and $I(V_{ILac})$ respectively. Rtt(eff) = $(V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IHac}) - I(V_{ILac}))$.
2) Measurement Definition for V_M: Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: delta V_M = ((2 x V_M / V_{DDQ}) – 1) x 100%.

Table 25 Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Units	Notes
I_{IL}	Input Leakage Current; any input 0 V < V_{IN} < V_{DD}	–2	+2	µA	1)
I_{OL}	Output Leakage Current; 0 V < V_{OUT} < V_{DDQ}	–5	+5	µA	2)

1) all other pins not under test = 0 V.
2) DQ's, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ are disabled and ODT is turned off.

5.2 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable $\overline{DQS}$" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the $\overline{DQS}$ (and $\overline{RDQS}$) signals are internally disabled and don't care.

Table 26 DC & AC Logic Input Levels

Symbol	Parameter	Min.	Max.	Units
$V_{IH(dc)}$	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V
$V_{IL(dc)}$	DC input low	–0.3	V_{REF} – 0.125	V
$V_{IH(ac)}$	AC input logic high	V_{REF} + 0.250	—	V
$V_{IL(ac)}$	AC input low	—	V_{REF} – 0.250	V

Table 27 Single-ended AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1)
$V_{SWING(max)}$	Input signal maximum peak to peak swing	1.0	V	1)
SLEW	Input signal minimum slew rate	1.0	V / ns	2)3)

1) Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2) The input signal minimum slew rate is to be maintained over the range from $V_{IH(AC)min}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(AC)max}$ for falling edges as shown in **Figure 57**.

3) AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac}$ on the negative transitions.

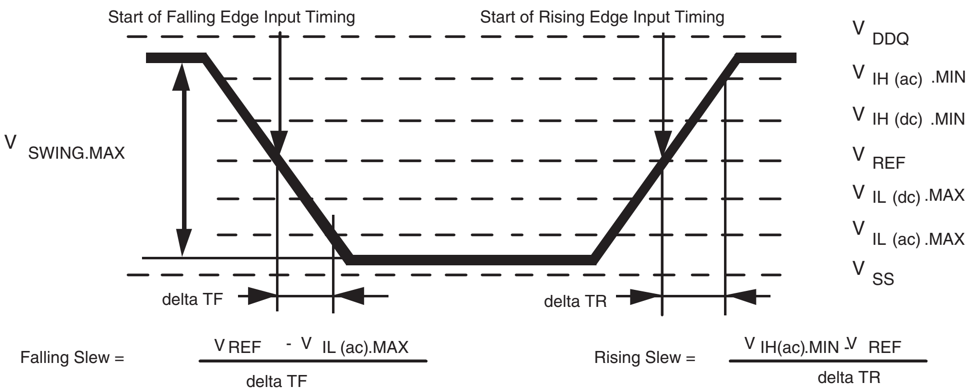


Figure 57 Single-ended AC Input Test Conditions Diagram

Table 28 Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IN(dc)}$	DC input signal voltage	–0.3	V_{DDQ} + 0.3		1)
$V_{ID(dc)}$	DC differential input voltage	0.25	V_{DDQ} + 0.6		2)
$V_{ID(ac)}$	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	3)
$V_{IX(ac)}$	AC differential cross point input voltage	0.5 × V_{DDQ} – 0.175	0.5 × V_{DDQ} + 0.175	V	4)
$V_{OX(ac)}$	AC differential cross point output voltage	0.5 × V_{DDQ} – 0.125	0.5 × V_{DDQ} + 0.125	V	5)

1) $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$ etc.
2) $V_{ID(dc)}$ specifies the input differential voltage V_{TR}– V_{CP} required for switching. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$.
3) $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} - V_{IL(ac)}$.
4) The value of $V_{IX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ}. $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.
5) The value of $V_{OX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ}. $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

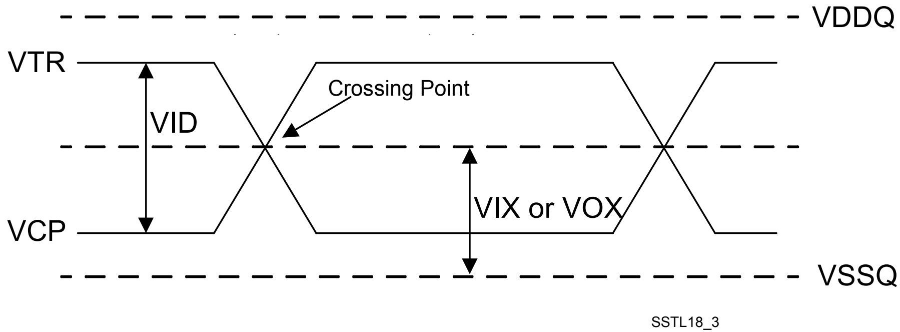


Figure 58 Differential DC and AC Input and Output Logic Levels Diagram

5.3 Output Buffer Characteristics

Table 29 SSTL_18 Output DC Current Drive

Symbol	Parameter	SSTL_18	Unit	Note
I_{OH}	Output Minimum Source DC Current	–13.4	mA	1)2)
I_{OL}	Output Minimum Sink DC Current	13.4	mA	2)3)

1) V_{DDQ} = 2.0V +/- 0.1V; V_{OUT} = 1.42 V. (V_{OUT}–V_{DDQ}) / I_{OH} must be less than 21 Ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} – 280 mV.
2) The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in [1)] and [3)]. They are used to test drive current capability to ensure $V_{IH.MIN}$. plus a noise margin and $V_{IL.MAX}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 Ohm load line to define a convenient current for measurement.
3) V_{DDQ} = 2.0V +/- 0.1V; V_{OUT} = 280 mV. V_{OUT} / I_{OL} must be less than 21 Ohm for values of V_{OUT} between 0 V and 280 mV.

Table 30 SSTL_18 Output AC Test Conditions

Symbol	Parameter	SSTL_18	Unit	Note
V_{OH}	Minimum Required Output Pull-up	V_{TT} + 0.603	V	1)
V_{OL}	Maximum Required Output Pull-down	V_{TT} – 0.603	V	1)
V_{OTR}	Output Timing Measurement Reference Level	$0.5 \times V_{DDQ}$	V	

1) SSTL_18 test load for V_{OH} and V_{OL} is different from the referenced load described in **Chapter 8.1**. The SSTL_18 test load has a 20 Ohm series resistor additionally to the 25 Ohm termination resistor into V_{TT}. The SSTL_18 definition assumes that ± 335 mV must be developed across the effectively 25 Ohm termination resistor (13.4 mA × 25 Ohm = 335 mV). With an additional series resistor of 20 Ohm this translates into a minimum requirement of 603 mV swing relative to V_{TT}, at the ouput device (13.4 mA × 45 Ohm = 603 mV).

Table 31 OCD Default Characteristics

Symbol	Description	Min.	Nominal	Max.	Unit	Note
—	Output Impedance	12.6	18	23.4	Ohms	1)2)
—	Pull-up / Pull down mismatch	0	—	4	Ohms	1)2)3)
—	Output Impedance step size for OCD calibration	0	—	1.5	Ohms	4)
S_{OUT}	Output Slew Rate	1.5	—	5.0	V / ns	1)5)6)7)8)

1) V_{DDQ} = 2.0V +/- 0.1V; V_{DD} = 2.0V +/- 0.1V
2) Impedance measurement condition for output source dc current: V_{DDQ} = 2.0V +/- 0.1V, V_{OUT} = 1420 mV; (V_{OUT}–V_{DDQ}) / I_{OH} must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and V_{DDQ} – 280 mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 2.0V +/- 0.1V; V_{OUT} = –280 mV; V_{OUT} / I_{OL} must be less than 23.4 Ohms for values of V_{OUT} between 0 V and 280 mV.
3) Mismatch is absolute value between pull-up and pull-down, both measured at same temperature and voltage.
4) This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is 18 ± 0.75 Ohms under nominal conditions.
5) Slew Rates according to **Chapter 8.2.1** $V_{IL(ac)}$ to $V_{IH(ac)}$ with the load specified in **Figure 63**.
6) The absolute value of the Slew Rate as measured from DC to DC is equal to or greater than the Slew Rate as measured from AC to AC. This is verified by design and characterization but not subject to production test.
7) Timing skew due to DRAM output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ's is included in t_{DQSQ} and t_{QHS} specification.
8) DRAM output Slew Rate specification applies to 400 and 533 MT/s speed bins.

5.4 Default Output V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS(1) bits A[9:7] ='111'. **Figure 59** and **Figure 60** show the driver characteristics graphically and the tables show the same data suitable for input into simulation tools.

Table 32 Full Strength Default Pull-up Driver Characteristics

Voltage (V)	Pull-up Driver Current [mA]			
	Min.	Nominal Default low	Nominal Default high	Max.
0.2	–8.5	–11.1	–11.8	–15.9
0.3	–12.1	–16.0	–17.0	–23.8
0.4	–14.7	–20.3	–22.2	–31.8
0.5	–16.4	–24.0	–27.5	–39.7
0.6	–17.8	–27.2	–32.4	–47.7
0.7	–18.6	–29.8	–36.9	–55.0
0.8	–19.0	–31.9	–40.8	–62.3
0.9	–19.3	–33.4	–44.5	–69.4
1.0	–19.7	–34.6	–47.7	–75.3
1.1	–19.9	–35.5	–50.4	–80.5
1.2	–20.0	–36.2	–52.5	–84.6
1.3	–20.1	–36.8	–54.2	–87.7
1.4	–20.2	–37.2	–55.9	–90.8
1.5	–20.3	–37.7	–57.1	–92.9
1.6	–20.4	–38.0	–58.4	–94.9
1.7	–20.6	–38.4	–59.6	–97.0
1.8	—	–38.6	–60.8	–99.1
1.9	—	—	—	–101.1

Note: The driver characteristics evaluation conditions are:

1. *Nominal Default 25°C (Tcase),* V_{DDQ} *= 2.0 V, typical process*
2. *Minimum:* T_{case} *= 85 °C,* V_{DDQ} *= 1.9 V, slow–slow process*
3. *Maximum:* T_{case} *= 0°C,* V_{DDQ} *= 2.1 V, fast–fast process*

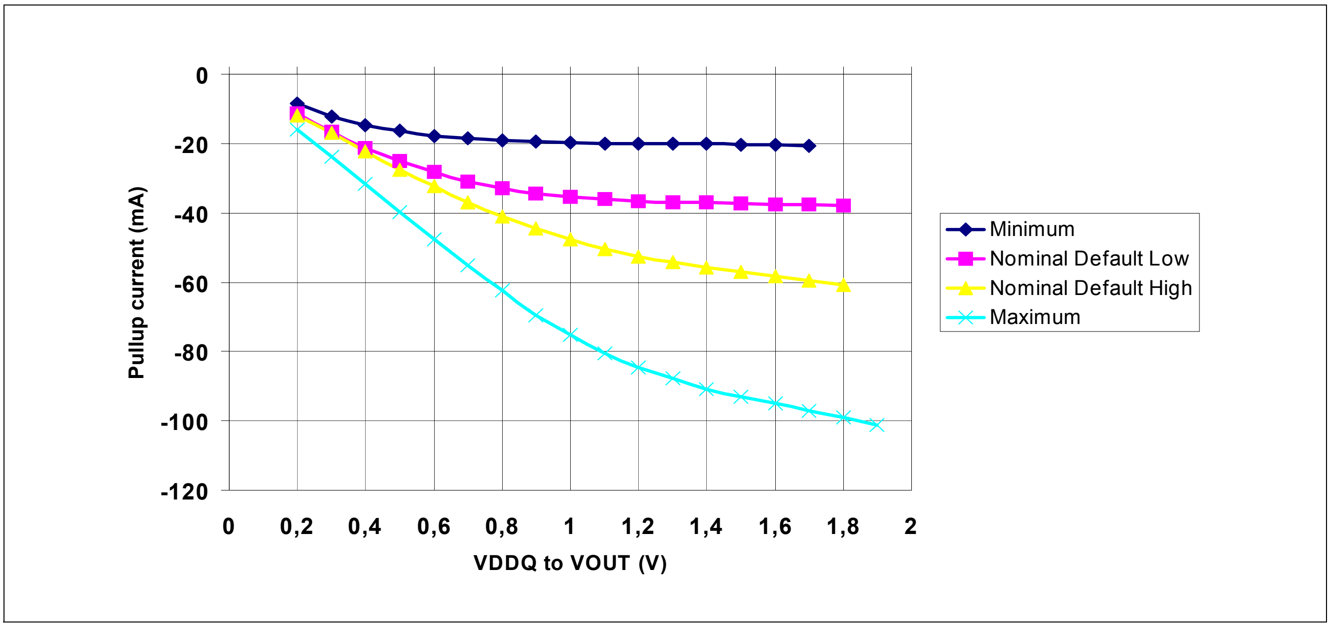


Figure 59 Full Strength Default Pull-up Driver Diagram

Table 33 Full Strength Default Pull–down Driver Characteristics

Voltage (V)	Pull-down Driver Current [mA]			
	Minimum	Nominal Default low	Nominal Default high	Maximum
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8	—	37.9	60.9	99.1
1.9	—	—	—	101.1

Note: The driver characteristics evaluation conditions are:

1. *Nominal Default 25 °C (T_{case}), V_{DDQ} = 2.0 V, typical process,*
2. *Minimum: T_{case} = 85 °C, V_{DDQ} = 1.9 V, slow–slow process*
3. *Maximum: T_{case} = 0°C, V_{DDQ} = 2.1 V, fast–fast process*

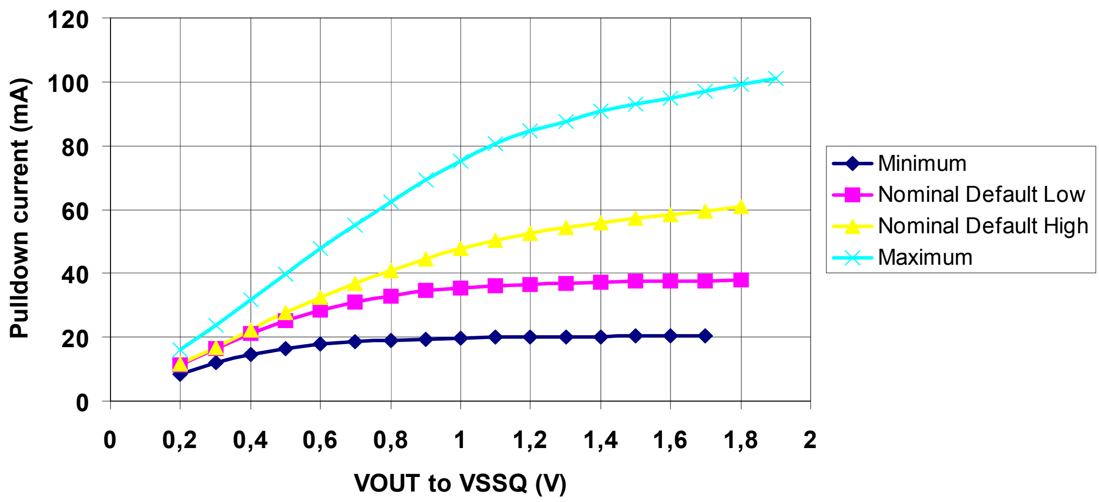


Figure 60 Full Strength Default Pull–down Driver Diagram

5.4.1 Calibrated Output Driver V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the Off-Chip Driver (OCD) Impedance Adjustment. The **Table 34** and **Table 35** show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohms step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves are represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figure. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy and uncertainty with DQ to DQ variation, it is recommended that only the default values to be used. The nominal maximum ad minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

Table 34 Full Strength Calibrated Pull-down Driver Characteristics

Voltage (V)	Calibrated Pull-down Driver Current [mA]				
	Nominal Minimum (21 Ohms)	Normal Low (18.75 Ohms)	Nominal (18 ohms)	Normal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

Note: The driver characteristics evaluation conditions are:

1. *Nominal 25 °C (T_{case}), V_{DDQ} = 2.0 V, typical process*
2. *Nominal Low and Nominal High: T_{case} = 25 °C , V_{DDQ} = 2.0 V, any process*
3. *Nominal Minimum: T_{case} = 85 °C, V_{DDQ} = 1.9 V, any process*
4. *Nominal Maximum: T_{case} = 0°C, V_{DDQ} = 2.1 V, any process*

Table 35 Full Strength Calibrated Pull-up Driver Characteristics

Voltage (V)	Calibrated Pull-up Driver Current [mA]				
	Nominal Minimum (21 Ohms)	Nominal Low (18.75 Ohms)	Nominal (18 ohms)	Nominal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	–9.5	–10.7	–11.4	–11.8	–13.3
0.3	–14.3	–16.0	–16.5	–17.4	–20.0
0.4	–18.3	–21.0	–21.2	–23.0	–27.0

Note: The driver characteristics evaluation conditions are:

1. *Nominal 25 °C (T_{case}), V_{DDQ} = 2.0 V, typical process*
2. *Nominal Low and Nominal High 25 °C (T_{case}), V_{DDQ} = 2.0 V, any process*
3. *Nominal Minimum: T_{case} = 85 °C, V_{DDQ} = 1.9 V, any process*
4. *Nominal Maximum: T_{case} = 0°C, V_{DDQ} = 2.1 V, any process*

5.5 Input / Output Capacitance

Table 36 Input / Output Capacitance

Symbol	Parameter	min.	max.	Units
CCK	Input capacitance, CK and $\overline{CK}$	0.5	1.5	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	0.5	1.5	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	—	0.25	pF

5.6 Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address (A[13:0], BA[2:0]), $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$, CKE and ODT pins. The V-I characteristics for pins with clamps is shown in **Table 37**.

Table 37 Power & Ground Clamp V-I Characteristics

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

5.7 Overshoot and Undershoot Specification

Table 38 AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2–900	DDR2–800	DDR2–700	Units
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	V
Maximum overshoot area above V_{DD}	0.75	0.75	0.75	V.ns
Maximum undershoot area below V_{SS}	0.75	0.75	0.75	V.ns

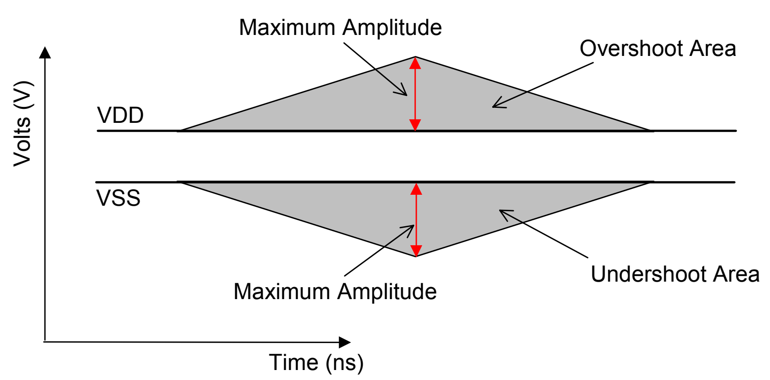


Figure 61 AC Overshoot / Undershoot Diagram for Address and Control Pins

Table 39 AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2–900	DDR2–800	DDR2–700	Units
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	V
Maximum overshoot area above V_{DDQ}	0.38	0.38	0.38	V.ns
Maximum undershoot area below V_{SSQ}	0.38	0.38	0.38	V.ns

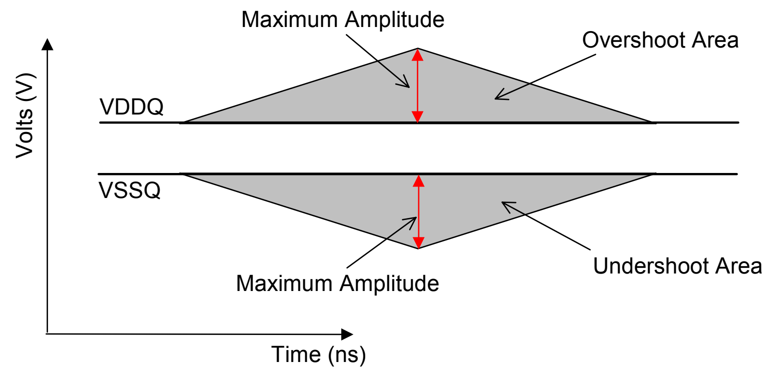


Figure 62 AC Overshoot / Undershoot Diagram for Clock, Data, Strobe and Mask Pins

6 I_{DD} Specifications and Conditions

Table 40 I_{DD} Measurement Conditions

Parameter	Symbol	Notes 1)2)3)4)5)6)
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin}$., $t_{RAS} = t_{RASmin.}$, CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin}$., $t_{RAS} = t_{RASmin.}$, $t_{RCD} = t_{RCDmin.}$,AL = 0, CL = CL_{min}.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	
Precharge Power-Down Current All banks idle; CKE is LOW; $t_{CK} = t_{CKmin}$;Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Power-Down Current All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “0” (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “1” (Slow Power-down Exit);	$I_{DD3P(1)}$	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin}$.; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}	
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CKmin}$., Refresh command every $t_{RFC} = t_{RFCmin.}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	
Distributed Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	

Table 40 I_{DD} Measurement Conditions

Parameter	Symbol	Notes 1)2)3)4)5)6)
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current 3. All banks interleaving reads, I_{OUT} = 0 mA; BL = 4, CL=CL$_{(IDD)}$, AL = $t_{RCD(IDD)}$ -1 × $t_{CK(IDD)}$; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RRD} = $t_{RRD(IDD)}$; t_{FAW} = $t_{FAW(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address bus inputs are stable during deselects; Data bus is switching.	I_{DD7}	

1) V_{DDQ} = 2.0V +/- 0.1V; V_{DD} = 2.0V +/- 0.1V
2) I_{DD} specifications are tested after the device is properly initialized.
3) I_{DD} parameter are specified with ODT disabled.
4) Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
5) Definitions for I_{DD}: LOW is defined as $V_{IN} \le V_{IL(ac)max}$; HIGH is defined as $V_{IN} \ge V_{IH(ac)min}$; STABLE is defined as inputs are stable at a HIGH or LOW level; FLOATING is defined as inputs are $V_{REF} = V_{DDQ} / 2$; SWITCHING is defined as: Inputs are changing between HIGH and LOW every other clock (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other clock (once per clock) for DQ signals not including mask or strobes.
6) Timing parameter minimum and maximum values for I_{DD} current measurements are defined in **Table 42**.

Table 41 I_{DD} Specification

Product Type Speed Code	–2.2	–2.5	–2.8	–3.3	Unit	Notes
Speed Grade	**DDR2 – 900**	**DDR2 – 800**	**DDR2 – 700**	**DDR2 – 600**		
Symbol	**Typ.**	**Typ.**	**Typ.**	**Typ.**		
I_{DD0}	90	80	70	60	mA	
I_{DD1}	95	85	70	65	mA	
I_{DD2P}	4	4	4	4	mA	
I_{DD2N}	45	40	35	30	mA	
I_{DD2Q}	40	35	30	25	mA	
I_{DD3P}	20	20	15	15	mA	
	4	4	4	4	mA	
I_{DD3N}	50	45	40	35	mA	
I_{DD4R}	140	130	120	115	mA	
I_{DD4W}	180	170	160	155	mA	
I_{DD5B}	130	120	110	110	mA	
I_{DD5D}	5	5	5	5	mA	
I_{DD6}	8	8	8	8	mA	
I_{DD7}	190	180	170	160	mA	

6.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the following timing parameters are used:

Table 42 IDD Measurement Test Condition

Parameter	Symbol		-2.2 DDR2–900	-2.5 DDR2–800	-2.8 DDR2–700	-3.3 DDR2–600	Units	Notes
CAS Latency	CL_{min}	CL=6	450	400	350	300	t_{CK}	
		CL=5	400	400	350	300		
Clock Cycle Time	t_{CKmin}	CL=6	2.2	2.5	2.86	3.3	ns	
		CL=5	2.5	2.5	2.86	3.3		
Active to Read or Write delay	t_{RCDmin}		15	15	15	15	ns	
Active to Active / Auto-Refresh command period	t_{RCmin}		60	60	60	60	ns	
Active bank A to Active bank B command delay	t_{RRDmin}		7.5	7.5	7.5	7.5	ns	
Active to Precharge Command	t_{RASmin}		45	45	45	45	ns	
Precharge Command Period	t_{RPmin}		15	15	15	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	t_{RFCmin}		75	75	75	75	ns	

6.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "week" or "strong" termination can be selected. The current consumption for any terminated input pin depends on weather the input pin is in tri-state or driving "0" or "1", as long a ODT is enabled during a given period of time. See **Table 43**.

Table 43 ODT current per terminated input pin:

ODT Current		EMRS(1) State	min.	typ.	max.	Unit
Enabled ODT current per DQ added I_{DDQ} current for ODT enabled; ODT is HIGH; Data Bus inputs are floating	I_{ODTO}	A6 = 0, A2 = 1	5	6	7.5	mA/DQ
		A6 = 1, A2 = 0	2.5	3	3.75	mA/DQ
Active ODT current per DQ added I_{DDQ} current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are stable or switching.	I_{ODTT}	A6 = 0, A2 = 1	10	12	15	mA/DQ
		A6 = 1, A2 = 0	5	6	7.5	mA/DQ

Note: For power consumption calculations the ODT duty cycle has to be taken into account.

7 Electrical Characteristics & AC Timing - Absolute Specification

Table 44 Timing Parameters for HYB18T256161AF-22/-25 [1)]

Symbol	Parameter		–2.2 DDR2–900		–2.5 DDR2–800		Unit	Notes
			Min.	Max.	Min.	Max.		
f_{CK}	Clock Frequency	CL=5	125	400	125	400	MHz	
		CL=6	125	450	125	400	MHz	
t_{AC}	DQ output access time from CK / $\overline{CK}$		–0.45	0.45	–0.50	0.50	ns	
t_{DQSCK}	DQS output access time from CK / $\overline{CK}$		–0.45	0.45	–.500	.500	ns	
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	t_{CK}	
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	t_{CK}	
t_{HP}	Clock half period		min (t_{CL}, t_{HP})	—	min (t_{CL}, t_{HP})	—	t_{CK}	
t_{IS}	Address and control input setup time		0.65	—	0.70	—	ns	2)
t_{IH}	Address and control input hold time		0.65	—	0.70	—	ns	2)
t_{DS}	DQ and DM input setup time		0.345	—	0.375	—	ns	2)
t_{DH}	DQ and DM input hold time		0.345	—	0.375	—	ns	2)
t_{IPW}	Address and control input pulse width (each input)		0.60	—	0.60	—	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)		0.35	—	0.35	—	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK / $\overline{CK}$		—	t_{ACmax}	—	t_{ACmax}	ps	
$t_{LZ(DQ)}$	DQ low-impedance time from CK / $\overline{CK}$		$2 \times t_{ACmin}$	t_{ACmax}	$2 \times t_{ACmin}$	t_{ACmax}	ps	
$t_{LZ(DQS)}$	DQS low-impedance from CK / $\overline{CK}$		t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ps	
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)		—	320	—	350	ps	
t_{QHS}	Data hold skew factor		—	320	—	350	ps	
t_{QH}	Data output hold time from DQS		$t_{HP}–t_{QHS}$	—	$t_{HP}–t_{QHS}$	—		
t_{DQSS}	Write command to 1st DQS latching transition		WL – 0.25	WL +0.25	WL – 0.25	WL +0.25	t_{CK}	
t_{DQSH}	DQS input low (high) pulse width (write cycle)		0.35	—	0.35	—	t_{CK}	
t_{DQSL}	DQS input low (high) pulse width (write cycle)		0.35	—	0.35	—	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.20	—	0.20	—	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.20	—	0.20	—	t_{CK}	
t_{MRD}	Mode register set command cycle time		2	—	2	—	t_{CK}	
t_{WPRE}	Write preamble		0.25	—	0.25	—	t_{CK}	
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}	
t_{RPRE}	Read preamble		0.90	1.10	0.90	1.10	t_{CK}	
t_{RPST}	Read postamble			0.60	0.40	0.60	t_{CK}	
t_{RAS}	Active to Precharge command		45	70000	45	70000	ns	
t_{RC}	Active to Active/Auto-Refresh command period		60	—	60	—	ns	
t_{RFC}	Auto-Refresh to Active/Auto-Refresh command period		75	—	75	—	ns	

Table 44 Timing Parameters for HYB18T256161AF-22/-25 [1)]

Symbol	Parameter	–2.2 DDR2–900		–2.5 DDR2–800		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{RCD}	Active to Read or Write delay (with and without Auto-Precharge)	—	—	15	—	ns	
t_{RP}	Precharge command period	16	—	15	—	ns	
t_{RRD}	Active bank A to Active bank B command period	9	—	7.5	—	ns	
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B command period	2	—	2	—	t_{CK}	
t_{WR}	Write recovery time	14	—	15	—	ns	
t_{DAL}	Auto-Precharge write recovery + precharge time	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
t_{WTR}	Internal Write to Read command delay	7.5	—	7.5	—	ns	
t_{RTP}	Internal Read to Precharge command delay	7.5	—	7.5	—	ns	
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)	2	—	2	—	t_{CK}	
t_{XARDS}	Exit active power-down mode to Read command (slow exit, lower power)	6 - AL	—	6 - AL	—	t_{CK}	
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)	2	—	2	—	t_{CK}	
t_{XSRD}	Exit Self-Refresh to Read command	200	—	200	—	t_{CK}	
t_{XSNR}	Exit Self-Refresh to non-Read command	t_{RFC} + 10	—	t_{RFC} + 10	—	ns	
t_{CKE}	CKE minimum high and low pulse width	3	—	3	—	t_{CK}	
t_{REFI}	Average periodic refresh Interval	—	7.8	—	7.8	μs	3)
		—	3.9	—	3.9	μs	4)
t_{OIT}	OCD drive mode output delay	0	12	0	12	ns	
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{IS}+t_{CK}+t_{IH}$	—	$t_{IS}+t_{CK}+t_{IH}$	—	ns	

1) All parameters are based on V_{DD} 2.0 V ± 0.1 V
2) timing is based on signal to V_{REF}-crossing
3) 0°C - 85°C
4) 85°C and above

Table 45 Timing Parameters for HYB18T256161AF-28/-33 [1)]

Symbol	Parameter		–2.8 DDR2–700		–3.3 DDR2–600		Unit	Notes
			Min.	Max.	Min.	Max.		
f_{CK}	Clock Frequency	CL=5	125	350	125	300	MHz	
		CL=6	125	350	125	300	MHz	
t_{AC}	DQ output access time from CK / $\overline{CK}$		–0.55	0.55	–0.60	0.60	ns	
t_{DQSCK}	DQS output access time from CK / $\overline{CK}$		–.550	.550	–.600	.600	ns	
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	t_{CK}	
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	t_{CK}	

Table 45 Timing Parameters for HYB18T256161AF-28/-33 [1)]

Symbol	Parameter	–2.8 DDR2–700		–3.3 DDR2–600		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{HP}	Clock half period	min (t_{CL}, t_{HP})	—	min (t_{CL}, t_{HP})	—	t_{CK}	
t_{IS}	Address and control input setup time	0.75	—	0.80	—	ns	2)
t_{IH}	Address and control input hold time	0.75	—	0.80	—	ns	2)
t_{DS}	DQ and DM input setup time	0.400	—	0.425	—	ns	2)
t_{DH}	DQ and DM input hold time	0.400	—	0.425	—	ns	2)
t_{IPW}	Address and control input pulse width (each input)	0.60	—	0.60	—	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	—	0.35	—	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK / $\overline{CK}$	—	t_{ACmax}	—	t_{ACmax}	ps	
$t_{LZ(DQ)}$	DQ low-impedance time from CK / $\overline{CK}$	$2 \times t_{ACmin}$	t_{ACmax}	$2 \times t_{ACmin}$	t_{ACmax}	ps	
$t_{LZ(DQS)}$	DQS low-impedance from CK / $\overline{CK}$	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ps	
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)	—	350	—	350	ps	
t_{QHS}	Data hold skew factor	—	350	—	350	ps	
t_{QH}	Data output hold time from DQS	$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—		
t_{DQSS}	Write command to 1st DQS latching transition	WL – 0.25	WL +0.25	WL – 0.25	WL +0.25	t_{CK}	
t_{DQSH}	DQS input low (high) pulse width (write cycle)	0.35	—	0.35	—	t_{CK}	
t_{DQSL}	DQS input low (high) pulse width (write cycle)	0.35	—	0.35	—	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.20	—	0.20	—	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.20	—	0.20	—	t_{CK}	
t_{MRD}	Mode register set command cycle time	2	—	2	—	t_{CK}	
t_{WPRE}	Write preamble	0.25	—	0.25	—	t_{CK}	
t_{WPST}	Write postamble	0.40	0.60	0.40	0.60	t_{CK}	
t_{RPRE}	Read preamble	0.90	1.10	0.90	1.10	t_{CK}	
t_{RPST}	Read postamble	0.40	0.60	0.40	0.60	t_{CK}	
t_{RAS}	Active to Precharge command	45	70000	45	70000	ns	
t_{RC}	Active to Active/Auto-Refresh command period	60	—	60	—	ns	
t_{RFC}	Auto-Refresh to Active/Auto-Refresh command period	75	—	75	—	ns	
t_{RCD}	Active to Read or Write delay (with and without Auto-Precharge)	15	—	15	—	ns	
t_{RP}	Precharge command period	15	—	15	—	ns	
t_{RRD}	Active bank A to Active bank B command period	7.5	—	7.5	—	ns	
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B command period	2	—	2	—	t_{CK}	
t_{WR}	Write recovery time	15	—	15	—	ns	

Table 45 Timing Parameters for HYB18T256161AF-28/-33 [1)]

Symbol	Parameter	–2.8 DDR2–700		–3.3 DDR2–600		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{DAL}	Auto-Precharge write recovery + precharge time	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
t_{WTR}	Internal Write to Read command delay	7.5	—	7.5	—	ns	
t_{RTP}	Internal Read to Precharge command delay	7.5	—	7.5	—	ns	
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)	2	—	2	—	t_{CK}	
t_{XARDS}	Exit active power-down mode to Read command (slow exit, lower power)	6 - AL	—	6 - AL	—	t_{CK}	
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)	2	—	2	—	t_{CK}	
t_{XSRD}	Exit Self-Refresh to Read command	200	—	200	—	t_{CK}	
t_{XSNR}	Exit Self-Refresh to non-Read command	t_{RFC} + 10	—	t_{RFC} + 10	—	ns	
t_{CKE}	CKE minimum high and low pulse width	3	—	3	—	t_{CK}	
t_{REFI}	Average periodic refresh Interval	—	7.8	—	7.8	μs	3)
		—	3.9	—	3.9	μs	4)
t_{OIT}	OCD drive mode output delay	0	12	0	12	ns	
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{IS}+t_{CK}+t_{IH}$	—	$t_{IS}+t_{CK}+t_{IH}$	—	ns	

1) All parameters are based on V_{DD} 2.0 V ± 0.1 V
2) timing is based on signal to V_{REF}-crossing
3) 0°C - 85°C
4) 85°C and above

Table 46 Timing Parameters for HYB18T256161AFL25/L28/L33 [1)]

Symbol	Parameter		–2.5 DDR2–800		–2.8 DDR2–700		–3.3 DDR2–600		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
f_{CK}	Clock Frequency	CL=5	125	400	125	350	125	300	MHz	
		CL=6	125	400	125	350	125	300	MHz	
t_{AC}	DQ output access time from CK / $\overline{CK}$		–0.50	0.50	–0.55	0.55	–0.60	0.60	ns	
t_{DQSCK}	DQS output access time from CK / $\overline{CK}$		–.500	.500	–.550	.550	–.600	.600	ns	
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
t_{HP}	Clock half period		min (t_{CL}, t_{HP})	—	min (t_{CL}, t_{HP})	—	min (t_{CL}, t_{HP})	—	t_{CK}	
t_{IS}	Address and control input setup time		0.70	—	0.75	—	0.80	—	ns	2)
t_{IH}	Address and control input hold time		0.70	—	0.75	—	0.80	—	ns	2)
t_{DS}	DQ and DM input setup time		0.375	—	0.400	—	0.425	—	ns	2)

Table 46 Timing Parameters for HYB18T256161AFL25/L28/L33 [1)]

Symbol	Parameter	–2.5 DDR2–800		–2.8 DDR2–700		–3.3 DDR2–600		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{DH}	DQ and DM input hold time	0.375	—	0.400	—	0.425	—	ns	2)
t_{IPW}	Address and control input pulse width (each input)	0.60	—	0.60	—	0.60	—	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	—	0.35	—	0.35	—	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK / $\overline{CK}$	—	t_{ACmax}	—	t_{ACmax}	—	t_{ACmax}	ps	
$t_{LZ(DQ)}$	DQ low-impedance time from CK / $\overline{CK}$	$2 \times t_{ACmin}$	t_{ACmax}	$2 \times t_{ACmin}$	t_{ACmax}	$2 \times t_{ACmin}$	t_{ACmax}	ps	
$t_{LZ(DQS)}$	DQS low-impedance from CK / $\overline{CK}$	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ps	
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)	—	350	—	350	—	350	ps	
t_{QHS}	Data hold skew factor	—	350	—	350	—	350	ps	
t_{QH}	Data output hold time from DQS	$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—		
t_{DQSS}	Write command to 1st DQS latching transition	WL – 0.25	WL +0.25	WL – 0.25	WL +0.25	WL – 0.25	WL +0.25	t_{CK}	
t_{DQSH}	DQS input low (high) pulse width (write cycle)	0.35	—	0.35	—	0.35	—	t_{CK}	
t_{DQSL}	DQS input low (high) pulse width (write cycle)	0.35	—	0.35	—	0.35	—	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.20	—	0.20	—	0.20	—	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.20	—	0.20	—	0.20	—	t_{CK}	
t_{MRD}	Mode register set command cycle time	2	—	2	—	2	—	t_{CK}	
t_{WPRE}	Write preamble	0.25	—	0.25	—	0.25	—	t_{CK}	
t_{WPST}	Write postamble	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	
t_{RPRE}	Read preamble	0.90	1.10	0.90	1.10	0.90	1.10	t_{CK}	
t_{RPST}	Read postamble	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	
t_{RAS}	Active to Precharge command	45	70000	45	70000	45	70000	ns	
t_{RC}	Active to Active/Auto-Refresh command period	60	—	60	—	60	—	ns	
t_{RFC}	Auto-Refresh to Active/Auto-Refresh command period	75	—	75	—	75	—	ns	
t_{RCD}	Active to Read or Write delay (with and without Auto-Precharge)	15	—	15	—	15	—	ns	
t_{RP}	Precharge command period	15	—	15	—	15	—	ns	

Table 46 Timing Parameters for HYB18T256161AFL25/L28/L33 [1)]

Symbol	Parameter	–2.5 DDR2–800		–2.8 DDR2–700		–3.3 DDR2–600		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RRD}	Active bank A to Active bank B command period	7.5	—	7.5	—	7.5	—	ns	
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B command period	2	—	2	—	2	—	t_{CK}	
t_{WR}	Write recovery time	15	—	15	—	15	—	ns	
t_{DAL}	Auto-Precharge write recovery + precharge time	WR + t_{RP}	—	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
t_{WTR}	Internal Write to Read command delay	7.5	—	7.5	—	7.5	—	ns	
t_{RTP}	Internal Read to Precharge command delay	7.5	—	7.5	—	7.5	—	ns	
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)	2	—	2	—	2	—	t_{CK}	
t_{XARDS}	Exit active power-down mode to Read command (slow exit, lower power)	6 - AL	—	6 - AL	—	6 - AL	—	t_{CK}	
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)	2	—	2	—	2	—	t_{CK}	
t_{XSRD}	Exit Self-Refresh to Read command	200	—	200	—	200	—	t_{CK}	
t_{XSNR}	Exit Self-Refresh to non-Read command	t_{RFC} + 10	—	t_{RFC} + 10	—	t_{RFC} + 10	—	ns	
t_{CKE}	CKE minimum high and low pulse width	3	—	3	—	3	—	t_{CK}	
t_{REFI}	Average periodic refresh Interval	—	7.8	—	7.8	—	7.8	µs	3)
		—	3.9	—	3.9	—	3.9	µs	4)
t_{OIT}	OCD drive mode output delay	0	12	0	12	0	12	ns	
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{IS}+t_{CK}+t_{IH}$	—	$t_{IS}+t_{CK}+t_{IH}$	—	$t_{IS}+t_{CK}+t_{IH}$	—	ns	

1) All parameters are based on V_{DD} 1.8 V ± 0.1 V
2) timing is based on signal to V_{REF}-crossing
3) 0°C - 85°C
4) 85°C and above

8 AC Timing Measurement Conditions

8.1 Reference Load for Timing Measurements

Figure 63 represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally a coaxial transmission line terminated at the tester electronics. This reference load is also used for output slew rate characterization. The output timing reference voltage level for single ended signals is the crosspoint with V_{TT}.

The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. $\overline{\text{DQS}}$) signal.

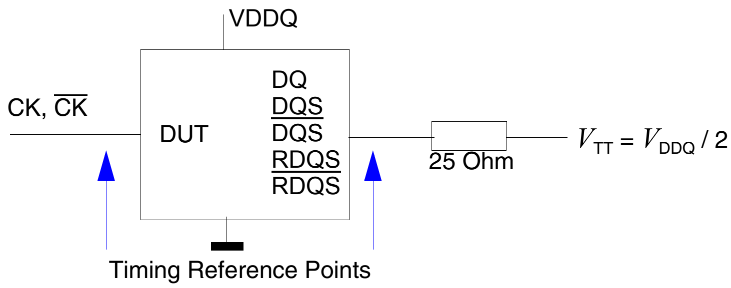


Figure 63 Reference Load for Timing Measurements

8.2 Slew Rate Measurement Conditions

8.2.1 Output Slewrate

With the reference load for timing measurements output slew rate for falling and rising edges is measured between V_{TT} – 250 mV and V_{TT} + 250 mV for single ended signals.

For differential signals (DQS / $\overline{\text{DQS}}$) output slew rate is measured between DQS - $\overline{\text{DQS}}$ = 500 mV and DQS – $\overline{\text{DQS}}$ = –500 mV. Output Slew Rate is defined with the reference load according to **Figure 63** and verified by design and characterization, but not subject to production testt.

8.2.2 Input Slewrate - Differential signals

Input slewrate for differential signals (CK / $\overline{\text{CK}}$, DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$) for rising edges are measured from CK - $\overline{\text{CK}}$ = –250 mV to CK – $\overline{\text{CK}}$ = +500 mV and from CK – $\overline{\text{CK}}$ = +250 mV to CK – $\overline{\text{CK}}$ = –500mV for falling edges.

8.2.3 Input Slewrate - Single ended signals

Input slew rate for single ended signals (other than t_{IS}, t_{IH}, t_{DS} and t_{DH}) are measured from dc-level to ac-level: V_{REF} –125 mV to V_{REF} + 250 mV for rising edges and from V_{REF} + 125 mV to V_{REF} – 250 mV for falling edges. For slew rate definition of the input and data setup and hold parameters see **Chapter 8.3** of this data sheet.

8.3 Input and Data Setup and Hold Time

8.3.1 Timing Definition for Input Setup (t_{IS}) and Hold Time (t_{IH})

Address and control input setup time (t_{IS}) is referenced from the input signal crossing at the $V_{IH(ac)}$ level for a rising signal and $V_{IL(ac)}$ for a falling signal applied to the device under test. Address and control input hold time (t_{IH}) is referenced from the input signal crossing at the $V_{IL(dc)}$ level for a rising signal and $V_{IH(dc)}$ for a falling signal applied to the device under test.

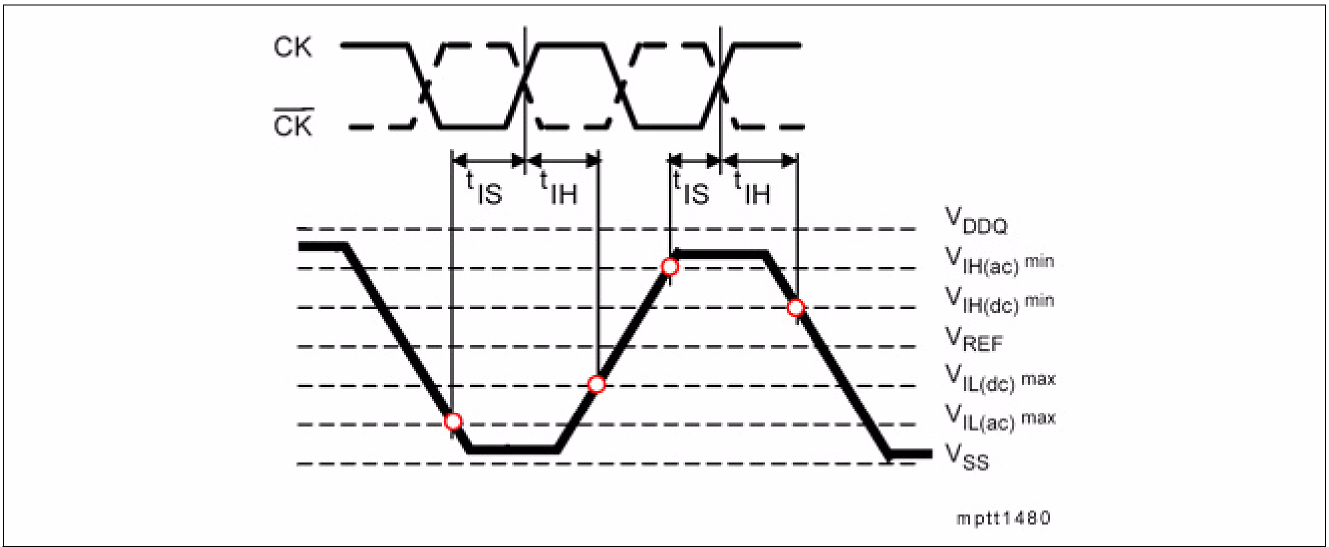


Figure 64 Timing Definition for Input Setup (tIS) and Hold Time (tIH)

8.3.2 Definition for Data Setup (t_{DS}) and Hold Time (t_{DH}), differential Data Strobes

Data input setup time (t_{DS}) with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test.

DQS/$\overline{\text{DQS}}$ signals must be monotonic between $V_{IL(dc).MAX}$ and $V_{IH(dc).MIN}$. Data input hold time (t_{DH}) with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IL(dc)}$ level to the differential data strobe crosspoint for a rising signal and $V_{IH(dc)}$ to the differential data strobe crosspoint for a falling signal applied to the device under test.

DQS/$\overline{\text{DQS}}$ signals must be monotonic between $V_{IL(dc).MAX}$ and $V_{IH(dc.MIN}$.

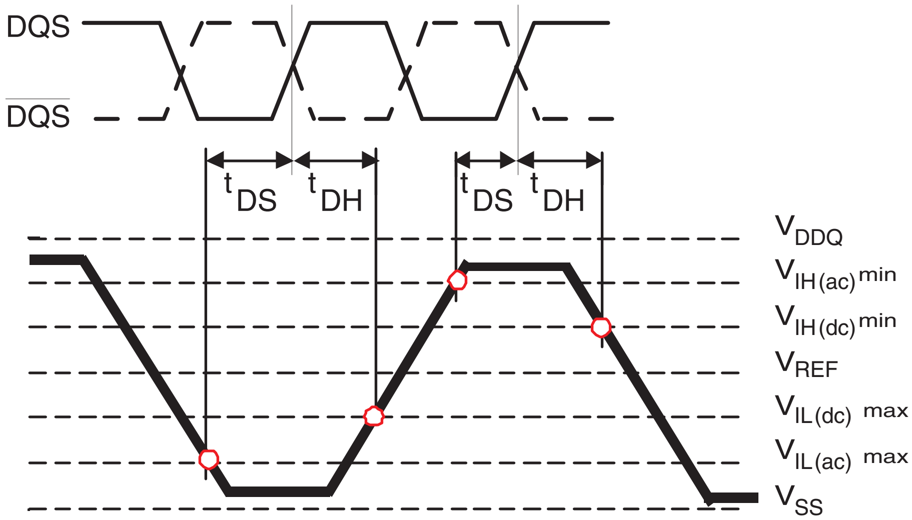


Figure 65 Data, Setup and Hold Time Diagram (Differential Data Strobes)

8.3.3 Definition for Data Setup (t_{DS1}) and Hold Time (t_{DH1}), Single-Ended Data Strobes

Data input setup time (t_{DS1}) with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a falling signal applied to the device under test.

Data input hold time ($_{tDH1}$) with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the $V_{IH(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a rising signal and from the input signal crossing at the $V_{IL(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a falling signal applied to the device under test.

The DQS signal must be monotonic between $V_{IL(dc.MAX}$ and $V_{IH(dc).MIN}$.

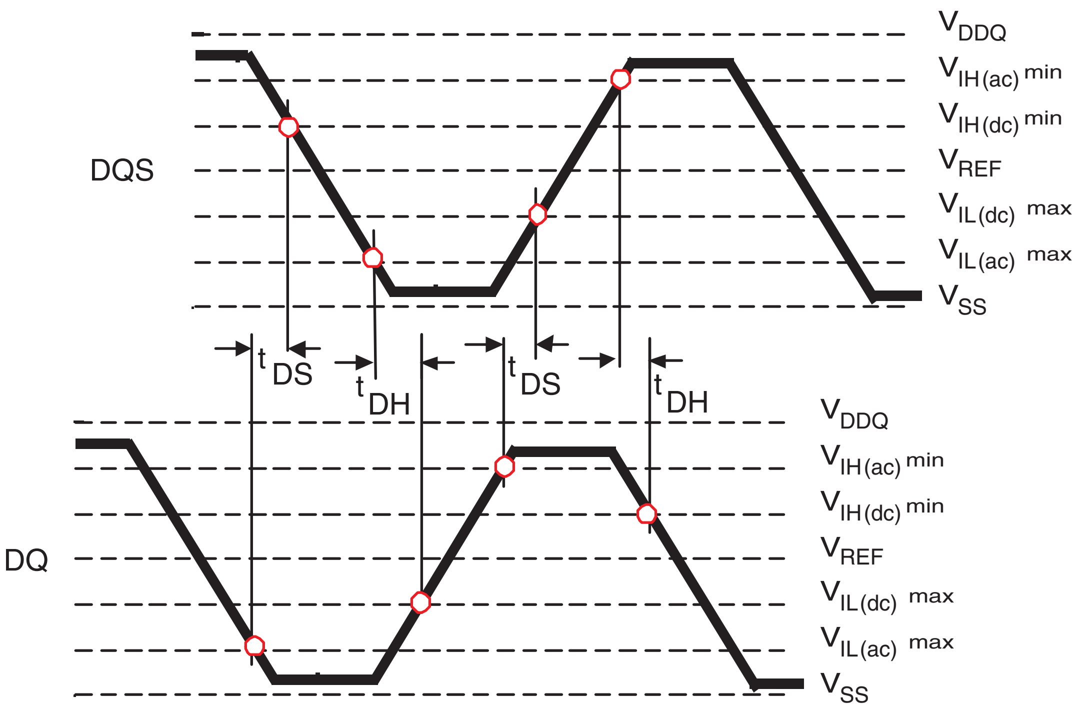


Figure 66 Data Setup and Hold Time (Single Ended Data Strobes)

8.3.4 Slew Rate Definition for Input and Data Setup and Hold Times

Setup (t_{IS} & t_{DS}) nominal Slew Rate for a rising signal is defined as the Slew Rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac).MIN}$. Setup (t_{IS} & t_{DS}) nominal Slew Rate for a falling signal is defined as the Slew Rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac).MAX}$. If the actual signal is always earlier than the nominal Slew Rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal Slew Rate for derating value (see **Figure 67**). If the actual signal is later than the nominal Slew Rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the Slew Rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.(see **Figure 68**) Hold (t_{IH} & t_{DH}) nominal Slew Rate for a rising signal is defined as the Slew Rate between the last crossing of $V_{IL(dc).MAX}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{IH} & t_{DH}) nominal Slew Rate for a falling signal is defined as the Slew Rate between the last crossing of $V_{IH(dc).MIN}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal Slew Rate line between shaded 'dc to V_{REF} region', use nominal Slew Rate for derating value (see **Figure 67**). If the actual signal is earlier than the actual signal from the dc level to V_{REF} level is used for derating value (see **Figure 68**)

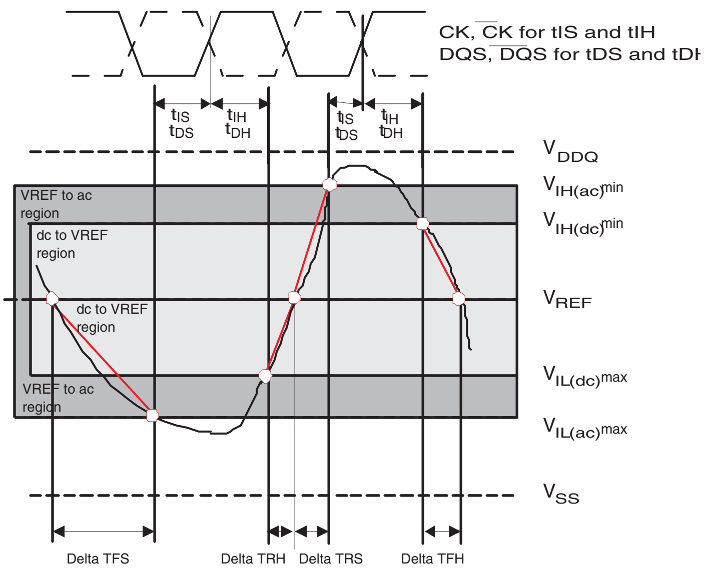


Figure 67 Slew Rate Definition Nominal

Note:

$$\text{Setup Slew Rate} = \frac{\text{VREF(dc) - VIL(ac)max}}{\text{Delta TFS}} \quad \text{falling signal}$$

$$\text{Setup Slew Rate} = \frac{\text{VIH(ac)min - VREF(dc)}}{\text{Delta TRS}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{VREF(dc) - VIL(dc)max}}{\text{Delta TRH}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{VIH(dc)min - VREF(dc)}}{\text{Delta TFH}} \quad \text{falling signal}$$

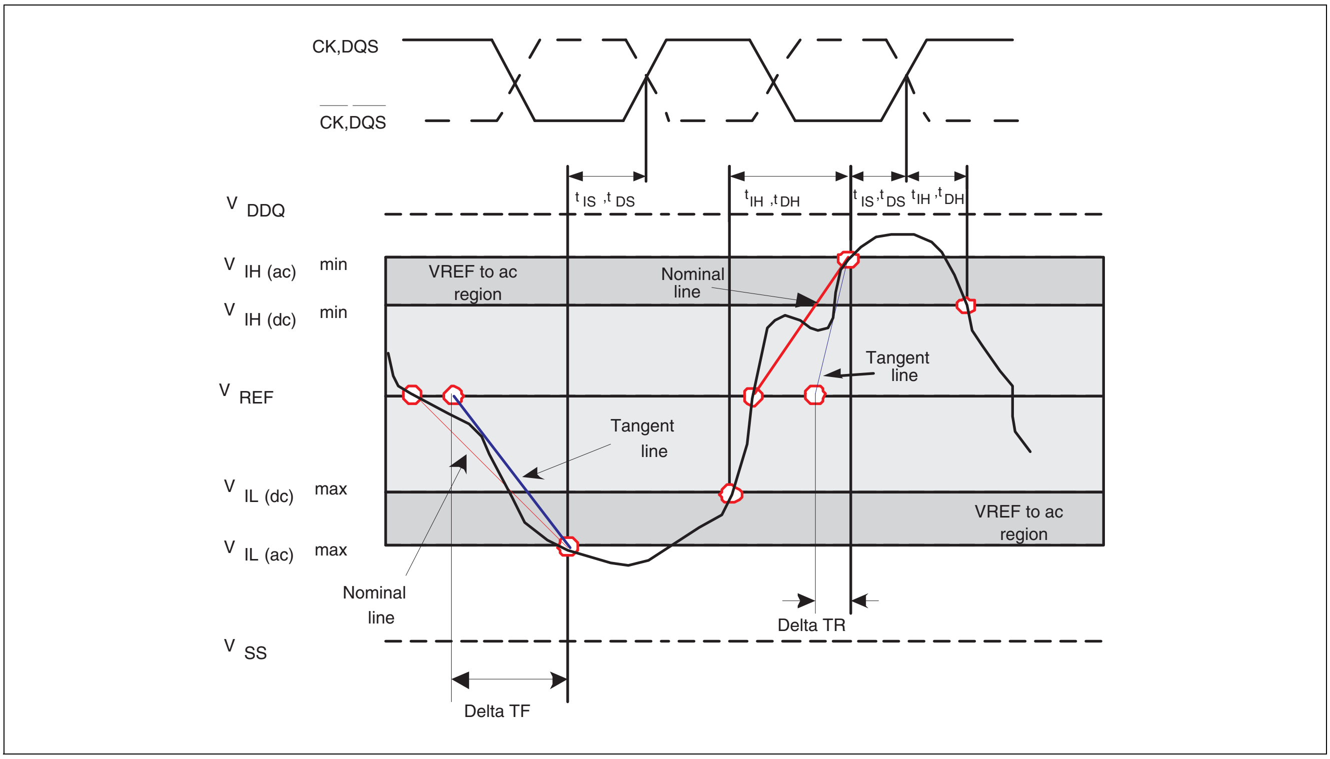


Figure 68 Slew Rate Definition Tangent

Note:

$$\text{Setup Slew Rate} = \frac{\text{tangent line [VREF(dc) - VIL(ac)max]}}{\text{Delta TFS}}$$ falling signal

$$\text{Setup Slew Rate} = \frac{\text{tangent line [VIH(ac)min - VREF(dc)]}}{\text{Delta TRS}}$$ rising signal

$$\text{Hold Slew Rate} = \frac{\text{tangent line [VREF(dc) - VIL(dc)max]}}{\text{Delta TRH}}$$ rising signal

$$\text{Hold Slew Rate} = \frac{\text{tangent line [VIH(dc)min - VREF(dc)]}}{\text{Delta TFH}}$$ falling signal

8.3.5 Setup (t_{IS}) and Hold (t_{IH}) Time Derating Tables

1. For all input signals the total input setup time and input hold time required is calculated by adding the data sheet value to the derating value respectively. Example: t_{IS}(total setup tine) = t_{IS}(base) + Δ t_{IS}
2. For slow Slew Rate the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH(ac)}$ / $V_{IL(ac)}$ at the time of the rising clock) a valid input signal is still required to complete the transition and reach $V_{IH(ac)}$ / $V_{IL(ac)}$. For Slew Rates in between the values listed in the next tables, the derating values may be obtained by linear interpolation. These values are not subject to production test. They are verified only by design and characterization.

Table 47 Input Setup (t_{IS}) and Hold (t_{IH}) Time Derating Values

Command / Address Slew Rate (V/ns)	CK, $\overline{CK}$ Differential Slew Rate						Unit	Note
	2.0 V/ns		1.5 V/ns		1.0 V/ns			
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}		
4.0	+187	+94	+217	+124	+247	+154	ps	1)
3.5	+179	+89	+209	+119	+239	+149	ps	1)
3.0	+167	+83	+197	+113	+227	+143	ps	1)
2.5	+150	+75	+180	+105	+210	+135	ps	1)
2.0	+125	+45	+155	+75	+185	+105	ps	1)
1.5	+83	+21	+113	+51	+143	+81	ps	1)
1.0	0	0	+30	+30	+60	+60	ps	1)
0.9	–11	–14	+19	+16	+49	+46	ps	1)
0.8	–25	–31	+5	–1	+35	+29	ps	1)
0.7	–43	–54	–13	–24	+17	+6	ps	1)
0.6	–67	–83	–37	–53	–7	–23	ps	1)
0.5	–110	–125	–80	–95	–50	–65	ps	1)
0.4	–175	–188	–145	–158	–115	–128	ps	1)
0.3	–285	–292	–255	–262	–225	–232	ps	1)
0.25	–350	–375	–320	–345	–290	–315	ps	1)
0.2	–525	–500	–495	–470	–465	–440	ps	1)
0.15	–800	–708	–770	–678	–740	–648	ps	1)
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps	1)

1) For all input signals t_{IS}(total) = t_{IS}(base) + Δt_{IS} and t_{IH}(total) = t_{IH}(base) + Δt_{IH}

Table 48 Data Setup (t_{DS}) and Hold Time (t_{DH}) Derating Values for Differential DQS/$\overline{DQS}$[1)2)]

DQ Slew Rate (V/ns)	DQS, $\overline{DQS}$ Differential Slew Rate																	
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}	Δ t_{DS}	Δ t_{DH}
2.0	+125	+45	+125	+45	+125	+45	—	—	—	—	—	—	—	—	—	—	—	—
1.5	+83	+21	+83	+21	+83	+21	+95	+33	—	—	—	—	—	—	—	—	—	—
1.0	0	0	0	0	0	0	+12	+12	+24	+24	—	—	—	—	—	—	—	—
0.9	—	—	–11	–14	–11	–14	+1	–2	+13	+10	+25	+22	—	—	—	—	—	—
0.8	—	—	—	—	–25	–31	–13	–19	–1	–7	+11	+5	+23	+17	—	—	—	—
0.7	—	—	—	—	—	—	–31	–42	–19	–30	–7	–18	+5	–6	+17	+6	—	—
0.6	—	—	—	—	—	—	—	—	–43	–49	–31	–47	–19	–35	–7	–23	+5	–11
0.5	—	—	—	—	—	—	—	—	—	—	–74	–89	–62	–77	–50	–65	–38	–53
0.4	—	—	—	—	—	—	—	—	—	—	—	—	–127	–140	–115	–128	–103	–116

1) All units in ps.
2) For all input signals t_{DS}(total) = t_{DS}(base) + Δt_{DS} and t_{DH}(total) = t_{DH}(base) + Δt_{DH}

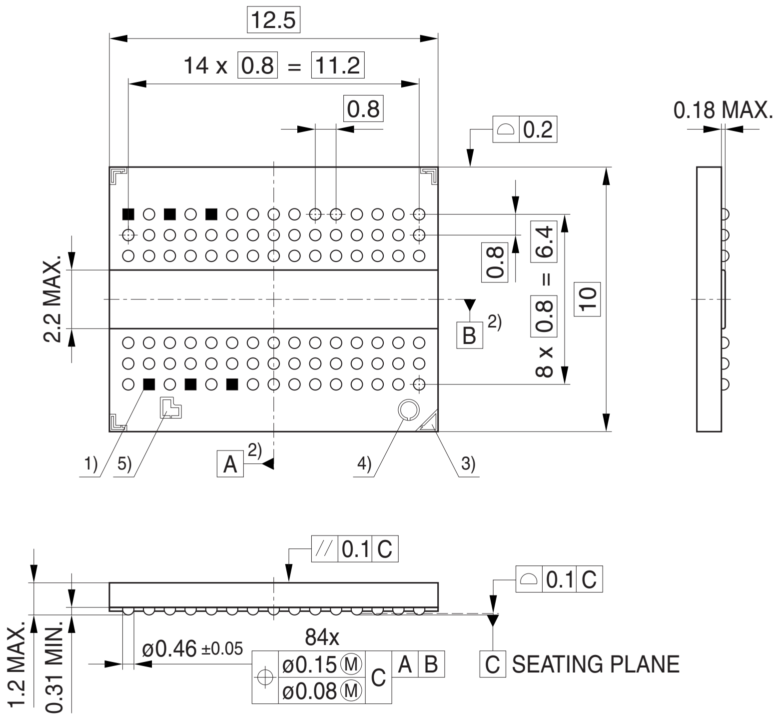
Table 49 Data Setup (t_{DS}) and Hold Time (t_{DH}) Derating Values for Single Ended DQS[1)2)3)]

DQ Slew Rate (V/ns)	DQS Single-ended Slew Rate																	
	2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
	Δ t_{D1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}	Δ t_{DS1}	Δ t_{DH1}
2.0	+125	+45	+125	+45	+125	+45	-	-	-	-	-	-	-	-	-	-	-	-
1.5	+83	+21	+83	+21	+83	+21	+95	+33	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	+12	+12	+24	+24	-	-	-	-	-	-	-	-
0.9	-	-	-11	-14	-11	-14	+1	-2	+13	+10	+25	+22	-	-	-	-	-	-
0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	+11	+5	+23	+17	-	-	-	-
0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	+5	-6	+17	+6	-	-
0.6	-	-	-	-	-	-	-	-	-43	-49	-31	-47	-19	-35	-7	-23	+5	-11
0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

1) All units in ps.
2) For all input signals t_{DS1}(total) = t_{DS1}(base) + Δt_{DS1} and t_{DH1}(total) = t_{DH1}(base) + Δt_{DH1}
3) For slow Slew Rate the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH(ac)}$ / $V_{IL(ac)}$ at the time of the rising DQS) a valid input signal is still required to complete the transition and reach $V_{IH(ac)}$ / $V_{IL(ac)}$. For Slew Rates in between the values listed in the table, the derating values may be obtained by linear interpolation. These values are not subject to production test. They are verified only by design and characterization.

9 Package

9.1 Package Outline



1) Dummy pads without ball ■
2) Middle of packages edges
3) Package orientation mark A1
4) Bad unit marking (BUM)
5) Die sort fiducial

9.2 Package Thermal Characterist

Table 50 T-FBGA-84 package thermal resistance

ODT Current	Theta-jA 1)						Theta-jL2)	Theta-jC3)
Jedec Board	1 s0p			2s2p				
Air Flow	0 m/s	1 m/s	3 m/s	0 m/s	1 m/s	3 m/s	–	–
R_{tH} K/W	69	53	47	41	35	33	18	5

1) Theta-jA: Junction to ambient thermal resistance. The values have been obtained by simulating using the conditions stated in the JEDEC JESD-51 standard.
2) Theta_jL: Junction to Lead thermal resistance (not according JESD-51). The value has been obtained by simulation.
3) Theta_jC: Junction to Case thermal resistance. The value has been obtained by simulation.

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