HYUNDAI
SEMICONDUCTOR

HY27C64
8192×8-Bit CMOS UV EPROM

DESCRIPTION

The HY27C64 is a high speed 65,536-bit UV erasable and electrically reprogrammable CMOS EPROM fabricated using high-performance HYCMOS technology, ideally suited for applications where low power, high speed, and fast turnaround are important requirements.

Two-line control and JEDEC-approved, 28 pin packaging are standard features of the HY27C64. This ensures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between non-volatile memory alternatives.

And to satistify our customer's requirements, Plastic OTP (One-Time-Programmable) ROM is available.

FEATURES

- ▲ **CMOS**
- ▲ **Fast access time—150/200/300ns**
- ▲ **Low power consumption—CMOS inputs**
  - **—Active : 30 mA (Max.)**
  - **—Standby: 100 μA (Max.)**
- ▲ **Single 5V (±10%) power supply**
- ▲ **Two-line control**
- ▲ **Smart programming algorithm**
  - **—Fast EPROM programming**
- ▲ **Silicon Identification code**
  - **—For automated programming operations**
- ▲ **TTL compatible inputs/outputs**
- ▲ **Compatible with 2764, 27128, 27256**

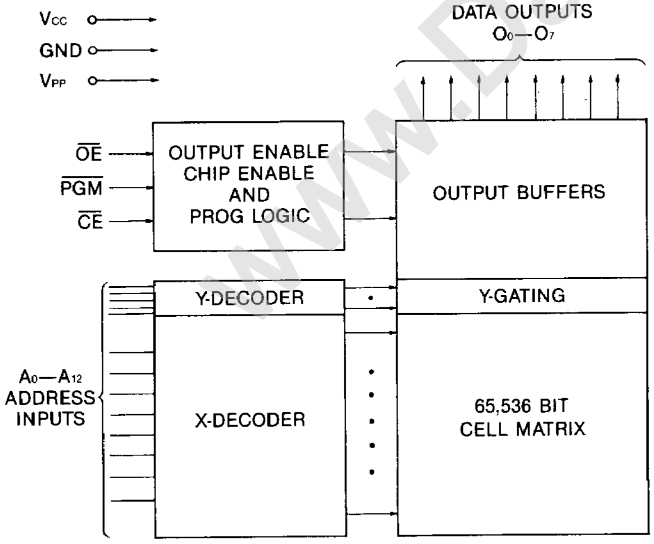
SELECTION GUIDE

PART NUMBER	ACCESS TIME
HY27C64D/P15	150ns
HY27C64D/P20	200ns
HY27C64D/P30	300ns

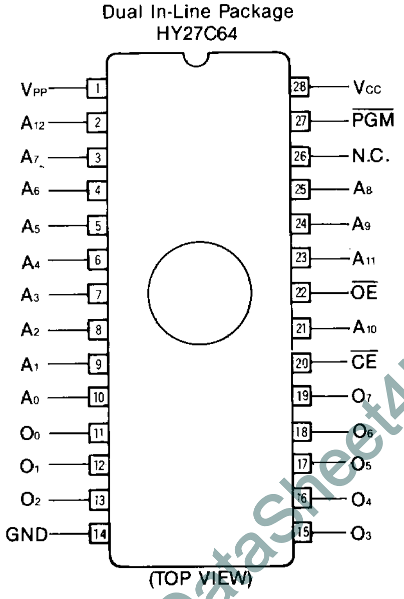
PIN NAMES

A_0—A_{12}	Addresses	Vpp	Programming Voltage
O_0—O_7	Outputs	V_{CC}	Power Supply (+5V)
$\overline{CE}$	Chip Enable	GND	Ground
$\overline{OE}$	Output Enable	N.C.	No Connection
$\overline{PGM}$	Program		

BLOCK DIAGRAM



PIN CONNECTIONS



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ABSOLUTE MAXIMUM RATINGS[1]

Ambient Temperature Under Bias (Commercial)	−10°C to +85°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC}+0.6V to GND-0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+13.5V to −0.6V
Voltage on Pin 24 with Respect to Ground	+14.0V to −0.6V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 1. MODE SELECTION

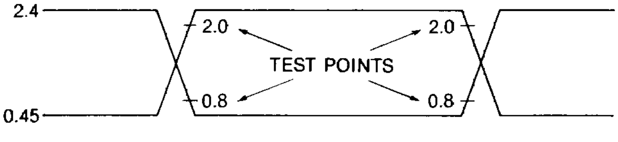
PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{OUT}
Program	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Mfg. Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code

Notes: 1. X can be V_{IH} or V_{IL} 2. V_H=12.0±0.5V

AC TEST CONDITIONS

Output Load	1 TTL Gate and C_L=100pF
Input Rise and Fall Times (10% to 90%)	≤20ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V to 2.0V
Outputs	0.8V to 2.0V

AC TESTING INPUT/OUTPUT WAVEFORM



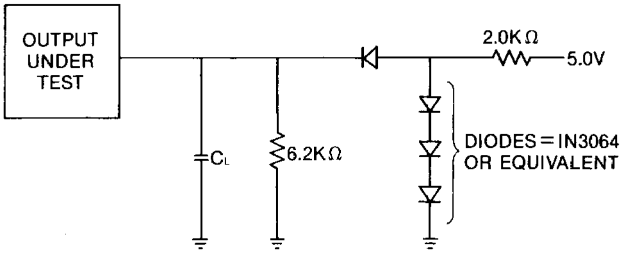
AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 AND 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1 AND 0.8V FOR A LOGIC 0.

OPERATING RANGES

Temperature Range	0°C to +70°C
V_{CC} Supply Voltages	
HY27C64 D/P15,20	+4.5V to +5.5V
HY27C64 D/P 30	+4.75V to +5.25V
V_{PP} Voltage	+12.2 V to +13.3 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

AC TESTING LOAD CIRCUIT



C_L=100pF, including jig capacitance.

CAPACITANCE[1]

T_A=25°C, f=1.0MHz

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{in}	Input Capacitance	V_{IN}=0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V		8	12	pF

1. This parameter is sampled and not 100% tested.

READ OPERATION
DC ELECTRICAL CHARACTERISTICS

DC and Operating Characteristics over operating ranges unless otherwise specified

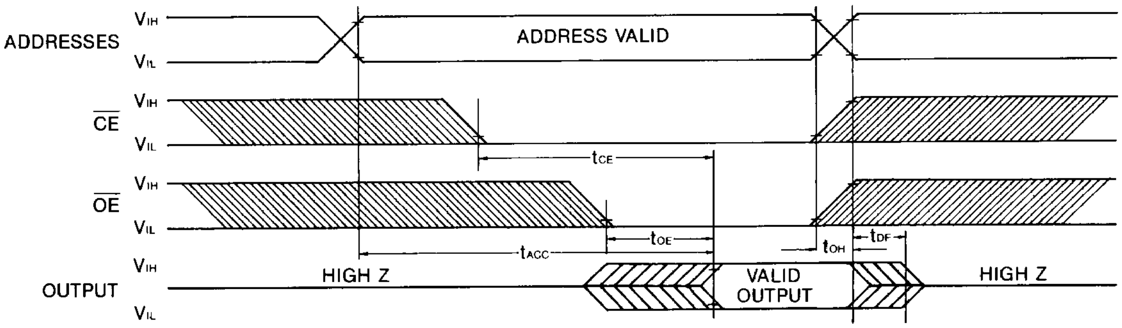
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{CE}=V_{IH}$			10	μA
I_{CC1}	Vcc Current (Active) TTL Inputs	$\overline{OE}=\overline{CE}=V_{IL}$ Inputs=V_{IH} or V_{IL} f=5MHz, I/O=0 mA			40	mA
I_{CC2}	Vcc Current (Active) CMOS Inputs	$\overline{OE}=\overline{CE}=GND\pm0.3V$ Inputs=GND±0.3V or Vcc±0.3V f=5MHz, I/O=0 mA			30	mA
I_{SB1}	Vcc Current (Standby) TTL Inputs	$\overline{CE}=V_{IH}$			1	mA
I_{SB2}	Vcc Current (Standby) CMOS Inputs	$\overline{CE}=V_{CC}\pm0.3V$			100	μA
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		Vcc+1	V
V_{OL1}	Output Low Voltage	$I_{OL}=2.1$ mA			0.45	V
V_{OH1}	Output High Voltage	$I_{OH}=-400$ μA	2.4			V
V_{OL2}	Output Low Voltage CMOS Outputs	$I_{OL}=0$ μA			0.1	V
V_{OH2}	Output High Voltage CMOS Outputs	$I_{OH}=0$ μA	Vcc-0.1			V

AC ELECTRICAL CHARACTERISTICS

AC Characteristics over operating ranges unless otherwise specified

Symbol	Parameter	Test Conditions	HY27C64-15			HY27C64-20			HY27C64-30			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	$\overline{CE}=\overline{OE}=V_{IL}$			150			200			300	ns
t_{CE}	Chip Enable to Output Delay	$\overline{OE}=V_{IL}$			150			200			300	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}=V_{IL}$			65			65			120	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE}=V_{IL}$	0		55	0		55	0		105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first	$\overline{CE}=\overline{OE}=V_{IL}$	0			0			0			ns

TIMING DIAGRAMS OF READ OPERATION



PROGRAMMING OPERATION DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 12.2V$ to $13.3V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4			V
I_{CC2}	V_{CC} Supply Current	(Program & Verify)			30	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $\overline{PGM} = V_{IL}$			30	mA

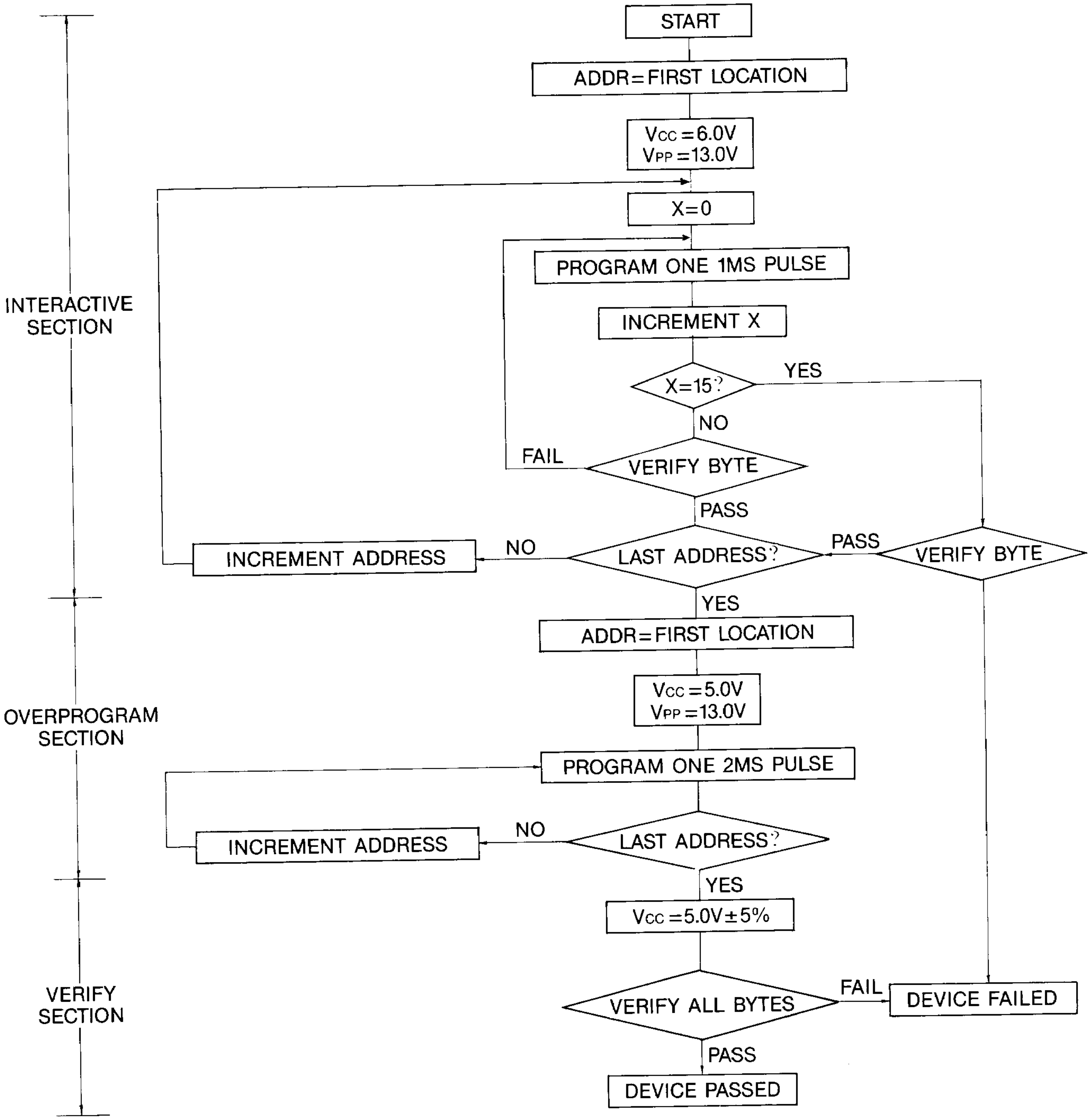
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-up Time		2			µs
t_{OES}	$\overline{OE}$ Set-up Time		2			µs
t_{DS}	Data Set-up Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay				130	µs
t_{VPS}	V_{PP} Set-up Time		2			µs
t_{VCS}	V_{CC} Set-up Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width		1.95	2.0	55	ms
t_{CES}	$\overline{CE}$ Set-up Time		2			µs
t_{OE}	Data Valid from $\overline{OE}$				150	µs

AC TEST CONDITIONS

V_{CC}		6.0V±0.25V
V_{PP}		12.2V to 13.3V
Input Rise and Fall Times (10% to 90%)		≤20ns
Input Pulse Levels		0.45V to 2.4V
Timing Measurement Reference Level	Inputs	0.8V to 2.0V
	Outputs	0.8V to 2.0V

INTERACTIVE PROGRAMMING FLOW CHART



FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The seven modes of operation of the HY27C64 are listed in table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} during programming and 12V on A_9 for the identifier mode.

READ MODE

The HY27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

STANDBY MODE

The device has a standby mode which reduces the maximum current from 40 mA to 1 mA (TTL Levels)/30 mA to 100 μA (CMOS Levels). The device is placed in standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR—TYING

Because EPROMs are usually used in large memory arrays, the HY27C64 is provided with a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

1) the lowest possible memory power dissipation, and
2) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of high speed CMOS EPROMs require CAREFUL DECOUPLING of the devices. The supply current, I_{CC} has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of the Chip Enable. The magnitude of these transient peaks is dependent on the output capacitive loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array of devices. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

ERASURE CHARACTERISTICS

The erasure characteristics of the HY27C64 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 400 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000—4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase that typical HY27C64 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the HY27C64 window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 Wsec/cm. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose a HY27C64 can be exposed to without damage is 7258 Wsec/cm (1 week @ 12000 μW/cm). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

PROGRAMMING MODES

CAUTION: Exceeding 14.0V on pin 1 (V_{PP}) will permanently damage the HY27C64.

Initially, and after each erasure, all bits of the device are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} input is at 12.5V, and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

IDENTIFIER MODE

The identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacture and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C±5°C ambient temperature range that is required when programming the HY27C64.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 (pin 24) of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the Identifier Mode.

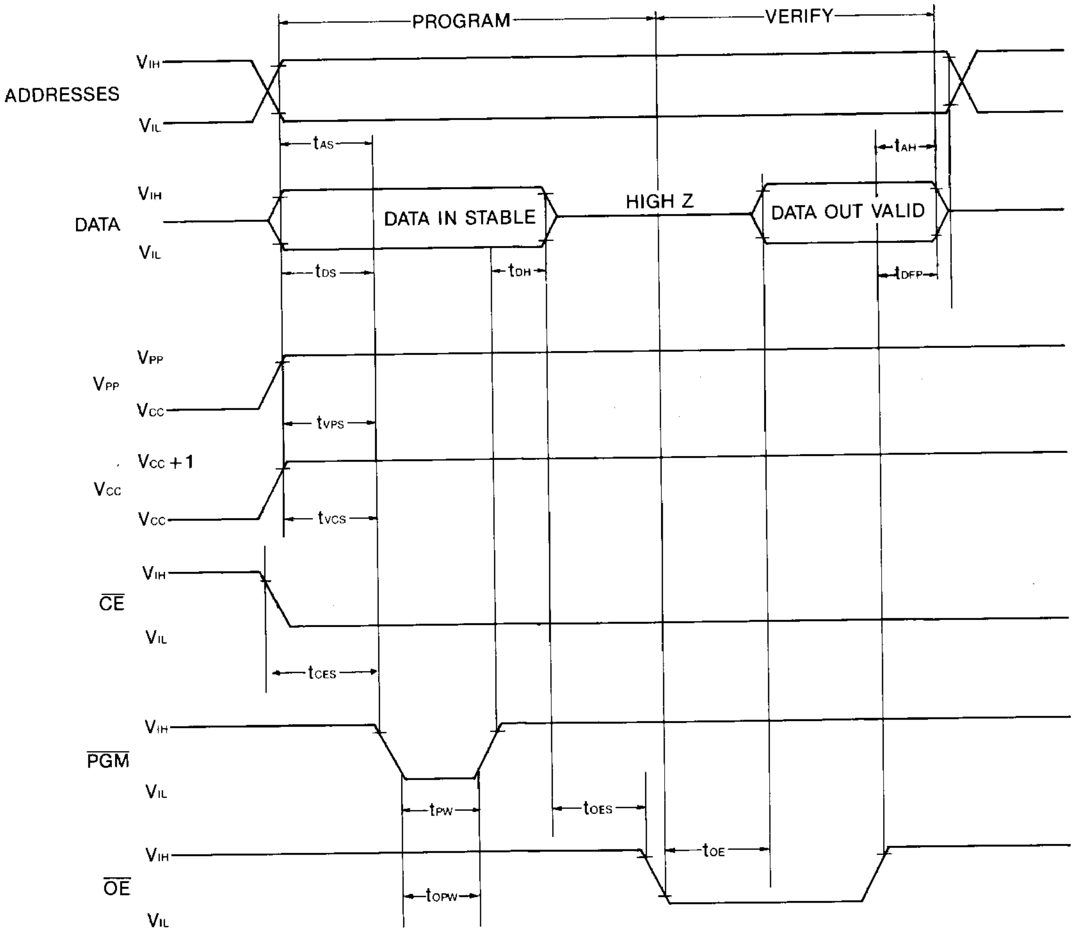
Byte 0 ($A_0=V_{IL}$) represents the manufacturer code and byte 1 ($A_0=V_{IH}$) the device identifier code. For the HY27C64, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

TABLE 2. HY27C64 IDENTIFIER BYTES

Identifier \ Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer	V_{IL}	1	0	1	0	0	1	1	1	A7
Device Code	V_{IH}	0	0	0	0	1	0	0	0	08

Notes: 1. A_9=12.0±0.5V
2. A_0—A_8, A_{10}—A_{12}, $\overline{CE}$, $\overline{OE}$=V_{IL}
3. PER JEDEC Pub. 106

TIMING DIAGRAMS OF PROGRAMMING OPERATION

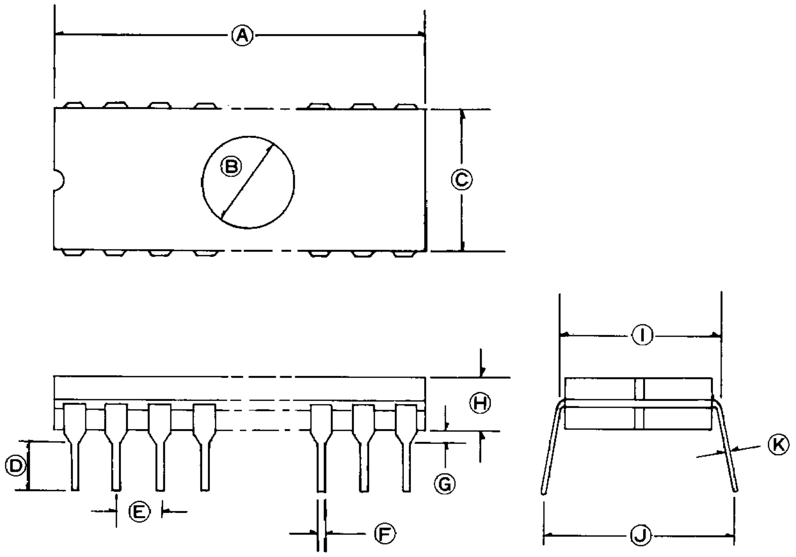


NOTES:
1. THE INPUT TIMING REFERENCE LEVEL IS 0.8V FOR V_{IL} AND 2.0V FOR V_{IH}.
2. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
3. WHEN PROGRAMMING THE HY27C64, A 0.1 µF CAPACITOR IS REQUIRED ACROSS V_{PP} AND GROUND TO SUPPRESS SPURIOUS VOLTAGE TRANSIENTS WHICH CAN DAMAGE THE DEVICE.

PHYSICAL DIMENSIONS

28-Lead EPROM CERDIP

DIM	Inches			Millimeters		
	Min	Typ	Max	Min	Typ	Max
A	1.446		1.474	36.728		37.440
B		0.280			7.112	
C	0.517		0.538	13.132		13.665
D	0.125		0.145	3.175		3.683
E		0.100			2.540	
F	0.016		0.020	0.406		0.508
G	0.020			0.508		
H	0.140		0.175	3.556		4.445
I	0.608		0.614	15.443		15.596
J	0.630		0.700	16.002		17.780
K		0.010			0.254	



ORDERING INFORMATION

Part Number: HY27C64XXX

Speed

15=150ns

20=200ns

30=300ns

Package

D: Cerdip

P: Plastic Dip

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