DATA SHEET

(DOC No. HX8817A-DS)

HX8817A

TCON with YUV Input and DAC

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1. General Description

The HX8817A is a TFT-LCD timing controller with 8-bit serial RGB, 18-bit parallel RGB, ITU-R BT. 656 and BT. 601 input interfaces. With the built-in color space conversion circuit, DAC, and operational amplifiers, this controller performs gamma correction and polarity inverted function to convert digital data into line inversion, analog amplified RGB signals for TFT-LCD panel. It also provides horizontal and vertical control timing to TFT-LCD source and gate drivers with 8 different zoom in/zoom out display modes on different display resolutions.

2. Features

- Interlaced YUV 4:2:2 input video signal compliant with ITU-R BT. 601 (8-bit YCbCr) and ITU-R BT. 656 standards
- Support 2 port of ITU-R BT. 656 or 601 8-bit inputs
- Support 8-bit serial RGB input
- Support 18-bit parallel RGB input
- Support NTSC/PAL TV system
- Support 4 different horizontal resolutions, 480, 960, 1200, and 1440
- Built-in gamma correction function
- Provide source and gate drivers control timing
- Built-in 8 zoom in/zoom out display modes
- Shift clock signals for the source driver (3-ϕ clock)
- Provide flip and mirror scan control
- Built-in 2 channel PWM DC-DC booster control circuit for VGH and VGL
- Digital IO voltage: 3.3V or 5.0V
- Operation voltage: 5.0V
- 64 pin LQFP

3. Block Diagram

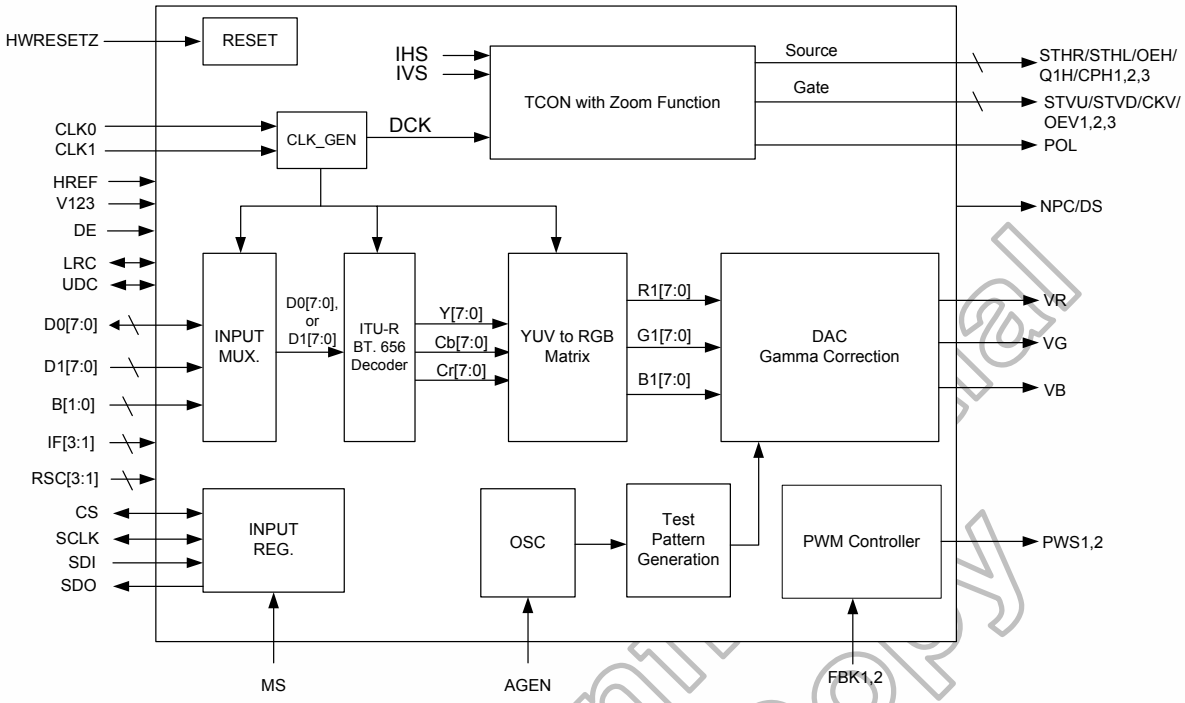


Figure 3. 1 Block diagram

4. Pin Assignment

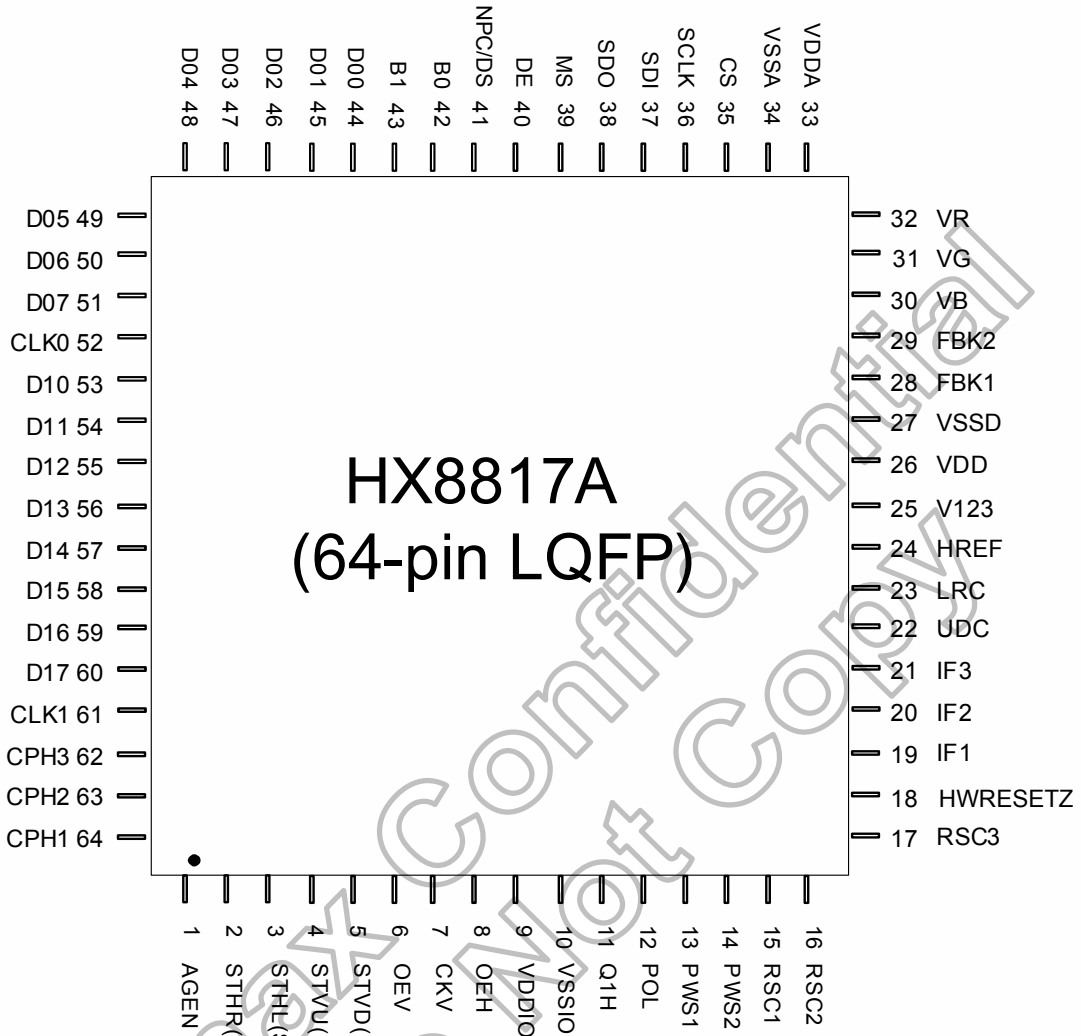


Figure 4. 1 Pin assignment

5. Pin Description

Pin no.	Symbol	I/O	Description
1	AGEN	I	Test pin for aging. (a) Aging with test pattern and prior display when AGEN=”H” (b) Normal operation when AGEN=”L”
2	STHR	O	Start pulse for source driver. (a) STHR is ”HiZ”, when LRC=”H” (b) STHR is ”Output”, when LRC=”L”
3	STHL	O	Start pulse for source driver. (a) STHL is ”HiZ”, when LRC=”L” (b) STHL is ”Output”, when LRC=”H”
4	STVU	O	Start pulse for gate driver. (a) STVU is “HiZ”, when UDC=”H” (b) STVU is ”Output”, when UDC=”L”
5	STVD	O	Start pulse for gate driver. (a) STVD is ”HiZ”, when UDC=”L” (b) STVD is ”Output”, when UDC=”H”
6	OEV	O	Gate driver output enable control
7	CKV	O	Shift clock for gate driver
8	OEH	O	Source driver output enable control
9	VDDIO	-	3.3V IO power
10	VSSIO	-	Ground
11	Q1H	O	R, G, B video signals sample & hold multiplexer control signal for source driver in delta color arrangement modes
12	POL	O	Toggling signal for common electrode generation circuits
13	PWS1	O	Pulse width modulation signal 1
14	PWS2	O	Pulse width modulation signal 2
15	RSC1(1)	I	Resolution mode setting pin 1
16	RSC2(1)	I	Resolution mode setting pin 2
17	RSC3(1)	I	Resolution mode setting pin 3
18	HWRESETZ	I	Active low global reset signal input
19	IF1(2)	I	Interface select pin 1
20	IF2(2)	I	Interface select pin 2
21	IF3(2)	I	Interface select pin 3
22	UDC	I/O	Up / Down scan setting. Default bit EXT2=1, UDC is input; otherwise EXT2=0, UDC is output. (a) Normal scan, when UDC=”L” (b) Reverse scan, when UDC=”H”
23	LRC	I/O	Left / Right scan setting. Default bit EXT2=1, LRC is input; otherwise EXT2=0, LRC is output. (a) Normal scan, when LRC=”H” (b) Reverse scan, when LRC=”L”
24	HREF	I	Horizontal reference input for ITU-R BT. 601 I/F Or HSYNC for digital RGB interface
25	V123	I	Vertical reference input for ITU-R BT. 601 I/F Or VSYNC for digital RGB interface
26	VDD	-	Power (5V)
27	VSSD	-	Ground
28	FBK1	I	PWM feedback voltage. Connect “H” when not used.
29	FBK2	I	PWM feedback voltage. Connect “L” when not used.

Pin no.	Symbol	I/O	Description
30	VB	O	Analog blue signal output
31	VG	O	Analog green signal output
32	VR	O	Analog red signal output
33	VDDA	-	Analog power (5V)
34	VSSA	-	Analog ground
35	CS	I/O	Chip Select (a) CS is output when MS="H" (b) CS is input when MS="L"
36	SCLK	I/O	3-Wire Serial bus clock (a) SCLK is output when MS="H" (b) SCLK is input when MS="L"
37	SDI	I	3-Wire Serial bus data input.
38	SDO	O	3-Wire Serial bus data output.
39	MS	I	Master mode selection for serial interface (a) Master mode when MS="H" (b) Slave mode when MS="L"
40	DE	I	DE for 8-bit/18-bit digital RGB interface
41	NPC/DS	O	NTSC/PAL output pin when register DS=0 (a) NTSC mode when NPC="H" (b) PAL mode when NPC="L" Dual Scan output for zoom modes when bit DS=1
42	B0	I	B0 for 18 bits RGB input mode
43	B1	I	B1 for 18 bits RGB input mode
44	D00	I	Digital image data input port 0 bit0 or B2
45	D01	I	Digital image data input port 0 bit1 or B3
46	D02	I	Digital image data input port 0 bit2 or B4
47	D03	I	Digital image data input port 0 bit3 or B5
48	D04	I	Digital image data input port 0 bit4 or G0
49	D05	I	Digital image data input port 0 bit5 or G1
50	D06	I	Digital image data input port 0 bit6 or G2
51	D07	I	Digital image data input port 0 bit7 or G3
52	CLK0	I	27MHz Main input clock for port 0
53	D10	I	Digital image data input port 1 bit0 or G4
54	D11	I	Digital image data input port 1 bit1 or G5
55	D12	I	Digital image data input port 1 bit2 or R0
56	D13	I	Digital image data input port 1 bit3 or R1
57	D14	I	Digital image data input port 1 bit4 or R2
58	D15	I	Digital image data input port 1 bit5 or R3
59	D16	I	Digital image data input port 1 bit6 or R4
60	D17	I	Digital image data input port 1 bit7 or R5
61	CLK1	I	27MHz Main input clock for port 1 or CLK for 8-bit/18-bit digital RGB interface
62	CPH3	O	Shift clock $\phi 3$ for source driver
63	CPH2	O	Shift clock $\phi 2$ for source driver
64	CPH1	O	Shift clock $\phi 1$ for source driver

Table 5. 1 Pin description

Note: (1) Resolution setting

RSC3	RSC2	RSC1	Resolution mode(H × V)
L	L	L	480 × 234 Delta
L	L	H	960 × 234 Delta
L	H	L	-
L	H	H	-
H	L	L	-
H	L	H	960 × 234 Stripe
H	H	L	1200 × 234 Stripe
H	H	H	1440 × 234 Stripe

Table 5. 2 Resolution setting

Note: (2) Interface setting

IF3	IF2	IF1	Interface
L	L	L	656 port 0 (D00~D07, CLK0)
L	L	H	656 port 1 (D10~D17, CLK1)
L	H	L	601 8-bit port 0 (D00~D07, CLK0, HREF, V123)
L	H	H	601 8-bit port 1(D10~D17, CLK1, HREF, V123)
H	L	L	Digital RGB 8-bit (D00~D07, CLK0, HS, VS, DE)
H	L	H	Digital RGB 8-bit (D10~D17, CLK1, HS, VS, DE)
H	H	L	-
H	H	H	Digital RGB 18-bit (R5~R0, G5~G0, B5~B0, CLK1, HS, VS, DE)

Table 5. 3 Interface setting

6. Functional Description

6.1 Register settings

Panel setup (R0h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	EXT1	RSTB0	IIF3	IIF2	IIF1	RES3	RES2	RES1
Default	1	1	0	0	0	1	1	1

Table 6. 1 Panel setup (R0h)

EXT1: Selects external pins (EXT1=1) or internal registers (EXT1=0) to setup interface and resolution.

EXT1	Interface Setting	Resolution Setting
1	External pins (IF1, IF2 IF3 pin)	External pins (RSC1, RSC2, RSC3 pin)
0	Internal register (IIF1, IIF2 IIF3 bit)	Internal register (RSC1, RSC2, RSC3 bit)

Table 6. 2 EXT1 setting

RSTB0: Firmware reset. Low enable.

IIF3~IIF1: Set input port and interface type and ignore pin 19~21 when EXT1=0.

IIF3	IIF2	IIF1	Interface
L	L	L	656 port 0 (D00~D07, CLK0)
L	L	H	656 port 1 (D10~D17, CLK1)
L	H	L	601 8-bit port 0 (D00~D07, CLK0, HREF, V123)
L	H	H	601 8-bit port 1 (D10~D17, CLK1, HREF, V123)
H	L	L	Digital RGB 8-bit (D00~D07, CLK0, HS, VS, DE)
H	L	H	Digital RGB 8-bit (D10~D17, CLK1, HS, VS, DE)
H	H	L	-
H	H	H	Digital RGB 18-bit (R5~R0, G5~G0, B5~B0, CLK1, HS, VS, DE)

Table 6. 3 Interface setting

RES3~RES1: Set display resolution and ignore pin 15~17 when EXT1=0.

RES3	RES2	RES1	Resolution mode(H × V)
L	L	L	480 × 234 Delta
L	L	H	960 × 234 Delta
L	H	L	-
L	H	H	-
H	L	L	-
H	L	H	960 × 234 Stripe
H	H	L	1200 × 234 Stripe
H	H	H	1440 × 234 Stripe

Table 6. 4 Resolution setting

Functional Control 1 (R1h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	EXT2	ILRC	IUDC	VZ_mode	DS	ZX3	ZX2	ZX1
Default	1	1	0	1	0	1	1	1

Table 6. 5 Functional control (R1h)

EXT2: Selects external pins (EXT2=1) or internal registers (EXT2=0) to setup mirror and flip functions.

IUDC: Set gate driver shift direction for up/down scan setting and ignore pin 22 when EXT2=0.

ILRC: Set source driver shift direction for left/right scan setting and ignore pin 23 when EXT2=0.

EXT2	Up / Down Scan Setting	Left / Right Scan Setting
1	External pin (UDC pin is input)	External pin (LRC pin is input)
0	Internal register (IUDC bit) and UDC pin is output	Internal register (ILRC bit) and LRC pin is output

Table 6. 6 EXT2 setting

VZ_mode: Vertical zoom-in algorithm select. Set VZ=0 for UPS017 algorithm.

DS: Vertical zoom-in with gate driver with dual scan function.

ZX3~ZX1: Set display modes for 1440, 1200, 960 stripe panels with ITU-R BT 656 or 601 interfaces. In 480, 960 delta panels, or in digital RGB interfaces, only full mode can be displayed.

ZX3	ZX2	ZX1	Display Mode
H	H	H	Full
H	H	L	Zoom1
H	L	H	Zoom1-wide
H	L	L	Normal
L	H	H	Zoom2
L	H	L	Wide
L	L	H	Zoom2-wide
L	L	L	Zoom3

Table 6. 7 Display Mode setting

See functional description for detail.

Functional control 2 (R2h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	CFIN_S	OVER	PH2	PH1	OEH_S	POL_S	HREFP	VREFP
Default	1	1	1	1	1	1	1	1

Table 6. 8 Functional control2(R2h)

CFIN_S: Set delta panel's input data sequence for 8-bit digital RGB interface.
1 => odd line is RGB; even line is GBR. (AUO)
0 => odd line is RGB; even line is BRG. (PVI)

OVER: Set display period for ITU-R BT. 656 or 601 interface
1 => 53.3us of active data is displayed on the panel
0 => 50.3 us of active data is displayed on the panel

PH2~PH1: Sets delta panel's output CPH phase for ITU-R BT. 656 or 601 interface
1X => CPH for odd and even lines is in phase
01 => even line lags odd line by one half dots. (AUO)
00 => even line lags odd line by one half dots. (PVI)

OEH_S: Set OEH's polarity
1 => OEH is normal polarity (active low)
0 => OEH is opposite polarity (active high)

POL_S: Set relationship between DAC output and POL
1 => with input gray scale increasing, DAC outputs ascend while POL is "H" and descend while POL is "L"
0 => with input gray scale increasing, DAC outputs descend while POL is "H" and ascend while POL is "L"

HREFP: Set HREF polarity of ITU-R BT. 601, set 0 for reversed signal

VREFP: Set V123 polarity of for ITU-R BT. 601, 0 for reversed signal

Input Horizontal Start Position Offset (R3h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	-	-	-	HPOF4	HPOF3	HPOF2	HPOF1	HPOF0
Default	0	0	0	0	0	0	0	0

Table 6. 9 Input horizontal start position offset (R3h)

HPOF4~HPOF0: Set 8-bit RGB input data position offset.

HPOF4	HPOF3	HPOF2	HPOF1	HPOF0	Dot Steps
1	1	1	1	1	-1
1	1	1	1	0	-2
1	1	1	0	1	-3
1	1	1	0	0	-4
1	1	0	1	1	-5
1	1	0	1	0	-6
1	1	0	0	1	-7
1	1	0	0	0	-8
1	0	1	1	1	-9
1	0	1	1	0	-10
1	0	1	0	1	-11
1	0	1	0	0	-12
1	0	0	1	1	-13
1	0	0	1	0	-14
1	0	0	0	1	-15
1	0	0	0	0	-16
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

Table 6. 10 Set 8-bit RGB input data position offset

Horizontal Position (R4h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	-	-	-	HPOS4	HPOS3	HPOS2	HPOS1	HPOS0
Default	0	0	0	0	0	0	0	0

Table 6. 11 Horizontal position (R4h)

HPOS4~HPOS0: Set horizontal display position.

HPOS4	HPOS3	HPOS2	HPOS1	HPOS0	Steps
1	1	1	1	1	-1
1	1	1	1	0	-2
1	1	1	0	1	-3
1	1	1	0	0	-4
1	1	0	1	1	-5
1	1	0	1	0	-6
1	1	0	0	1	-7
1	1	0	0	0	-8
1	0	1	1	1	-9
1	0	1	1	0	-10
1	0	1	0	1	-11
1	0	1	0	0	-12
1	0	0	1	1	-13
1	0	0	1	0	-14
1	0	0	0	1	-15
1	0	0	0	0	-16
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

Table 6. 12 Set horizontal display position

Vertical Position (R5h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	-	-	-	-	VPOS3	VPOS2	VPOS1	VPOS0
Default	0	0	0	0	0	0	0	0

Table 6. 13 Vertical position (R5h)

VPOS [3:0]: Used to set the gate start position.

VPOS3	VPOS2	VPOS1	VPOS0	Line Step
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7
1	0	0	0	-8
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7

Table 6. 14 Set the gate start position

Aging Pattern (R6h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	-	PWMON	-	-	AGE3	AGE2	AGE1	AGE0
Default	0	0	0	0	1	1	1	1

Table 6. 15 Aging pattern (R6h)

PWMON: Enable PWM function.
1 => PWM enabled, see PWM booster converter for detail.
0 => PWM disabled.

AG3~AG0: Set aging pattern.

AG3	AG2	AG1	AG0	Aging Pattern
H	H	H	H	Auto-looping
H	L	H	L	Flicker
H	L	L	H	Black
H	L	L	L	Color Bar
L	H	H	H	White Grayscale
L	H	H	L	Blue Grayscale
L	H	L	H	Green Grayscale
L	H	L	L	Red Grayscale
L	L	H	H	White
L	L	H	L	Blue
L	L	L	H	Green
L	L	L	L	Red

Table 6. 16 Set aging pattern

Gamma Correction Reference 1~8 (R7h~REh)

	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Default
R7h	-	-	-	RV14	RV13	RV12	RV11	RV10	0x06
R8h	-	-	-	RV24	RV23	RV22	RV21	RV20	0x13
R9h	-	-	-	RV34	RV33	RV32	RV31	RV30	0x1C
RAh	-	-	-	RV44	RV43	RV42	RV41	RV40	0x11
RBh	-	-	-	RV54	RV53	RV52	RV51	RV50	0x15
RCh	-	-	-	RV64	RV63	RV62	RV61	RV60	0x0A
RDh	-	-	-	RV74	RV73	RV72	RV71	RV70	0x0F
REh	-	-	-	RV84	RV83	RV82	RV81	RV80	0x16

Table 6. 17 Gamma correction reference 1~8 (R7h~REh)

RVn[4:0]: Set 8 gamma correction reference voltage values for gray scale 0, 36, 72, 108, 147, 183, 219, and 255 in positive polarity separately. For RV1~RV3, output reference voltage is $\frac{RVn[4:0]}{63}\times V_{DDA}$. The register values greater than 6 (binary 00110) are recommended for RV1~RV3 to keep minimum voltage higher than 0.5V. For RV4 or RV5, output reference voltage is $\frac{RVn[4:0]+16}{63}\times V_{DDA}$. For RV6 ~ RV8, output reference voltage is $\frac{RVn[4:0]+32}{63}\times V_{DDA}$. The register values smaller than 25 (binary 11001) are recommended for RV6~RV8 to keep maximum voltage lower than 4.5V. The default gamma curve for both positive and negative polarity is shown in the following figure.

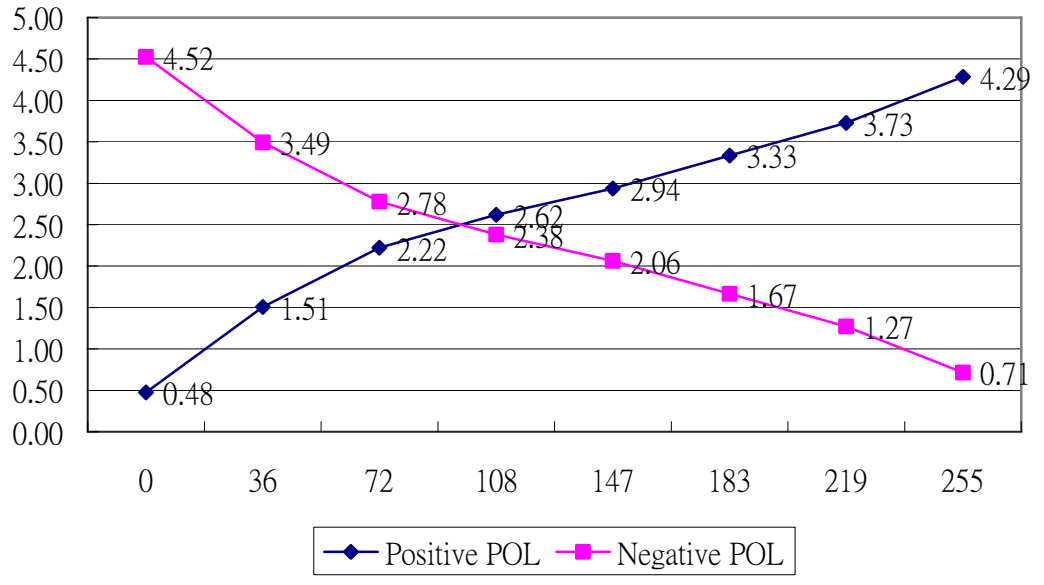


Figure 6. 1 The default gamma curve for both positive and negative polarity

FIELD Mix Mode (RFh)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	FIELDPAL1	FIELDPAL0	FIELDNTSC1	FIELDNTSC0	NPCMSEL	NPCMVAL	-	-
Default	0	1	0	0	0	1	0	0

Table 6. 18 FIELD mix mode (RFh)

FIELDPAL [1:0]: When PAL Mode, the relationship of first line in even field and odd field.
00: First line in even field = First line in odd field
01: First line in even field = First line in odd field + 1
10: No Use
11: First line in even field = First line in odd field - 1

FIELDNTSC [1:0]: When NTSC mode, the relationship of first line in even field and odd field.
00: First line in even field = First line in odd field
01: First line in even field = First line in odd field + 1
10: No Use
11: First line in even field = First line in odd field - 1

NPCMSEL: Input format select.
0: Auto detects NTSC or PAL mode.
1: NTSC or PAL mode selected by register RFh, bit 2. (NPCMVAL)

NPCMVAL: When NPCMSEL = 1, set display format by
0: PAL mode
1: NTSC mode

TESTING (R10h)

Bit	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Name	T7	T6	T5	T4	T3	T2	T1	T0
Default	0	0	0	1	0	0	1	1

Table 6. 19 TESTING (R10h)

6.2 Color space conversion

The input data should be compliant to ITU-R BT. 601 8-bit data format or ITU-R BT. 656 standards and be connected to input pins D17~D10 or D07~D00 as listed in the following table.

Signal		ITU-R BT. 601 and BT. 656			
D07	D17	CB07	Y07	CR07	Y17
D06	D16	CB06	Y06	CR06	Y16
D05	D15	CB05	Y05	CR05	Y15
D04	D14	CB04	Y04	CR04	Y14
D03	D13	CB03	Y03	CR03	Y13
D02	D12	CB02	Y02	CR02	Y12
D01	D11	CB01	Y01	CR01	Y11
D00	D10	CB00	Y00	CR00	Y10

Table 6. 20 Color space conversion

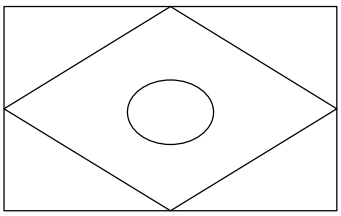
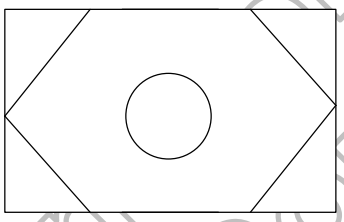
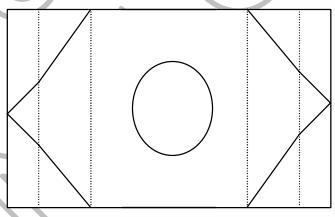
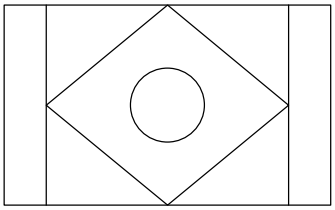
In ITU-R BT. 656 data streams the included codes are used for identifying even and odd frames, blanking and active video data. The codes start with the byte sequence FF 00 00, followed by the reference code byte. The code byte contains vertical and horizontal blanking as well as odd and even field information. The code information will be decoded internally and used for timing control.

MSB							LSB
7	6	5	4	3	2	1	0
1	F(1)	V(2)	H(3)	P3	P2	P1	P0

Note: (1) F=0: odd filed; F=1: even field.
(2) V=0: in active field lines; V=1: in field blanking.
(3) H=0: SAV (Start of Active video); H=1: EAV (End of Active video).

Table 6. 21 Color space conversion

6.3 Zoom in/out display mode setting

Display Mode	ZX1	ZX2	ZX3	Display Characteristics (4:3 aspect-ratio input signal)	Remark
Full	H	H	H		Input signals are displayed on full screen.(To display 4:3 signal on 16:9 screen)
Zoom1	L	H	H		Central 176 lines of input signals are displayed on full screen. (Vertically extension, zoom factor =4/3).
zoom-Wide1	H	L	H		Central 176 lines of input signals are displayed on full screen. (Vertically extension and different horizontal timing scaling).
Normal	L	L	H		Input signal (4:3) is displayed on center 75% screen. (4:3 aspect-ratio).

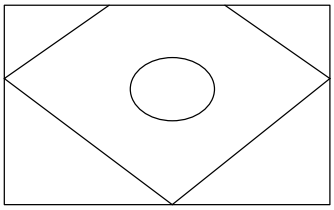
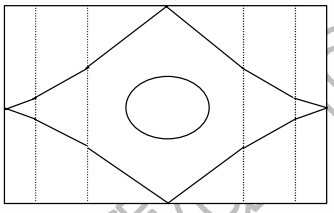
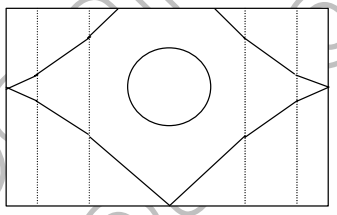
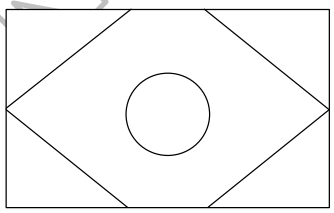
Display Mode	ZX1	ZX2	ZX3	Display Characteristics (4:3 aspect-ratio input signal)	Remark
Zoom2	H	H	L		Lower 205 lines of input signals are displayed on full screen. (Zoom factor=8/7, vertically offset extension).
Wide	L	H	L		Input signals are displayed on full screen. (Different horizontal timing scaling).
Zoom-Wide2	H	L	L		Lower 205 lines of input signal are displayed on full screen. (Vertically extension and different horizontal timing scaling).
Zoom3	L	L	L		Center 205 lines of input signal are displayed on full screen. (Vertically extension, zoom factor=8/7).

Table 6. 22 Zoom in/out display mode setting

6.4 Aging pattern generator

For simplifying TFT-LCD burn-in process, an aging pattern generator is embedded into HX8817A. In normal operation, AGEN pin should be pulled down to VSS. When AGEN pin is pulled up to VDD or no clock detected, HX8817A will operate at aging mode and generate eight sets of aging patterns including black, white, red, green, blue, gray scale(R, G, B, W), and color bar.

6.5 PWM booster converter

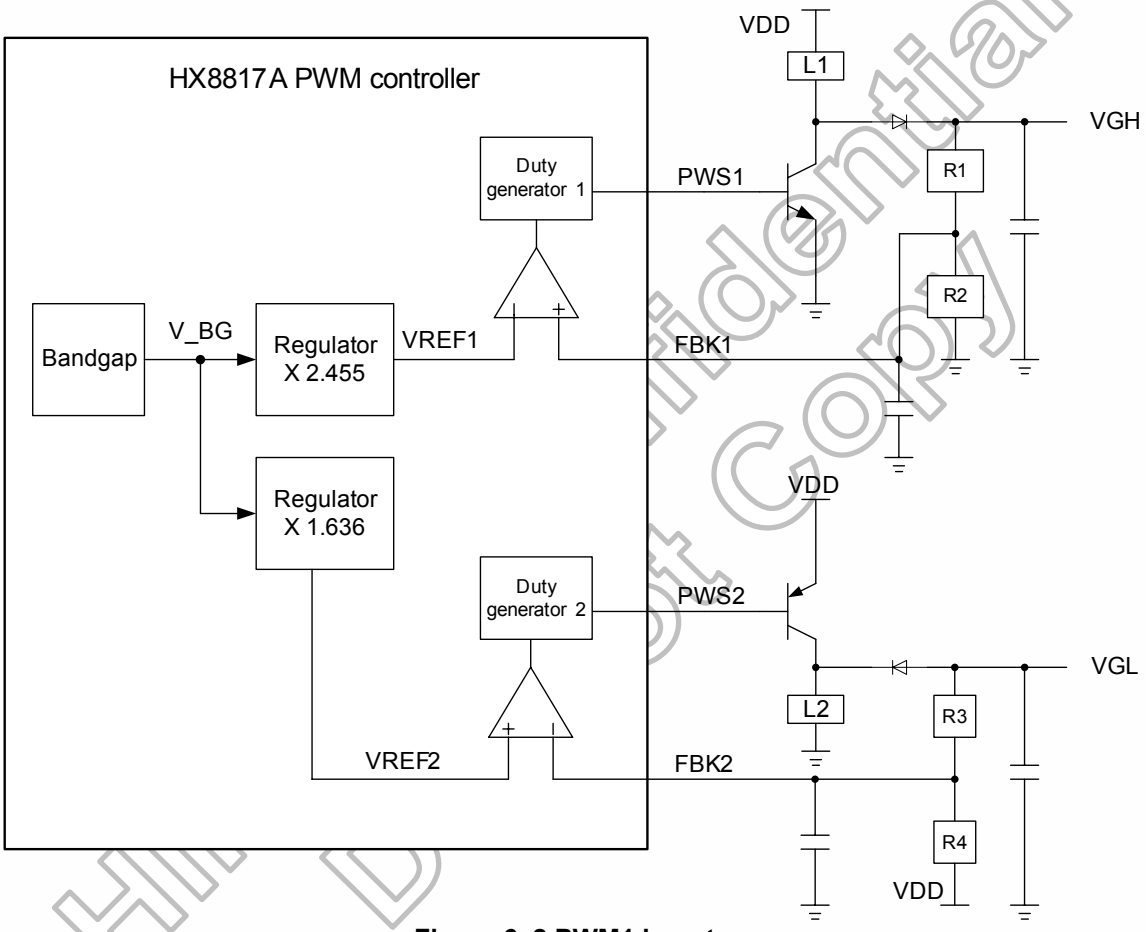


Figure 6. 2 PWM1 booster

$$VGH = VFB1 \times (1 + \frac{R1}{R2})$$

$$VGL = VFB2 \times (1 + \frac{R3}{R4}) - VDD\frac{R3}{R4}$$

The PWM boost converter can be used to generate VGH and VGL with external application circuits. The DC-DC converter is highly efficient switching voltage generator circuits that generate the high voltage level required by gate drivers. HX8817A contains 2 sets of sub-circuits of the PWM buck/boost converter, including a precision reference voltage, comparator, PWM controlling logic, and the output buffer. The boost converter uses an external power transistor to provide maximum efficiency and to minimize the number of external components. The VO output voltage level can be adjusted by R1 and R2.
Please be noted that the output pulse width modulation signal PWS1 for booster is active high, while the other signal PWS2 for buck-booster is active low. The voltage swing of PWS1 and PWS2 are both from VSSIO to VDDIO. The internal comparison voltages for feedback pin FB1 and FB2 are 3.25±0.35V and 2.2±0.35V, respectively.

6.6 Serial digital RGB mode input data sequence and color filter type

The input data sequence in serial digital RGB mode as following figures

Color filter stripe type

R	G	B	R	G	B
R	G	B	R	G	B
R	G	B	R	G	B
R	G	B	R	G	B

Scan direction	U/D	Low	Low	High	High
Shift direction	L/R	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	RGB	BGR
	Even line	RGB	BGR	RGB	BGR

Figure 6. 3 Serial digital RGB input data sequence on color filter stripe type

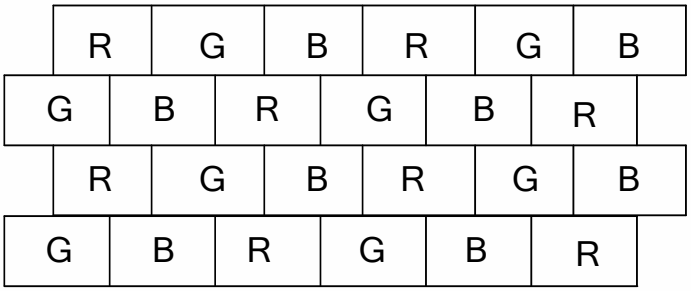
Color filter delta type 1

R	G	B	R	G	B
B	R	G	B	R	G
R	G	B	R	G	B
B	R	G	B	R	G

Scan direction	U/D	Low	Low	High	High
Shift direction	L/R	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	BRG	GRB
	Even line	BRG	GRB	RGB	BGR

Figure 6. 4 Serial digital RGB input data sequence on color filter delta type 1

Color filter delta type 2



Scan direction	U/D	Low	Low	High	High
Shift direction	L/R	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	GBR	RBG
	Even line	GBR	RBG	RGB	BGR

Figure 6. 5 Serial digital RGB input data sequence on color filter delta type 2

7. DC Characteristics

7.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply	V_{DD} (1)	-0.3	-	6.0	V
Output voltage	V_R, V_G, V_B	-0.3	-	V_{DD} +0.3	V
Storage temperature	T_{STG}	-40	-	95	ºC

Note: (1) For V_{DDD}, V_{DDA}, V_{DDIO}.

7.2 Recommended operating conditions

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply	V_{DDIO}	3	3.3	3.6	V
		4.5	5.0	5.5	V
Power supply	V_{DD}, V_{DDA}	4.5	5.0	5.5	V
Operating temperature	T_{OPR}	-30	-	+85	ºC

7.3 Electrical characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	µA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	µA
Tri-state leakage current	I_{OZ}	-	-10	-	10	µA
Input capacitance	C_{IN}	-	-	3	-	pF
Output capacitance	C_{OUT}	-	3	-	6	pF
Logic input low voltage	V_{IL}	CMOS	-	-	$0.3V_{IO}$	V
Logic input high voltage	V_{IH}	CMOS	$0.7V_{IO}$	-	-	V
Output low voltage	V_{OL}	I_{OL}=4mA	-	-	$0.2V_{IO}$	V
Output high voltage	V_{OH}	I_{OH}=-4mA	$0.8V_{IO}$	-	-	V
Input pull up/down resistance	R_I	V_{IL}= 0V or V_{IH}= V_{IO}	20	-	100	kΩ
Digital operating current	I_{DDIO}	V_{DDIO} =3.3V, Input data format: CCIR656	-	-	4.2	mA
Analog operating current	I_{DD}	V_{DD} =5V, Input data format: CCIR656	-	-	11.3	mA
Analog operating current	I_{DDA}	V_{DDA} =5V, Input data format: CCIR656	-	-	13.9	mA

8. AC Characteristics

8.1 Input signal characteristics

8.1.1 ITU-R BT.601 8-bit or ITU-R BT.656 8-bit

Parameter	Symbol		Spec.			Unit
			Min.	Typ.	Max.	
CLK period	t_C		35	37	39	ns
CLK Duty	t_{CW}		40	50	60	%
HREF period	t_H	NTSC	60.1	63.5	66.9	µs
			-	1716	-	t_C
		PAL	60.5	64	67.4	µs
			-	1728	-	t_C
HREF pulse width	t_{HD}	NTSC	50.4	53.3	56.1	µs
			-	1440	-	t_C
		PAL	50.4	53.3	56.1	µs
			-	1440	-	t_C
V123 period	t_V	NTSC	15.8	16.6	17.5	ms
			-	262.5	-	t_H
		PAL	18.9	20	21	ms
			-	312.5	-	t_H
V123 pulse width	t_{VP}		1.3	1.5	1.7	t_H
Data setup time	t_{DS}		10	-	-	ns
Data hold time	t_{DH}		10	-	-	ns

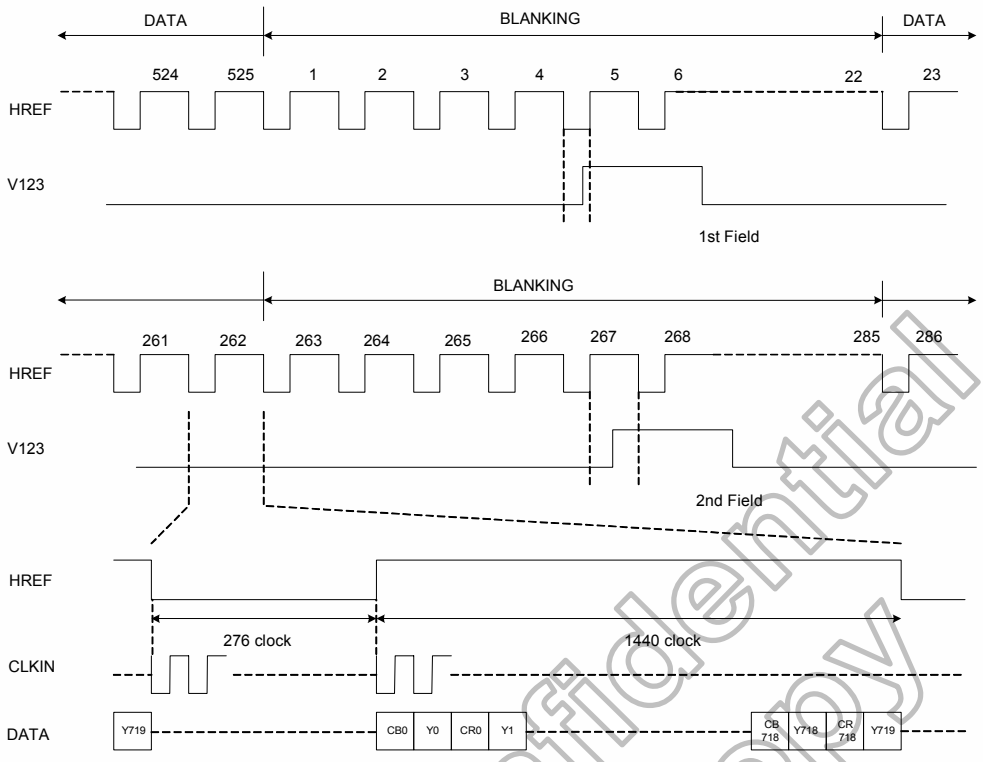


Figure 8. 1 ITU-R BT. 601 NTSC input timing

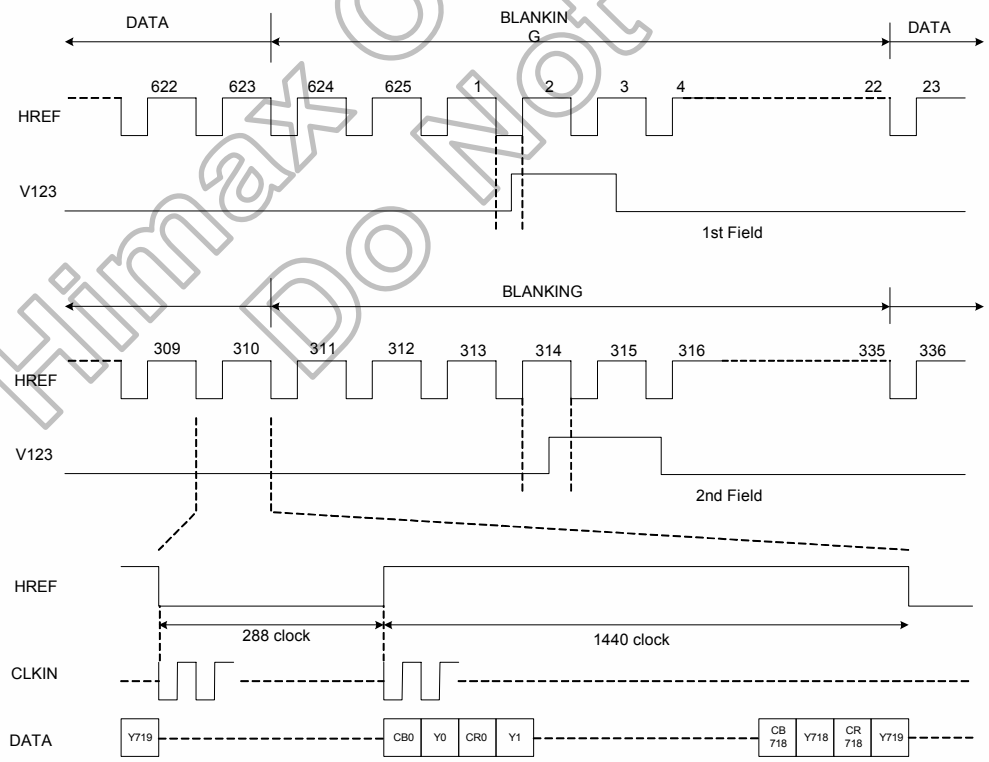


Figure 8. 2 ITU-R BT. 601 PAL input timing

8.1.2 8-bit digital RGB input interface

Parameter	Symbol		Resolution				Unit
			1440	1200	960	480	
CLK period	t_C	Min.	33.3	40.3	49.9	99.8	ns
		Typ.	35.3	42.3	52.9	105.8	
		Max.	37.3	44.3	55.9	111.8	
CLK duty	t_{CW}		50±10				%
HS period	t_H		1800	1500	1200	600	t_C
Display period	t_{HD}, t_{EP}		1440	1200	960	480	t_C
HS pulse width min	t_{HP}	Min	5				t_C
HS-DE time	t_{HE}	Min	162	135	108	54	t_C
		Max	360	300	240	120	t_C
HS to internal DE when DE fixed low	t_{HE}		306	255	204	102	Min
VS period	t_V	NTSC	262				t_H
		PAL	312				t_H
VS pulse width	t_{VP}	Min	3				t_H
Vertical display position	t_{VS}	NTSC	18				t_H
		PAL	26				t_H
Vertical data period	t_{VD}	NTSC	240				t_H
		PAL	280				t_H
Setup time	t_{VH},	Min	1				t_C
Setup time (Data, HS, DE)	t_{DS}, tc_S t_{HC}	Min	10				ns
Hold time	t_{DH}	Min	10				ns

8.1.3 18-bit Digital RGB input interface

Parameter	Symbol		Resolution				Unit
			1440	1200	960	480	
CLK Period	t_C	Min.	99.8	121	149.8	299.5	ns
		Typ.	105.8	127	158.8	317.5	
		Max.	111.8	133	167.8	335.5	
CLK Duty	t_{CW}		50±10				%
HS Period	t_H		600	500	400	200	t_C
HS display period	t_{HD}, t_{EP}		480	400	320	160	t_C
HS pulse width	t_{HP}	Min	5				t_C
HS-DE time	t_{HE}	Min	54	45	36	18	t_C
		Max	120	100	80	40	t_C
HS to internal DE when DE fixed low	t_{HE}		102	85	68	34	t_C
VS period	t_V	NTSC	262				t_H
		PAL	312				t_H
VS pulse width	t_{VP}	Min	3				t_H
Vertical display position	t_{VS}	NTSC	18				t_H
		PAL	26				t_H
Vertical data period	t_{VD}	NTSC	240				t_H
		PAL	280				t_H
Setup time	t_{VH},	Min	1				t_C
Setup time (Data, HS, DE)	t_{DS}, tc_S t_{HC}	Min	10				ns
Hold time	t_{DH}	Min	10				ns

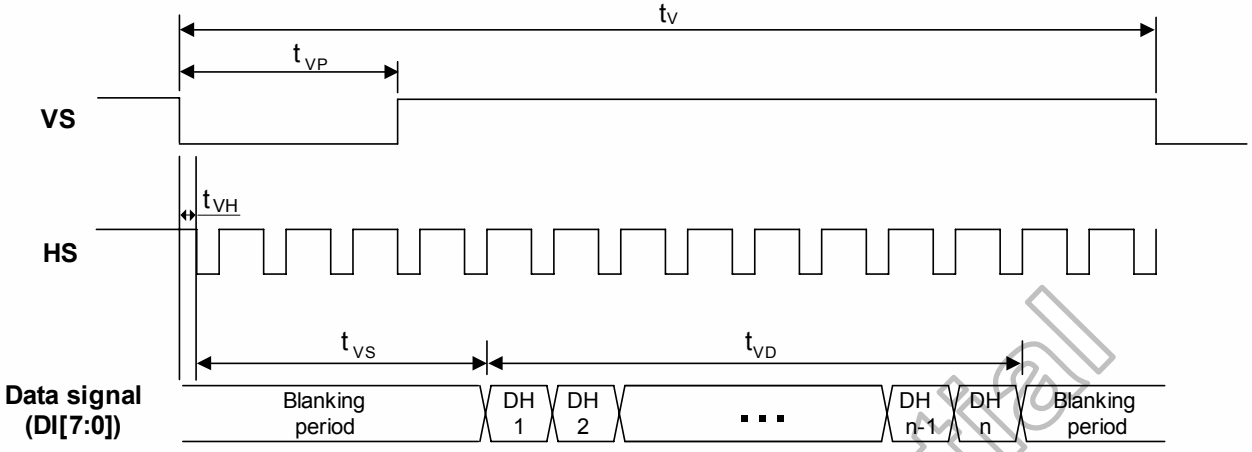


Figure 8. 3 Input vertical timing

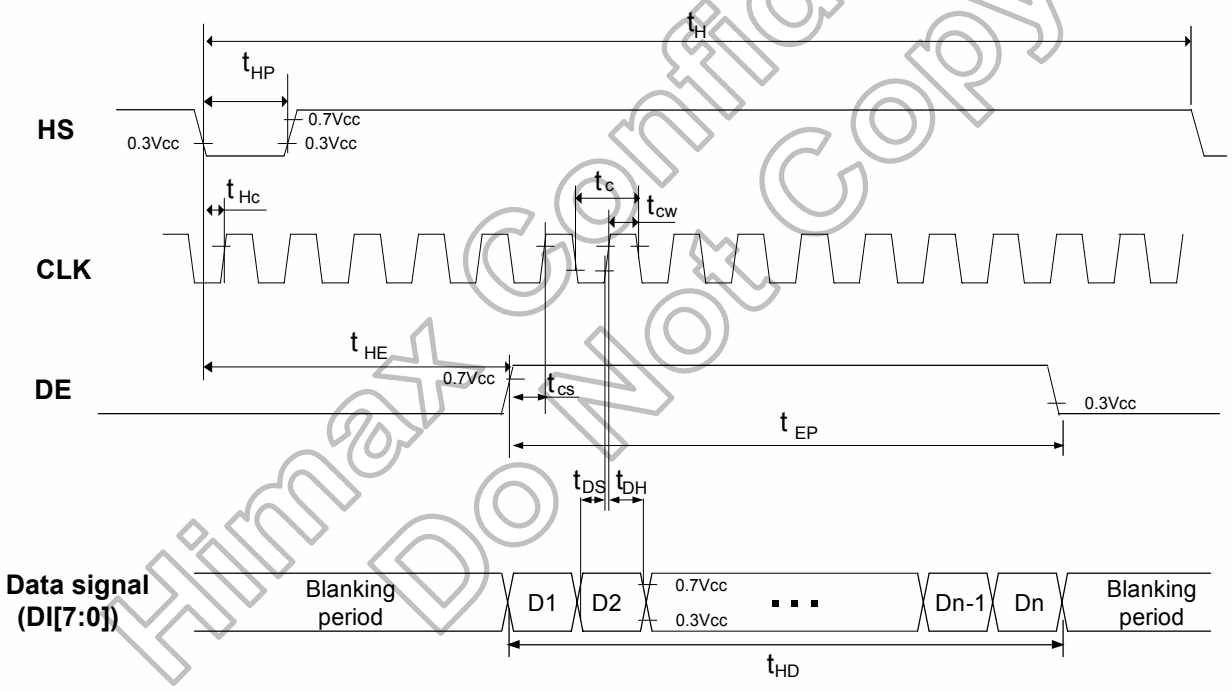


Figure 8. 4 Input horizontal timing

8.2 Output signal characteristics

8.2.1 ITU-R BT.601 or ITU-R BT.656 in full mode

Parameter	Symbol		Min.	Typ.	Max.	Unit
Display period	t_{ACT}		-	1360	-	t_C
Clock pulse duty	t_{CWH}		33	50	67	%
STH setup time	t_{SUH}		-	1	-	t_C
STH pulse width	t_{STH}		-	2	-	t_C
OEH pulse width	t_{OEH}		-	36	-	t_C
Sample & hold disable time	t_{DIS1}		-	108	-	t_C
CKV pulse width	t_{CKV}		-	108	-	t_C
OEV pulse width	t_{OEV}		-	144	-	t_C
IHS-OEH time (1)	t_1		-	126	-	t_C
IHS -CKV time	t_2		-	72	-	t_C
IHS -OEV time	t_3		-	18	-	t_C
STV setup time	t_{SUV}		-	54	-	t_C
STV pulse width	t_{STV}		-	1	-	t_H
V123-STV time	t_{VS1}	NTSC	-	19	-	t_H
		PAL	-	27	-	t_H
OEH-STV time	t_{OES}		-	2	-	t_H

Note: (1) IHS is internally generated horizontal sync signal for reference.

8-bit digital RGB interface

Parameter	Symbol		Resolution				Unit
			1440	1200	960	480	
Clock period(1)	t_{CPH}		3				t_C
Clock pulse duty	t_{CWH}		50				%
3-ϕ clock phase difference	t_{C12}, t_{C23}		10				ns
STH setup time	t_{SUH}		$t_{CPH}/2$				ns
STH pulse width	t_{STH}		1				t_{CPH}
OEH pulse width	t_{OEH}		12	10	8	4	t_{CPH}
Sample & hold disable time	t_{DIS1}		59	41	33	17	t_{CPH}
CKV pulse width	t_{CKV}		36	30	24	12	t_{CPH}
OEV pulse width	t_{OEV}		48	40	32	16	t_{CPH}
HS-OEH time	t_1		42	35	28	14	t_{CPH}
HS -CKV time	t_2		24	20	16	8	t_{CPH}
HS -OEV time	t_3		6	5	4	2	t_{CPH}
STV setup time	t_{SUV}		18	15	12	6	t_{CPH}
STV pulse width	t_{STV}		1				t_H
VS-STV time	t_{VS1}	NTSC	16				t_H
		PAL	24				t_H
OEH-STV time	t_{OES}		2				t_H

8.2.2 18-bit digital RGB interface

Parameter	Symbol	Resolution				Unit
		1440	1200	960	480	
Clock period	t_{CPH}	1				t_C
Clock pulse duty	t_{CWH}	50				%
3-ϕ clock phase difference	t_{C12}, t_{C23}	10				ns
STH setup time	t_{SUH}	t_{CPH}/2				ns
STH pulse width	t_{STH}	1				t_{CPH}
OEH pulse width	t_{OEH}	12	10	8	4	t_{CPH}
Sample & hold disable time	t_{DIS1}	58.5	40.5	32.5	16.5	t_{CPH}
CKV pulse width	t_{CKV}	36	30	24	12	t_{CPH}
OEV pulse width	t_{OEV}	48	40	32	16	t_{CPH}
HS-OEH time	t_1	42	35	28	14	t_{CPH}
HS -CKV time	t_2	24	20	16	8	t_{CPH}
HS -OEV time	t_3	6	5	4	2	t_{CPH}
STV setup time	t_{SUV}	18	15	12	6	t_{CPH}
STV pulse width	t_{STV}	1				t_H
VS-STV time	t_{VS1} NTSC	16				t_H
	t_{VS1} PAL	24				t_H
OEH-STV time	t_{OES}	2				t_H

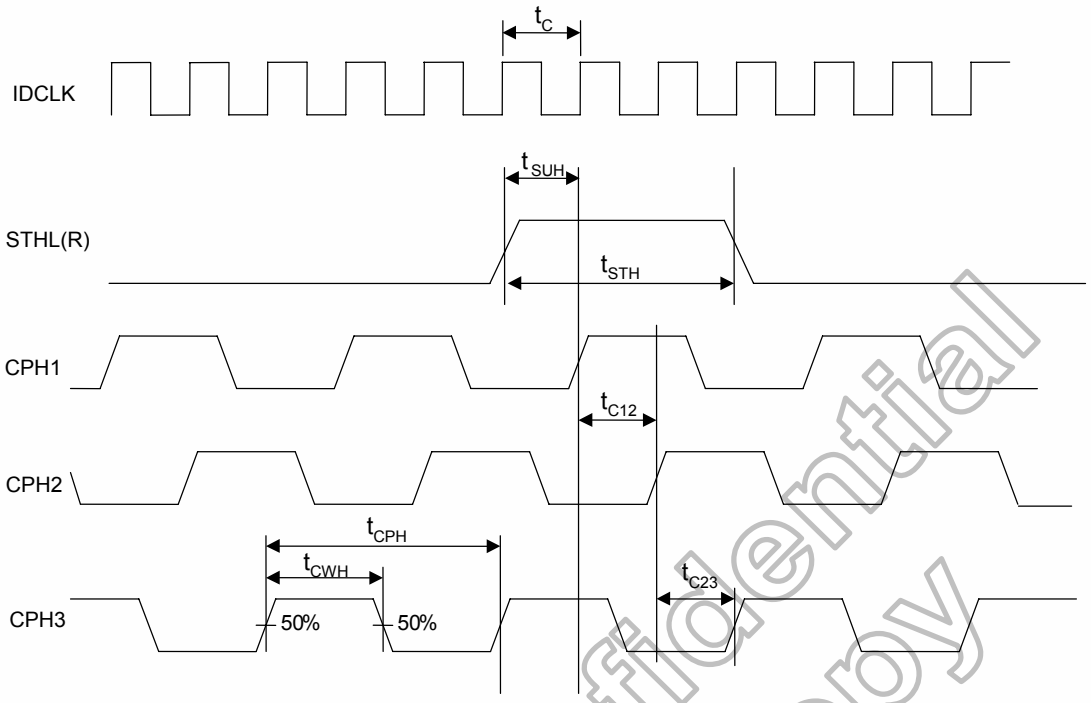


Figure 8. 5 IDCLK, STHL(R) and CPH timing waveform

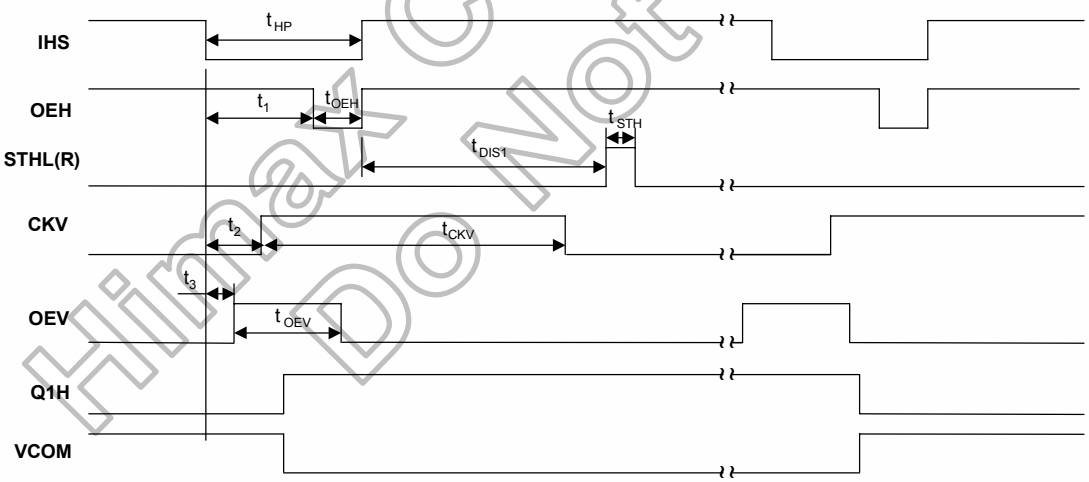


Figure 8. 6 IHS and horizontal control timing waveform

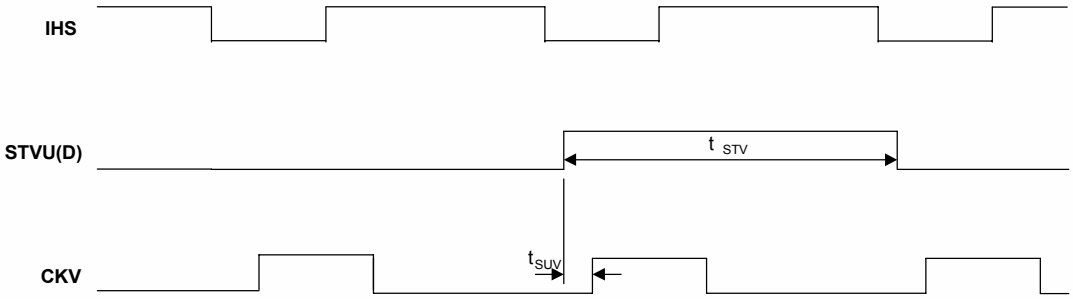


Figure 8. 7 IHS and vertical shift clock timing waveform

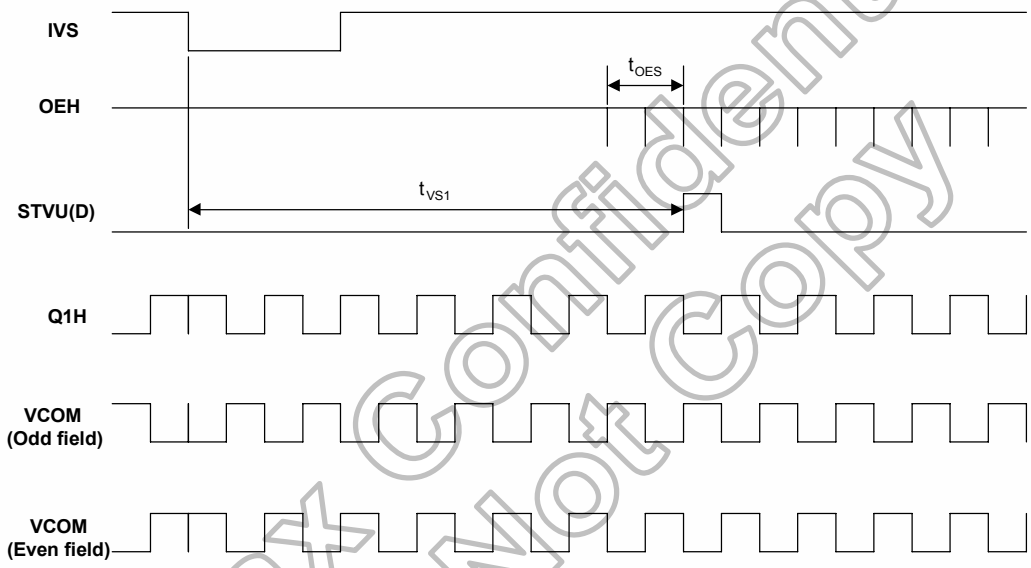


Figure 8. 8 IHS and vertical control timing waveform (for the case of UDC="H")

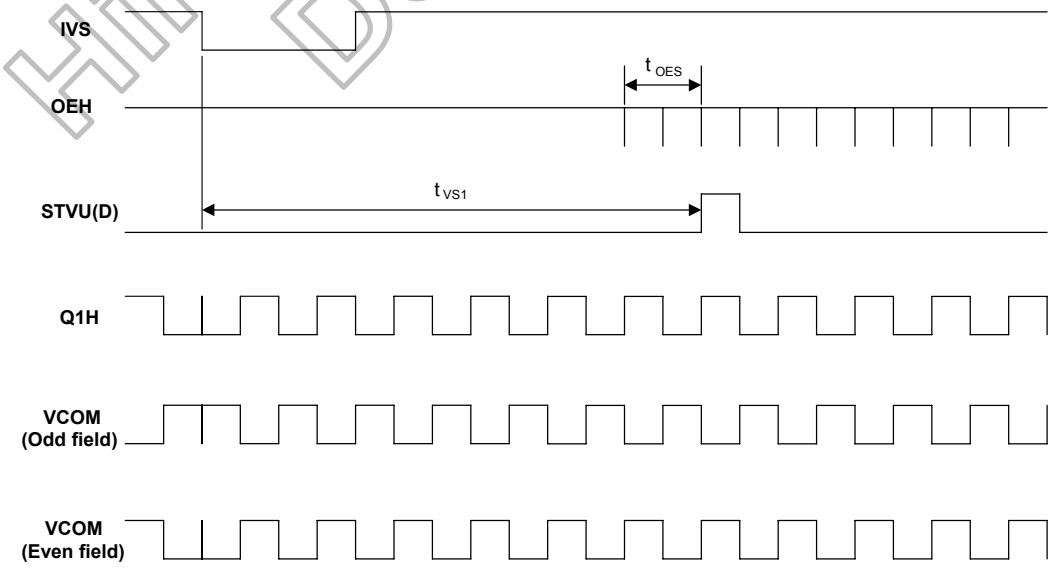


Figure 8. 9 IHS and vertical control timing waveform (for the case of UDC="L")

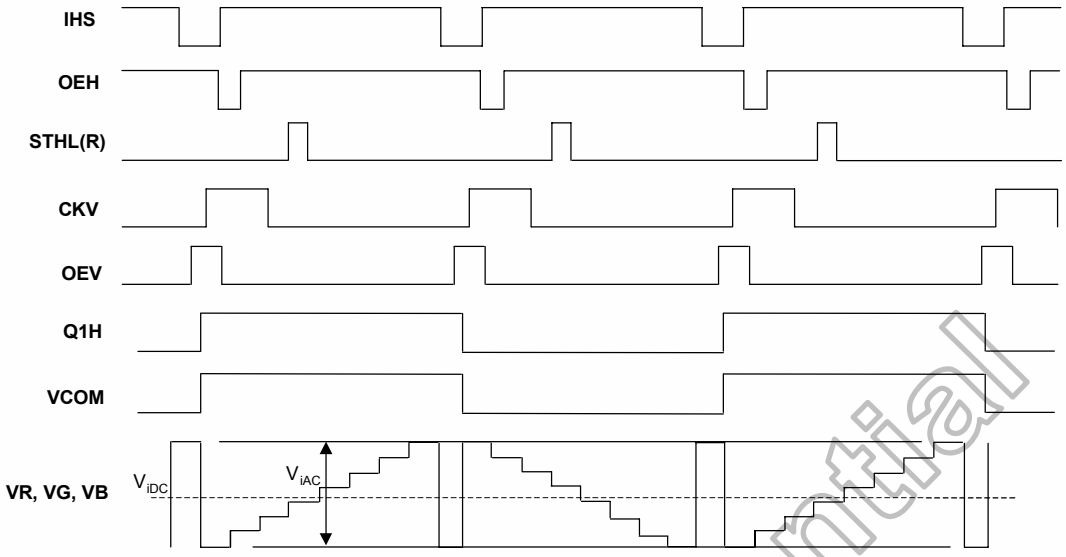


Figure 8. 10 Analog video signal amplitude (VR, VG, VB)

8.3 SPI Interface

8.3.1 Slave mode, written through SPI interface

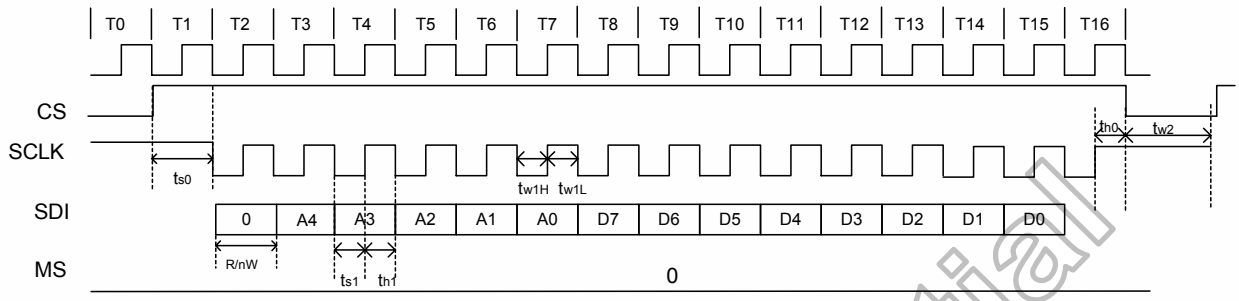


Figure 8. 11 Slave mode, written through SPI interface

8.3.2 Slave mode, read through SPI interface

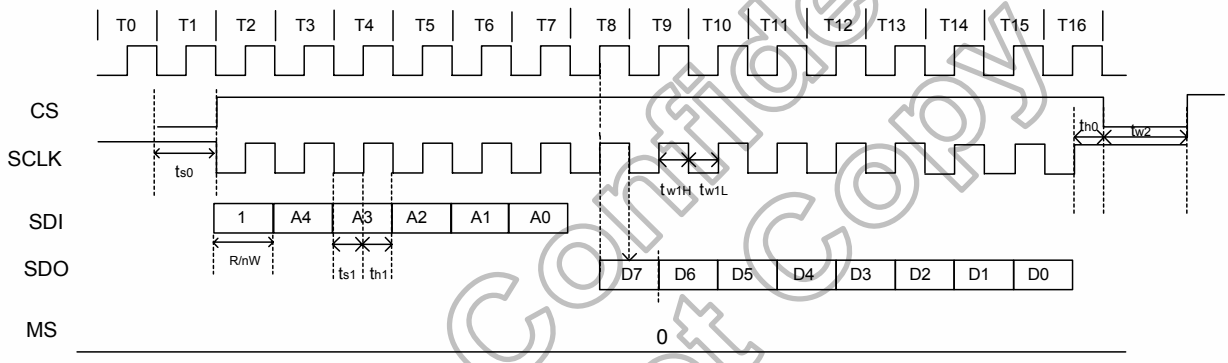


Figure 8. 12 Slave mode, read through SPI interface

Item	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Data Setup Time	ts0	CS to SCLK	300	-	-	ns
	ts1	DATA to SCLK	150	-	-	ns
Data Hold Time	th0	CS to SCLK	150	-	-	ns
	th1	DATA to SCLK	150	-	-	ns
Pulse Width	tw1L	SCLK pulse width	160	-	-	ns
	tw1H	SCLK pulse width	160	-	-	ns
	tw2	CS pulse width	1.0	-	-	µs
Clock duty	-	-	40	-	60	%

Table 8. 1 SPI timing

8.3.3 Master mode, access data from EERPOM when power on

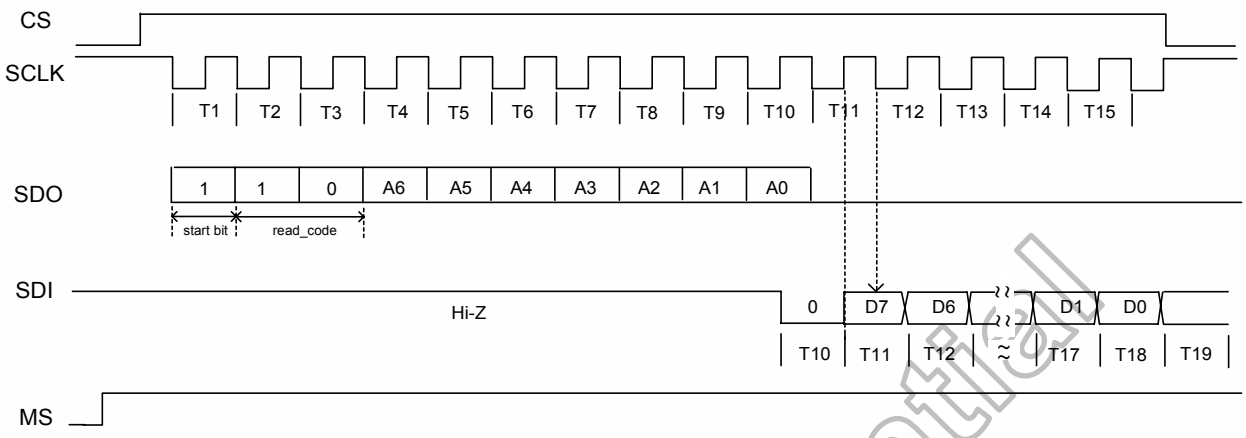


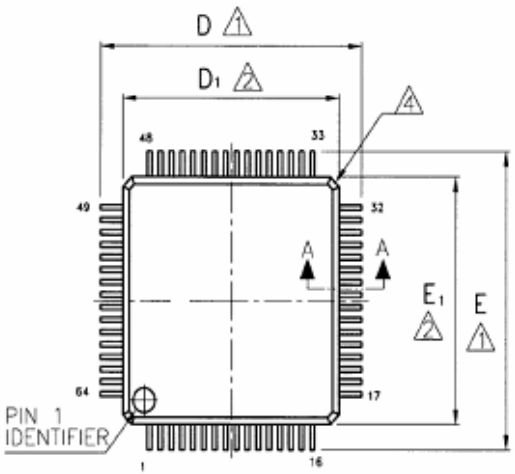
Figure 8. 13 Master mode, access data from EERPOM when power on

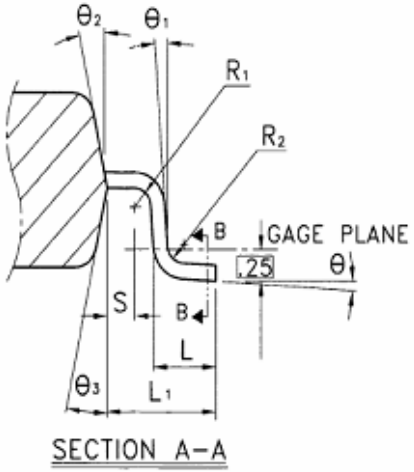
Note: (1) Please refer to 93C46 datasheet

9. Analog Video Signal Characteristics

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Video signal amplitude (VR, VG, VB)	V_{IAC}	-	4	-	V
	V_{IDC}	-	2.5	-	V

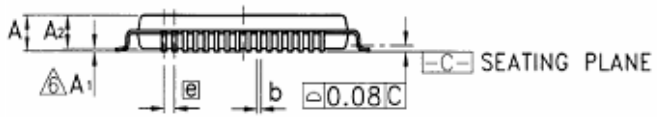
Table 9. 1 Analog video signal characteristics

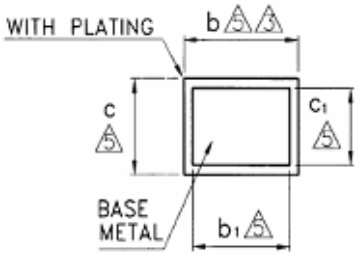




SECTION A–A

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		





SECTION B–B

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BCD.

TITLE: 64LD LQFP (10x10x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm
L/F MATERIAL: C7025 1/2H

10. Ordering Information

Part NO.	Package
HX8817ALAG	64 pin LQFP

11. Revision History

Version	Date	Description of Changes
01	2004/03/16	New setup
02	2005/08/08	1. Add 3-ϕ clock phase difference 2. Modify 8.2.2 to 18-bit Digital RGB Interface 3. Modify PWM feedback value and add PWM formula
03	2006/02/27	1. Add clock tolerance in section 8.1.1 ITU-R BT601 8 bit or ITU-R BT656 bit, 8.1.2 8-bit Digital RGB Input Interface, and 8.1.3 18-bit Digital RGB Input Interface. 2. Add section 6.6 Serial digital RGB mode input data sequence and color filter type 3. Modify Figure 6. 2 PWM1 booster 4. Add tVH in Figure 8.3 Input vertical timing 5. Add Register settings of R3h(IB5,IB6, and IB7) and R4h(IB5 and IB6) 6. Add Figure 8. 5 Input timing of 18 bits RGB DE only mode 7. Add Figure 8. 6 Input timing of 8 bits RGB DE only mode
04	2007/10/23	1. Page 2 Change the Figure 3. 1 Block Diagram output pin VCOM to POL 2. Page 10 and 11 Remove Register settings of R3h(IB5,IB6, and IB7) and R4h(IB5 and IB6) 3. Page 27 Remove Figure of Input timing of 8/18 bits RGB DE only mode 4. ALL pages Remove “Subject to change without notice” from datasheet