HWD2180 Audio PowerAmplifier

Dual 250 mW Audio Power Amplifier with Shutdown Mode

General Description

The HWD2180 is a dual audio power amplifier capable of delivering typically 250mW per channel of continuous average power to an 8Ω load with 0.1% THD+N using a 5V power supply.

audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging.

Since the HWD2180 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The HWD2180 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable HWD2180 can be configured by external gain-setting resistors.

Key Specifications

- THD+N at 1kHz at 200mW continuous average output power into 8Ω: 0.1% (max)
- THD+N at 1kHz at 85mW continuous average output power into 32Ω: 0.1% (typ)
- Output power at 10% THD+N at 1kHz into 8Ω: 325mW (typ)
- Shutdown current: 0.7µA (typ)
- 2.7V to 5.5V supply voltage range

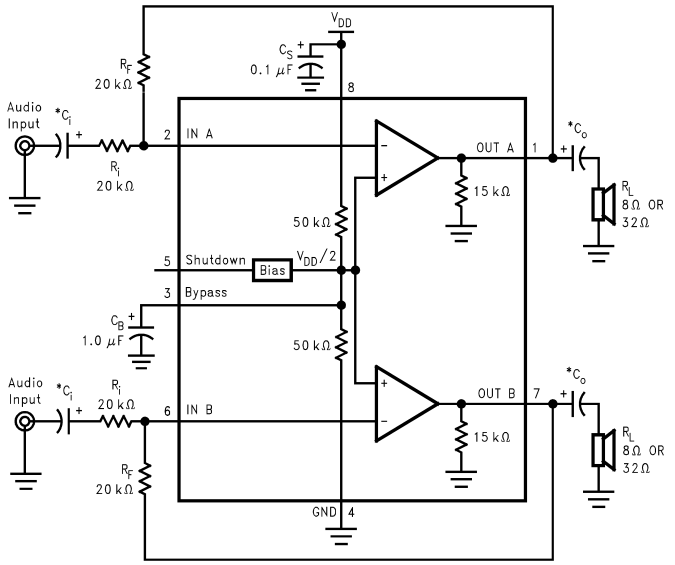
Features

- No bootstrap capacitors or snubber circuits are necessary
- Small Outline (SO) and DIP packaging
- Unity-gain stable
- External gain configuration capability

Applications

- Headphone Amplifier
- Personal Computers
- CD-ROM Players

Typical Application

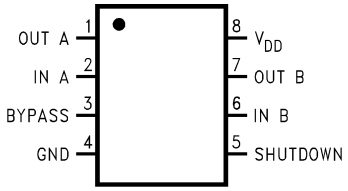


*Refer to the **Application Information** section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline and DIP Packages



Top View
Order Number HWD2180M or HWD2180N

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the CSMSC Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	3500V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150˚C
Soldering Information	
Small Outline Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance

θ_{JC} (DIP)	37˚C/W
θ_{JA} (DIP)	107˚C/W
θ_{JC} (SO)	35˚C/W
θ_{JA} (SO)	170˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	−40˚C≤T_A≤+85˚C
Supply Voltage	2.7V≤V_{DD}≤5.5V

Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5V unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	HWD2180		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V, I_O=0A	3.6	6.0	mA (max)
I_{SD}	Shutdown Current	V_{PIN5}=V_{DD}	0.7	5	µA (max)
V_{OS}	Output Offset Voltage	V_{IN}=0V	5	50	mV (max)
P_O	Output Power	THD=0.1% (max); f=1 kHz;			
		R_L=8Ω	250	200	mW (min)
		R_L=32Ω	85		mW
		THD+N=10%; f=1 kHz			
		R_L=8Ω	325		mW
		R_L=32Ω	110		mW
THD+N	Total Harmonic Distortion+Noise	R_L=8Ω, P_O=200 mW;	0.03		%
		R_L=32Ω, P_O=75 mW;	0.02		%
		f=1 kHz			
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, V_{RIPPLE}=200 mVrms, f = 100 Hz	50		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the HWD2180, T_{JMAX} = 150˚C, and the typical junction-to-ambient thermal resistance is 170˚C/W for package M08A and 107˚C/W for package N08E.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Automatic Shutdown Circuit

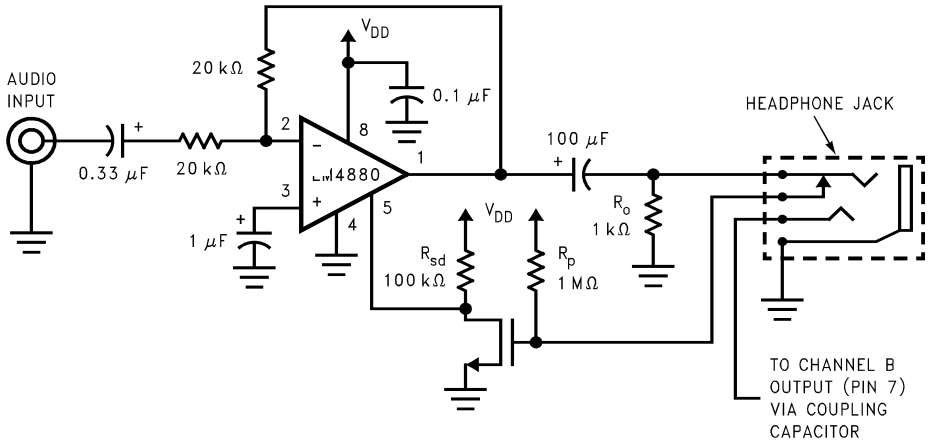


FIGURE 2. Automatic Shutdown Circuit

Automatic Switching Circuit

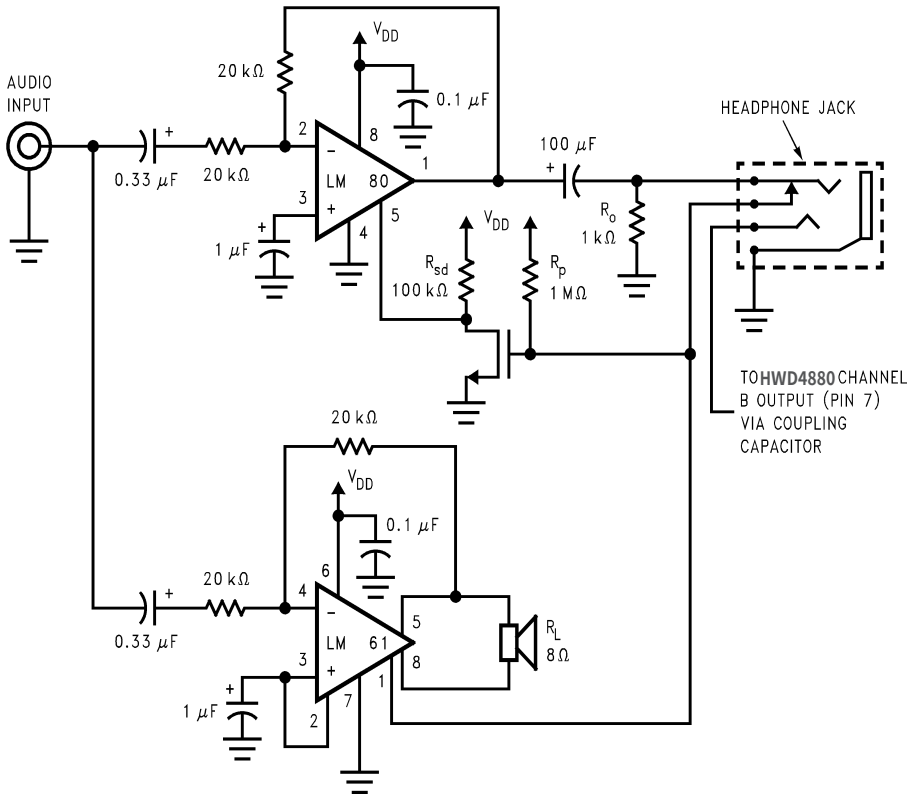


FIGURE 3. Automatic Switching Circuit

External Components Description (*Figure 1*)

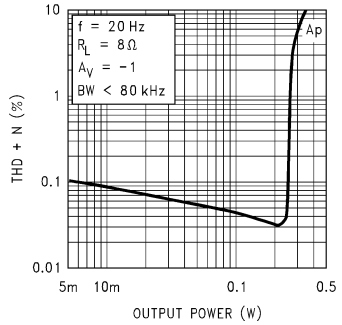
Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_F. This resistor also forms a high pass filter with C_i at $f_c = 1/(2pR_iC_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high pass filter with R_i at $f_c = 1/(2pR_iC_i)$. Refer to the section, Proper Selection of External Components, for an explanation of how to determine the value of C_i.
3.	R_F	Feedback resistance which sets closed-loop gain in conjunction with R_i.

External Components Description (*Figure 1*) (Continued)

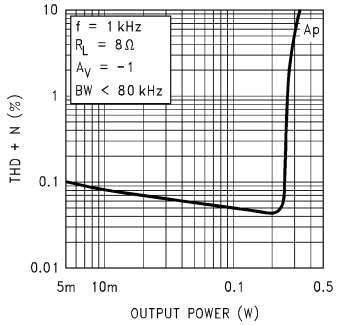
Components		Functional Description
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Application Information** section for proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of External Components,** for information concerning proper placement and selection of C_B.
6.	C_o	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with R_L at $f_o = 1/(2\pi R_L C_o)$.

Typical Performance Characteristics

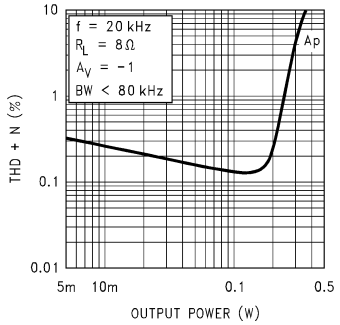
THD + N vs Output Power



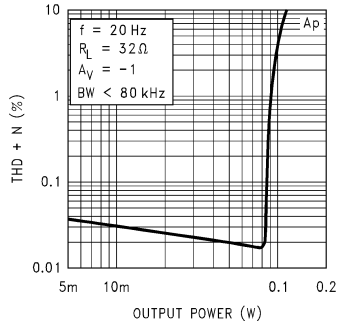
THD + N vs Output Power



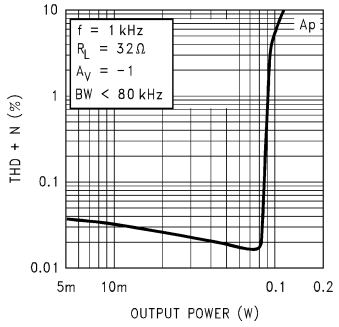
THD + N vs Output Power



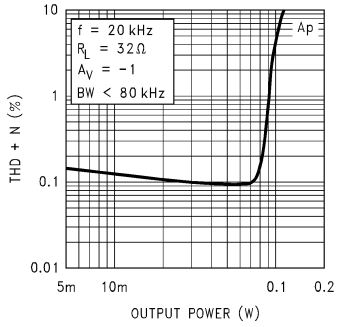
THD + N vs Output Power



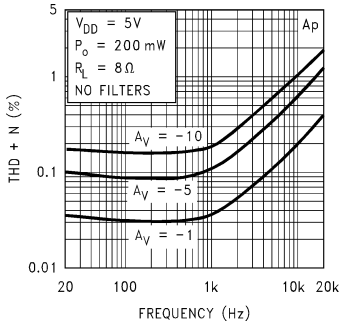
THD + N vs Output Power



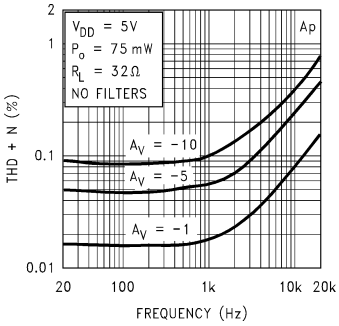
THD + N vs Output Power



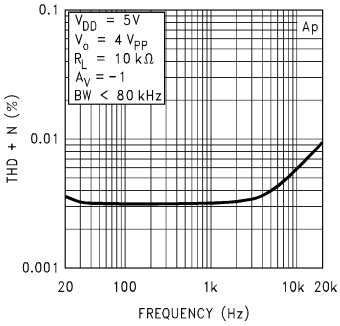
THD + N vs Frequency



THD + N vs Frequency

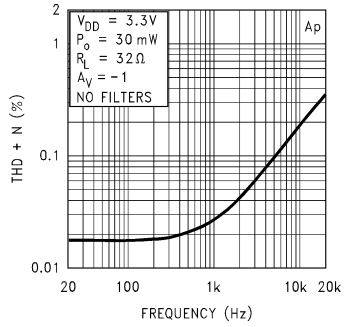


THD + N vs Frequency

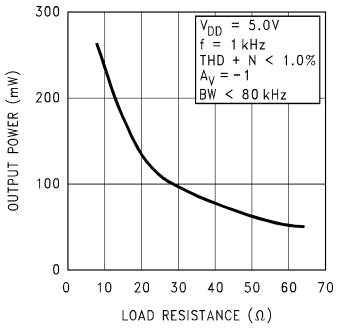


Typical Performance Characteristics (Continued)

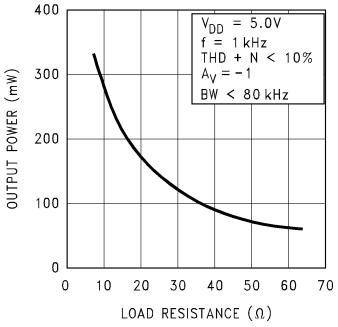
THD + N vs Frequency



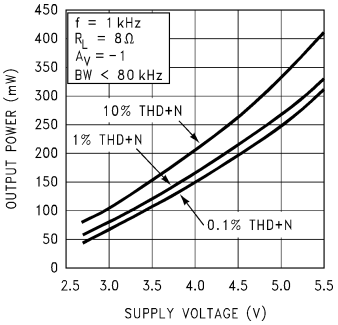
Output Power vs Load Resistance



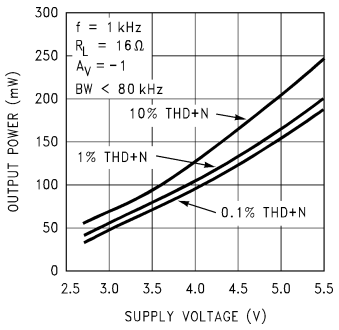
Output Power vs Load Resistance



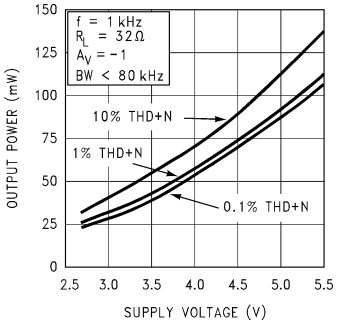
Output Power vs Supply Voltage



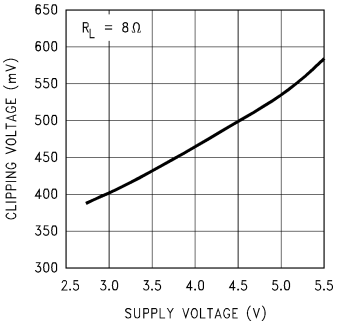
Output Power vs Supply Voltage



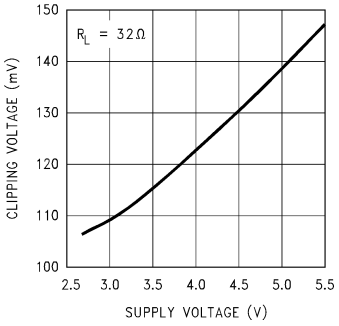
Output Power vs Supply Voltage



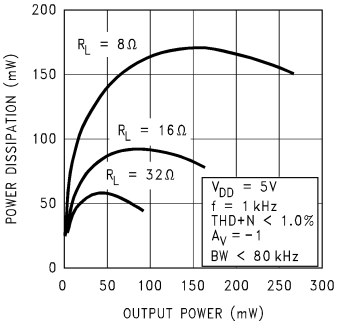
Clipping Voltage vs Supply Voltage



Clipping Voltage vs Supply Voltage

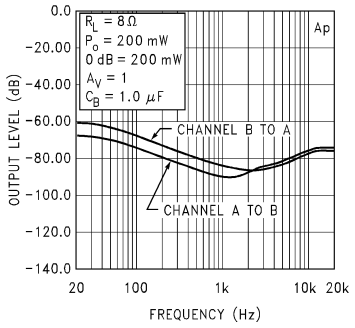


Power Dissipation vs Output Power

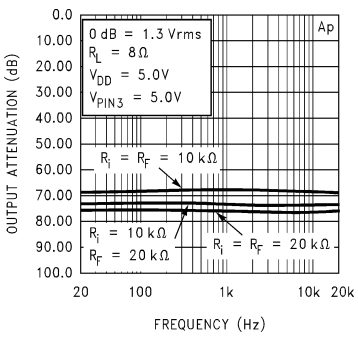


Typical Performance Characteristics (Continued)

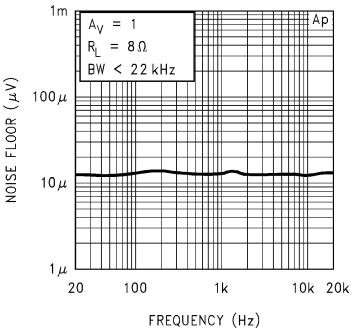
Channel Separation



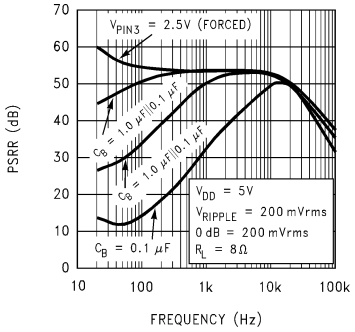
Output Attenuation in Shutdown Mode



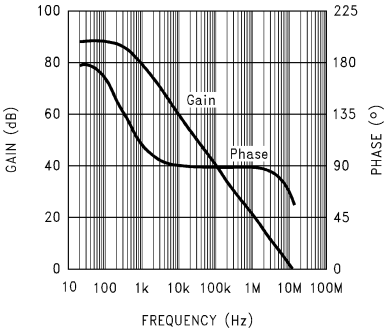
Noise Floor



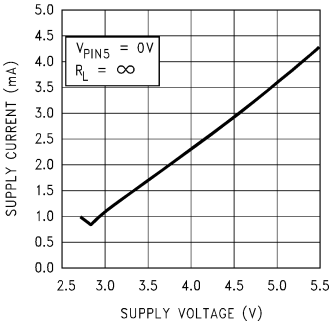
Power Supply Rejection Ratio



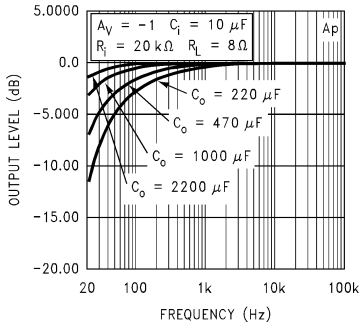
Open Loop Frequency Response



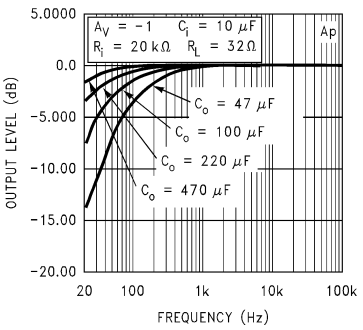
Supply Current vs Supply Voltage



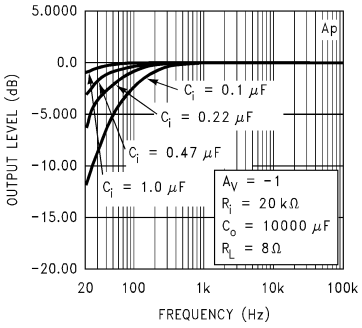
Frequency Response vs Output Capacitor Size



Frequency Response vs Output Capacitor Size

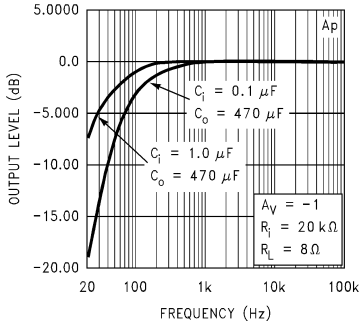


Frequency Response vs Input Capacitor Size

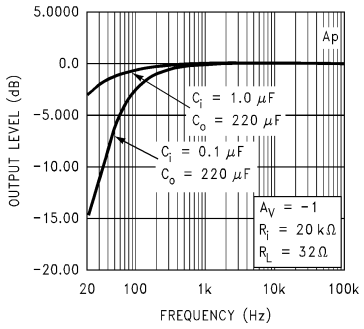


Typical Performance Characteristics (Continued)

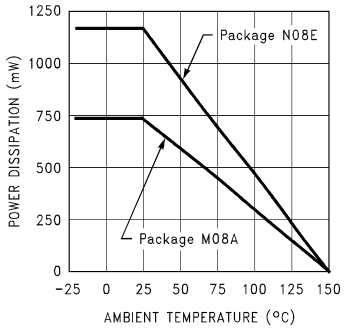
Typical Application Frequency Response



Typical Application Frequency Response



Power Derating Curve



Application Information

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the HWD2180 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half supply. It is best to switch between ground and the supply to provide maximum device performance. By switching the shutdown pin to V_{DD}, the HWD2180 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than V_{DD}, the idle current may be greater than the typical value of 0.7 µA. In either case, the shutdown pin should be tied to a definite voltage because leaving the pin floating may result in an unwanted shutdown condition.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and enables the amplifier. If the switch is open, then the external pull-up resistor will disable the HWD2180. This scheme guarantees that the shutdown pin will not float which will prevent unwanted state changes.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. *Equation (1)* states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

Since the HWD2180 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from *Equation (1)*. Even with the large internal power dissipation, the HWD2180 does not require heat sinking over a large range of ambient temperatures. From *Equation (1)*, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 158 mW per amplifier. Thus the maximum package dissipation point is 317 mW. The maximum power dissipation point obtained must not be greater than the power dissipation that results from *Equation (2)*:

$$P_{DMAX} = (T_{JMAX}-T_A)/\theta_{JA} \quad (2)$$

For the HWD2180 surface mount package, θ_{JA} = 170˚ C/W and T_{JMAX} = 150˚C. Depending on the ambient temperature, T_A, of the system surroundings, *Equation (2)* can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of *Equation (1)* is greater than that of *Equation (2)*, then either the supply voltage must be decreased, the load impedance increased, or the ambient temperature reduced. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 96˚C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the **Typical Performance Characteristics** curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. As displayed in the **Typical Performance Characteristics** section, the effect of a larger half supply bypass capacitor is improved low frequency PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 10 µF and a 0.1 µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the HWD2180. The selection of bypass capacitors, especially C_B, is thus dependant upon desired low frequency PSRR, click and pop performance as explained in the section, **Proper Selection of External Components** section, system cost, and size constraints.

AUTOMATIC SHUTDOWN CIRCUIT

As shown in *Figure 2*, the HWD2180 can be set up to automatically shutdown when a load is not connected. This circuit is based upon a single control pin common in many headphone jacks. This control pin forms a normally closed switch with one of the output pins. The output of this circuit (the voltage on pin 5 of the HWD2180) has two states based on the state of the switch. When the switch is open, signifying that headphones are inserted, the HWD2180 should be enabled. When the switch is closed, the HWD2180 should be off to minimize power consumption.

Application Information (Continued)

The operation of this circuit is rather simple. With the switch closed, R_p and R_o form a resistor divider which produces a gate voltage of less than 5 mV. This gate voltage keeps the NMOS inverter off and R_{sd} pulls the shutdown pin of the HWD2180 to the supply voltage. This places the HWD2180 in shutdown mode which reduces the supply current to 0.7 µA typically. When the switch is open, the opposite condition is produced. Resistor R_p pulls the gate of the NMOS high which turns on the inverter and produces a logic low signal on the shutdown pin of the HWD2180. This state enables the HWD2180 and places the amplifier in its normal mode of operation.

This type of circuit is clearly valuable in portable products where battery life is critical, but is also benefical for power conscious designs such as "Green PC's".

AUTOMATIC SWITCHING CIRCUIT

A circuit closely related to the **Automatic Shutdown Circuit** is the **Automatic Switching Circuit** of *Figure 3*. The **Automatic Switching Circuit** utilizes both the input and output of the NMOS inverter to toggle the states of two different audio power amplifiers. The HW2180 is used to drive stereo single ended loads, while the LM2161 drives bridged internal speakers.

In this application, the HWD2180 and LM2161 are never on at the same time. When the switch inside the headphone jack is open, the HWD2180 is enabled and the LM2161 is disabled since the NMOS inverter is on. If a headphone jack is not present, it is assumed that the internal speakers should be on and thus the voltage on the LM2161 shutdown pin is low and the voltage at the HWD2180 pin is high. This results in the HWD2180 being shutdown and the LM2161 being enabled.

Only one channel of this circuit is shown in *Figure 3* to keep the drawing simple but the typical application would a HWD2180 driving a stereo external headphone jack and two LM2161's driving the internal stereo speakers. If only one internal speaker is required, a single LM2161 can be used as a summer to mix the left and right inputs into a single mono channel.

PROPER SELECTION OF EXTERNAL COMPONENTS

Selection of external components when using integrated power amplifiers is critical to optimize device and system performance. While the HWD2180 is tolerant of external component combinations, care must be exercised when choosing component values.

The HWD2180 is unity-gain stable which gives a designer maximum system flexibility. The HWD2180 should be used in low gain configurations to minimize THD + N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design,** for a more complete explanation of proper gain selection.

Besides gain, one of the major design considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. Both the input coupling capacitor, C_i, and the output coupling capacitor, C_o, form first order high pass filters which limit low frequency response. These values should be chosen based on needed frequency response for a few distinct reasons.

Selection of Input and Output Capacitor Size

Large input and output capacitors are both expensive and space hungry for portable designs. Clearly a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the transducers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz–150 Hz. Thus using large input and output capacitors may not increase system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (normally 1/2 V_{DD}.) This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input and output capacitor sizes, careful consideration should be paid to the bypass capacitor size. The bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the HWD2180 turns on. The slower the HWD2180's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 µF or larger is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

Design a Dual 200 mW/8Ω Audio Amplifier

Given:

Power Output: 200 mWrms
Load Impedance: 8Ω
Input Level: 1 Vrms (max)
Input Impedance: 20 kΩ
Bandwidth: 100 Hz–20 kHz ± 0.50 dB

A designer must first determine the needed supply rail to obtain the specified output power. Calculating the required supply rail involves knowing two parameters, V_{opeak} and also the dropout voltage. As shown in the Typical Performance Curves, the dropout voltage is typically 0.5V. V_{opeak} can be determined from *Equation (3)*.

$$V_{opeak} = \sqrt{(2R_L P_o)} \quad (3)$$

For 200 mW of output power into an 8Ω load, the required V_{opeak} is 1.79V. Since this is a single supply application, the minimum supply voltage is twice the sum of V_{opeak} and V_{od}. Since 5V is a standard supply voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the HWD2180 to reproduce peaks in excess of 200 mW without clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section. Remember that the maximum power dissipation value from *Equation (1)* must be multiplied by two since there are two independent amplifiers inside the package.

Once the power dissipation equations have been addressed, the required gain can be determined from *Equation (4)*.

Application Information (Continued)

$$|A_V| \geq \sqrt{(P_o R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

$$A_V = -R_F/R_i \quad (5)$$

From *Equation (4)*, the minimum gain is:: $A_V = -1.26$

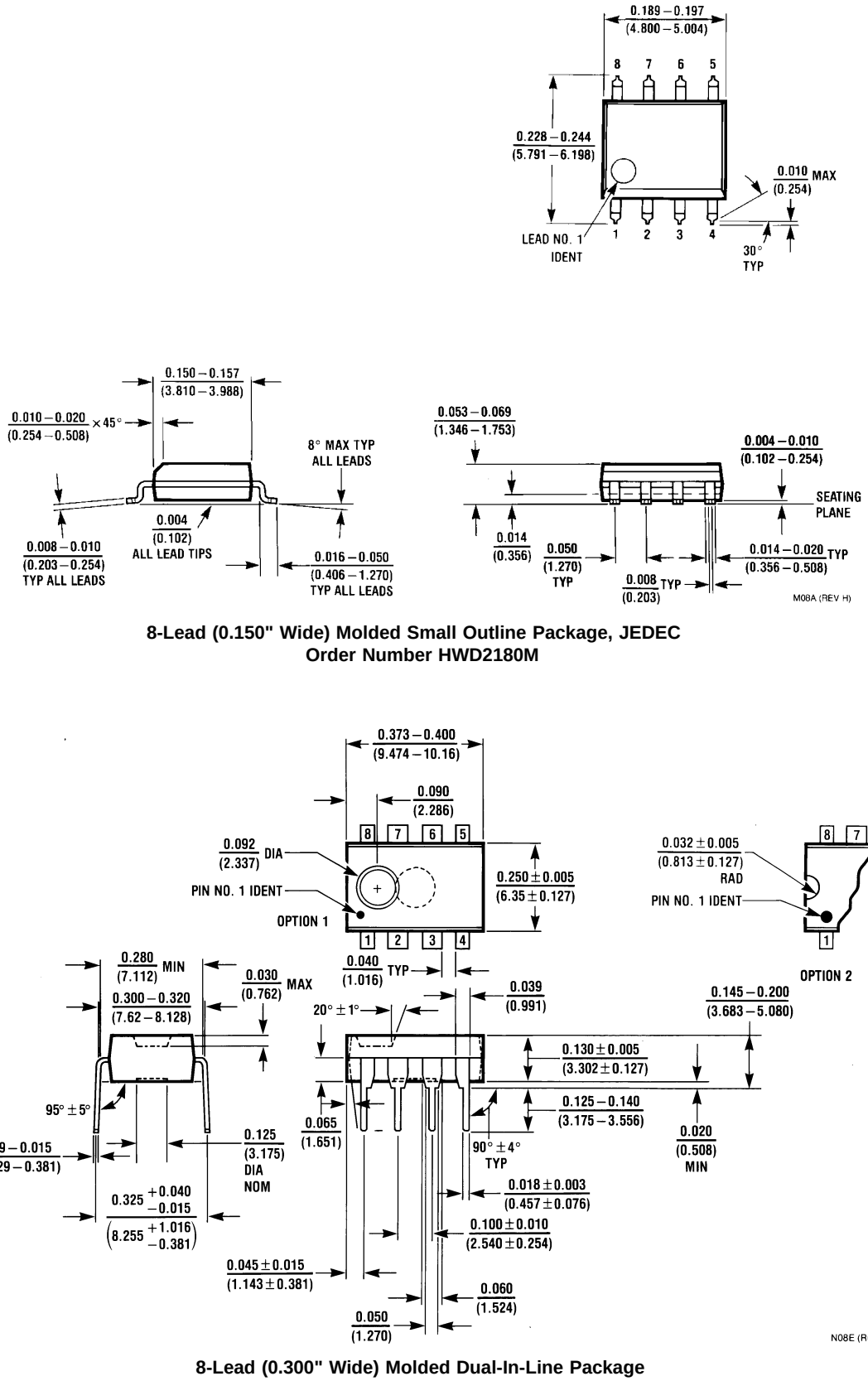
Since the desired input impedance was 20 kΩ, and with a gain of −1.26, a value of 27 kΩ is designated for R_f, assuming 5% tolerance resistors. This combination results in a nominal gain of −1.35. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response assuming a single pole roll-off. As stated in the **External Components** section, both R_i in conjunction with C_i, and C_o with R_L, create first order high pass filters. Thus to obtain the desired frequency low response of 100 Hz within ± 0.5 dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34 dB at five times away from the single order filter −3 dB point. Thus, a frequency of 20 Hz is used in the following equations to ensure that the response if better than 0.5 dB down at 100 Hz.

$C_i \geq 1/(2\pi * 20k\Omega * 20Hz) = 0.397\ \mu F$; use 0.39 µF

$C_o \geq 1/(2\pi * 8\Omega * 20Hz) = 995\ \mu F$; use 1000 µF

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the closed-loop gain, A_V. With a closed-loop gain magnitude of 1.35 and f_H = 100 kHz, the resulting GBWP = 135 kHz which is much smaller than the HWD2180 GBWP of 12.5 MHz. This figure displays that if a designer has a need top design an amplifier with a higher gain, the HWD2180 can still be used without running into bandwidth limitations.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number HWD2180M

8-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Number HWD2180N

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