

12-Channel High Voltage Analog Switch

Features

- HVCMOS[®] Technology for High Performance
- Operating Voltage of Up to 200V
- Output On-resistance Typically 22Ω
- Integrated Bleed Resistors on the Outputs
- 5.0V to 12.0V CMOS Logic Compatibility
- Very Low-quiescent Current Consumption (-10 μA)
- -58 dB Typical OFF-isolation at 5.0 MHz
- Low Parasitic Capacitance
- Excellent Noise Immunity
- Flexible High Voltage Supplies

Applications

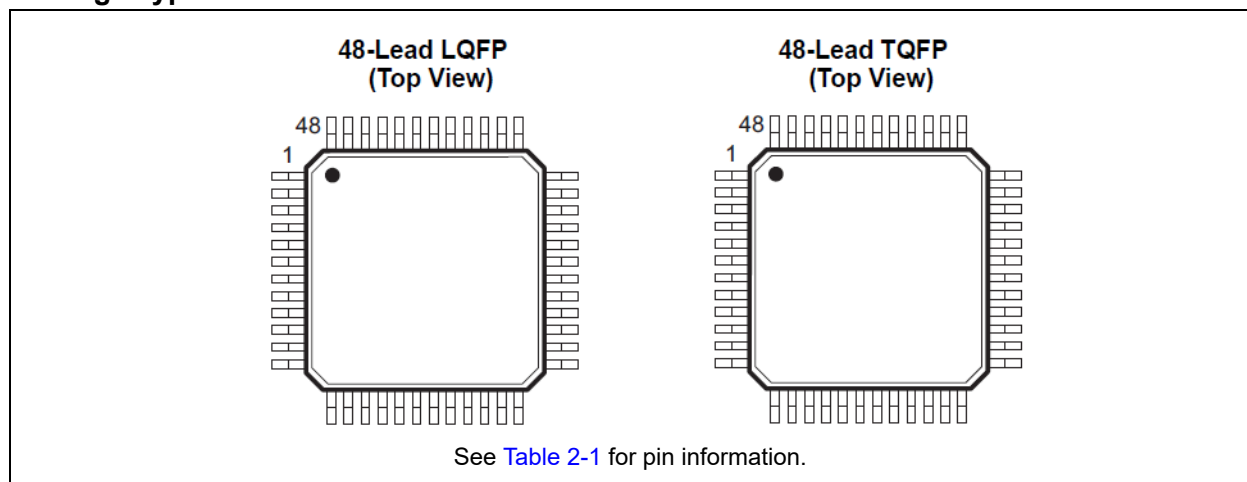
- Medical Ultrasound Imaging
- NDT Metal Flaw Detection
- Piezoelectric Transducer Drivers

Description

The HV209 is a 200V low charge injection 12-channel high voltage analog switch configured as 6 SPDT analog switches intended for medical ultrasound applications.

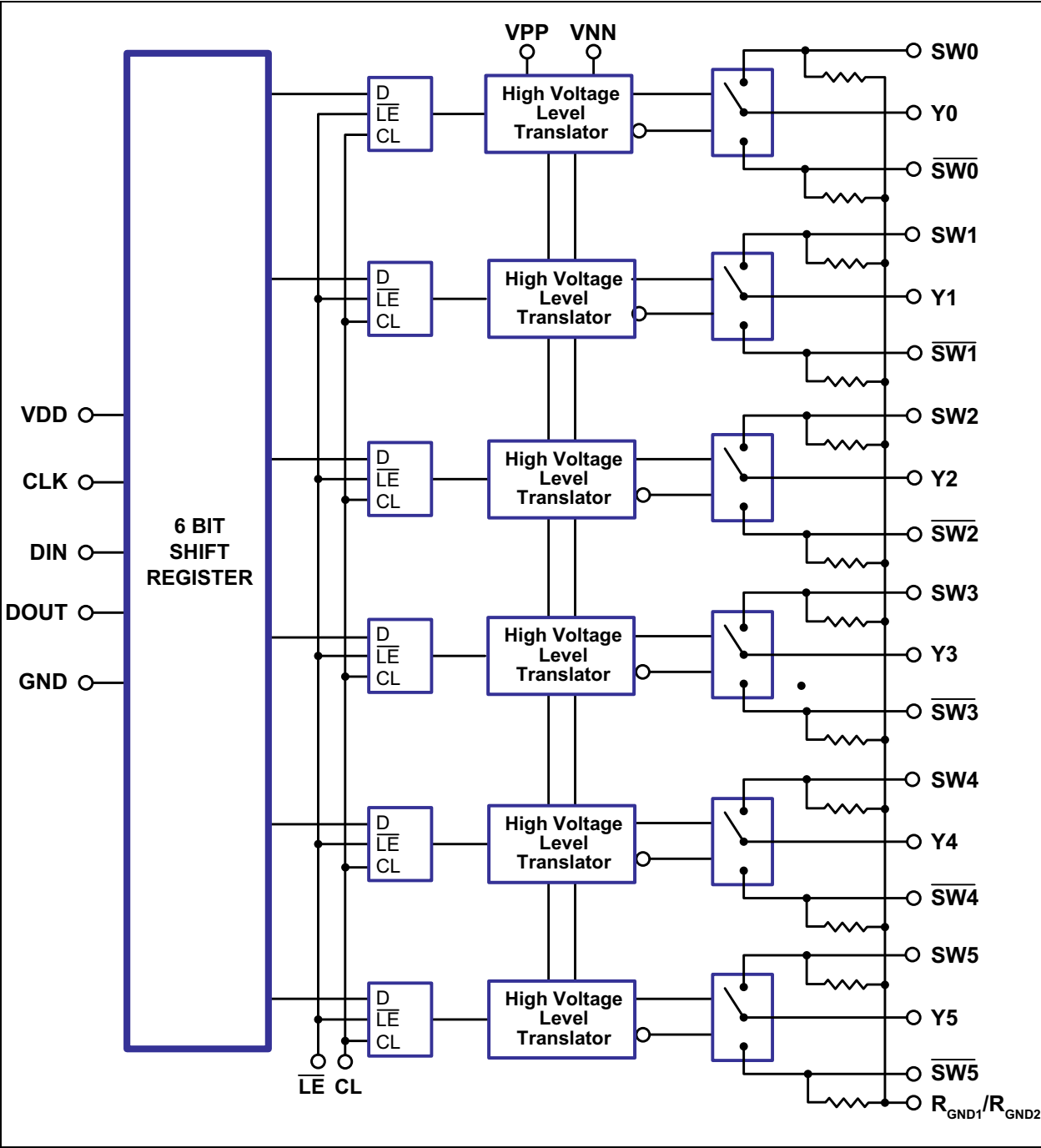
Bleed resistors are integrated on the output switches to eliminate the charge built up on the piezoelectric transducers. The bleed resistors are at a nominal value of 35 kΩ. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals. The outputs are configured as single-pole double-throw analog switches. Data is shifted into a 6-bit shift register using an external clock. The LE latches the shift register data into the individual switch latches. A logic HI connects a switch common YX to SWX. A logic LOW connects YX to SWX. A logic HI in CL resets all switches to SWX simultaneously.

Package Types[†]



[†] **Notice:** The LQFP package is not recommended for new designs. Please use TQFP package as an alternative.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[†]

Logic Supply, V_{DD}	-0.5V to +15V
Supply Voltage, $V_{PP}-V_{NN}$	+220V
Positive High Voltage Supply, V_{PP}	-0.5V to +200V
Negative High Voltage Supply, V_{NN}	+0.5V to -200V
Logic Input Voltages	-0.5V to $V_{DD} + 0.3V$
Analog Signal Range, V_{SIG}	V_{NN} to V_{PP}
Peak Analog Signal Current/Channel	3A
Storage Temperature, T_S	-55°C to +150°C
Power Dissipation:	
48-Lead LQFP/TQFP	1W

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Positive High Voltage Supply	V_{PP}	+40	—	$V_{NN} + 200$	V	Note 1
Negative High Voltage Supply	V_{NN}	-10	—	-160	V	Note 1
Logic Power Supply Voltage	V_{DD}	+4.5	—	13.2	V	Note 1
High-level Input Voltage	V_{IH}	$0.8 V_{DD}$	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	$0.2 V_{DD}$	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	$V_{NN} + 10V$	—	$V_{PP} - 10V$	V	Note 2

Note 1: Power-up/power-down sequence is arbitrary except GND must be powered up first and powered down last.

2: V_{SIG} must be within $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power-up/power-down transition.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
Small Signal Switch ON-resistance	R _{ONS}	—	30	—	26	38	—	48	Ω	I _{SIG} = 5 mA	V _{PP} = +40V
		—	25	—	22	27	—	32	Ω	I _{SIG} = 200 mA	V _{NN} = −160V
		—	25	—	22	27	—	30	Ω	I _{SIG} = 5 mA	V _{PP} = +100V
		—	18	—	18	24	—	27	Ω	I _{SIG} = 200 mA	V _{NN} = −100V
		—	23	—	20	25	—	30	Ω	I _{SIG} = 5 mA	V _{PP} = +190V
		—	22	—	16	25	—	27	Ω	I _{SIG} = 200 mA	V _{NN} = −10V
Small Signal Switch ON-resistance Matching	ΔR _{ONS}	—	20	—	5	20	—	20	%	I _{SW} = 5 mA, V _{PP} = +100V, V _{NN} = −100V	
Large Signal Switch ON-resistance	R _{ONL}	—	—	—	15	—	—	—	Ω	V _{SIG} = V _{PP} −10V, I _{SIG} = 1A	
Output Switch Shunt Resistance	R _{INT}	—	—	20	35	50	—	—	kΩ	Output Switch to R _{GND} I _{RINT} = 0.5 mA	
DC Offset Switch OFF	V _{OS}	—	50	—	—	50	—	50	mV	No load, R _{GND} = 0V	
DC Offset Switch ON		—	50	—	—	50	—	50	mV		
Positive HV Supply Current	I _{PPQ}	—	—	—	10	50	—	—	μA	All SWs off	
Negative HV Supply Current	I _{NNQ}	—	—	—	−10	−50	—	—	μA		
Positive HV Supply Current	I _{PPQ}	—	—	—	10	50	—	—	μA	All SWs on, I _{SW} = 5 mA	
Negative HV Supply Current	I _{NNQ}	—	—	—	−10	−50	—	—	μA		
Switch Output Peak Current	I _{SW}	—	3	—	3	2	—	2	A	V _{SIG} duty cycle ≤ 0.1%	
Output Switching Frequency	f _{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
I _{PP} Supply Current	I _{PP}	—	6.5	—	—	7	—	8	mA	V _{PP} = +40V V _{NN} = −160V	50 kHz output switching frequency with no load
		—	4	—	—	5	—	5.5	mA	V _{PP} = +100V V _{NN} = −100V	
		—	4	—	—	5	—	5.5	mA	V _{PP} = +190V V _{NN} = −10V	
I _{NN} Supply Current	I _{NN}	—	6.5	—	—	7	—	8	mA	V _{PP} = +40V V _{NN} = −160V	50 kHz output switching frequency with no load
		—	4	—	—	5	—	5.5	mA	V _{PP} = +100V V _{NN} = −100V	
		—	4	—	—	5	—	5.5	mA	V _{PP} = +190V V _{NN} = −10V	
Logic Supply Average Current	I _{DD}	—	4	—	—	4	—	4	mA	f _{CLK} = 5 MHz, V _{DD} = 5V	
Logic Supply Quiescent Current	I _{DDQ}	—	10	—	—	10	—	10	μA	—	
Data Out Source Current	I _{SOR}	0.45	—	0.45	0.7	—	0.4	—	mA	V _{OUT} = V _{DD} −0.7V	
Data Out Sink Current	I _{SINK}	0.45	—	0.45	0.7	—	0.4	—	mA	V _{OUT} = 0.7V	
Logic Input Capacitance	C _{IN}	—	10	—	—	10	—	10	pF	—	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: over recommended operating conditions $V_{DD} = 5V$, unless otherwise noted.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Set-up Time before $\overline{LE}$ Rises	t_{SD}	150	—	150	—	—	150	—	ns	—
Time Width of $\overline{LE}$	t_{WLE}	150	—	150	—	—	150	—	ns	—
Clock Delay Time to Data Out	t_{DO}	—	150	—	—	150	—	150	ns	—
Time Width of CL	t_{WCL}	150	—	150	—	—	150	—	ns	—
Set-up Time Data to Clock	t_{SU}	15	—	15	8	—	20	—	ns	—
Hold Time Data from Clock	t_H	35	—	35	—	—	35	—	ns	—
Clock Frequency	f_{CLK}	—	5	—	—	5	—	5	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
Turn ON Time	t_{ON}	—	5	—	—	5	—	5	μs	$V_{SIG} = V_{PP} - 10V$, $R_L = 10 k\Omega$
Turn OFF Time	t_{OFF}	—	5	—	—	5	—	5	μs	$V_{SIG} = V_{PP} - 10V$, $R_L = 10 k\Omega$
Maximum V_{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	$V_{PP} = +40V$, $V_{NN} = -160V$
		—	20	—	—	20	—	20	V/ns	$V_{PP} = +100V$, $V_{NN} = -100V$
		—	20	—	—	20	—	20	V/ns	$V_{PP} = +190V$, $V_{NN} = -10V$
OFF Isolation	K_O	-30	—	-30	-33	—	-30	—	dB	$f = 5 MHz$, $1 k\Omega/15 pF$ load
		-58	—	-58	—	—	-58	—	dB	$f = 5 MHz$, 50Ω load
Switch Crosstalk	K_{CR}	-60	—	-60	-70	—	-60	—	dB	$f = 5 MHz$, 50Ω load
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle
OFF Capacitance SW to GND	$C_{SG(OFF)}$	5	17	5	12	17	5	17	pF	0V, $f = 1 MHz$
ON Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, $f = 1 MHz$
Output Voltage Spike	$+V_{SPK}$	—	150	—	—	150	—	150	mV	$R_{LOAD} = 50\Omega$
	$-V_{SPK}$	—	150	—	—	150	—	150	mV	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Temperature Range						
Operating Free-air Temperature	T_A	0	—	+70	°C	
Storage Temperature	T_S	-55	—	+150	°C	
Package Thermal Resistances						
48-Lead LQFP	θ_{JA}	—	52	—	°C/W	
48-Lead TQFP	θ_{JA}	—	42	—	°C/W	

2.0 PIN DESCRIPTION

The description of pins in the 48-Lead TQFP and 48-Lead LQFP packages are listed on [Table 2-1](#). The locations of the pads are listed in [Package Types†](#).

TABLE 2-1: 48-LEAD TQFP/LQFP PIN FUNCTION TABLE

Pin Number	Function	Pin Number	Function
1	N/C	25	$\overline{\text{SW5}}$
2	SW0	26	Y5
3	Y0	27	SW5
4	$\overline{\text{SW0}}$	28	N/C
5	N/C	29	$\overline{\text{SW3}}$
6	SW2	30	Y3
7	Y2	31	SW3
8	$\overline{\text{SW2}}$	32	N/C
9	N/C	33	$\overline{\text{SW1}}$
10	SW4	34	Y1
11	Y4	35	SW1
12	$\overline{\text{SW4}}$	36	N/C
13	N/C	37	RGND1
14	N/C	38	N/C
15	N/C	39	DOUT
16	VNN	40	VDD
17	N/C	41	DIN
18	N/C	42	CLR
19	N/C	43	$\overline{\text{LE}}$
20	N/C	44	CLK
21	VPP	45	GND
22	N/C	46	N/C
23	N/C	47	N/C
24	N/C	48	RGND2

3.0 FUNCTIONAL DESCRIPTION

3.1 Test Circuits

Figure 3-1 to Figure 3-6 show the test circuits for HV209.

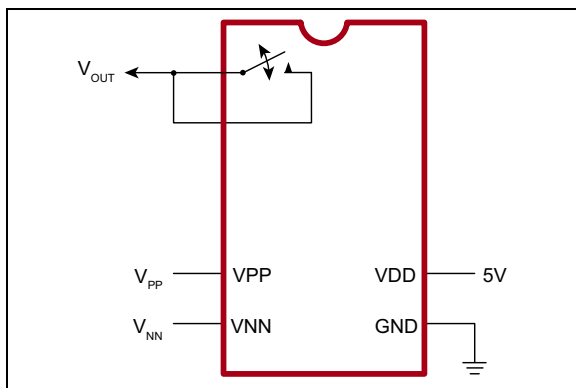


FIGURE 3-1: DC Offset ON/OFF.

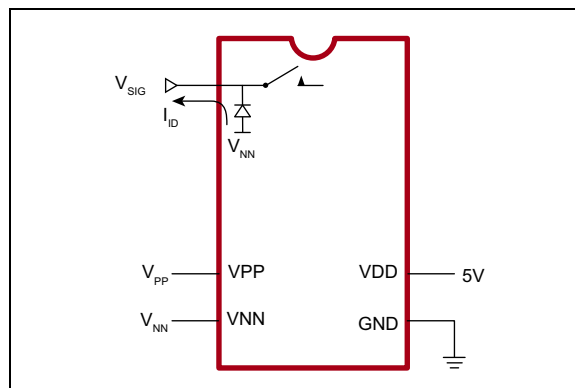


FIGURE 3-4: Isolation Diode Current.

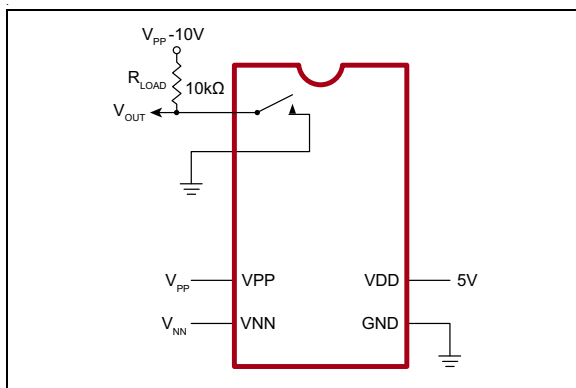


FIGURE 3-2: T_{ON}/T_{OFF} Test Circuit.

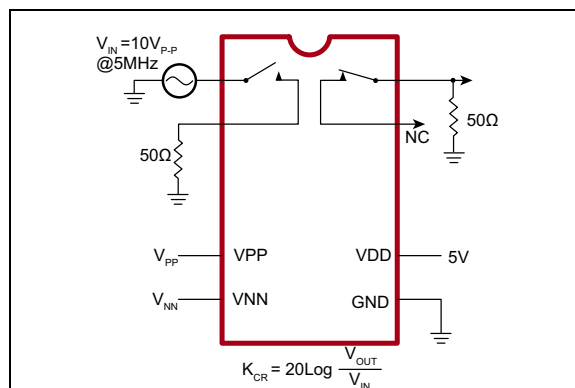


FIGURE 3-5: Crosstalk.

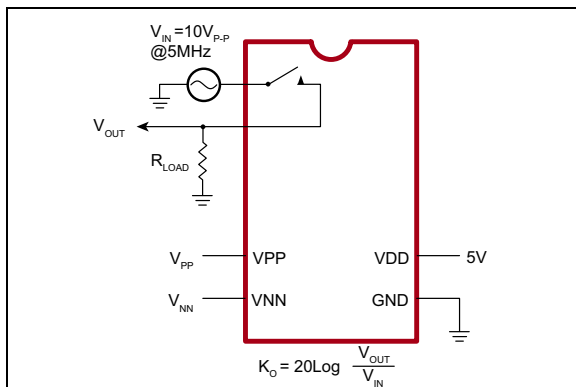


FIGURE 3-3: OFF Isolation.

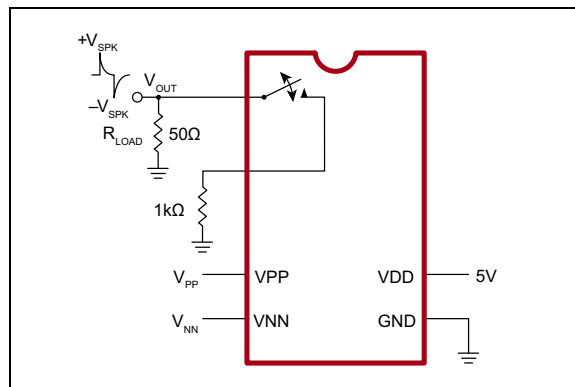


FIGURE 3-6: Output Voltage Spike.

TABLE 3-1: LOGIC TRUTH TABLE

Data Inputs						LE	CL	Switch States					
D0	D1	D2	D3	D4	D5			Y0	Y1	Y2	Y3	Y4	Y5
L						L	L	SW0					
H						L	L	SW0					
	L					L	L		SW1				
	H					L	L		SW1				
		L				L	L			SW2			
		H				L	L			SW2			
			L			L	L				SW3		
			H			L	L				SW3		
				L		L	L					SW4	
				H		L	L					SW4	
					L	L	L						SW5
					H	L	L						SW5
X	X	X	X	X	X	H	L	Hold Previous State					
X	X	X	X	X	X	X	H	SW0	SW1	SW2	SW3	SW4	SW5

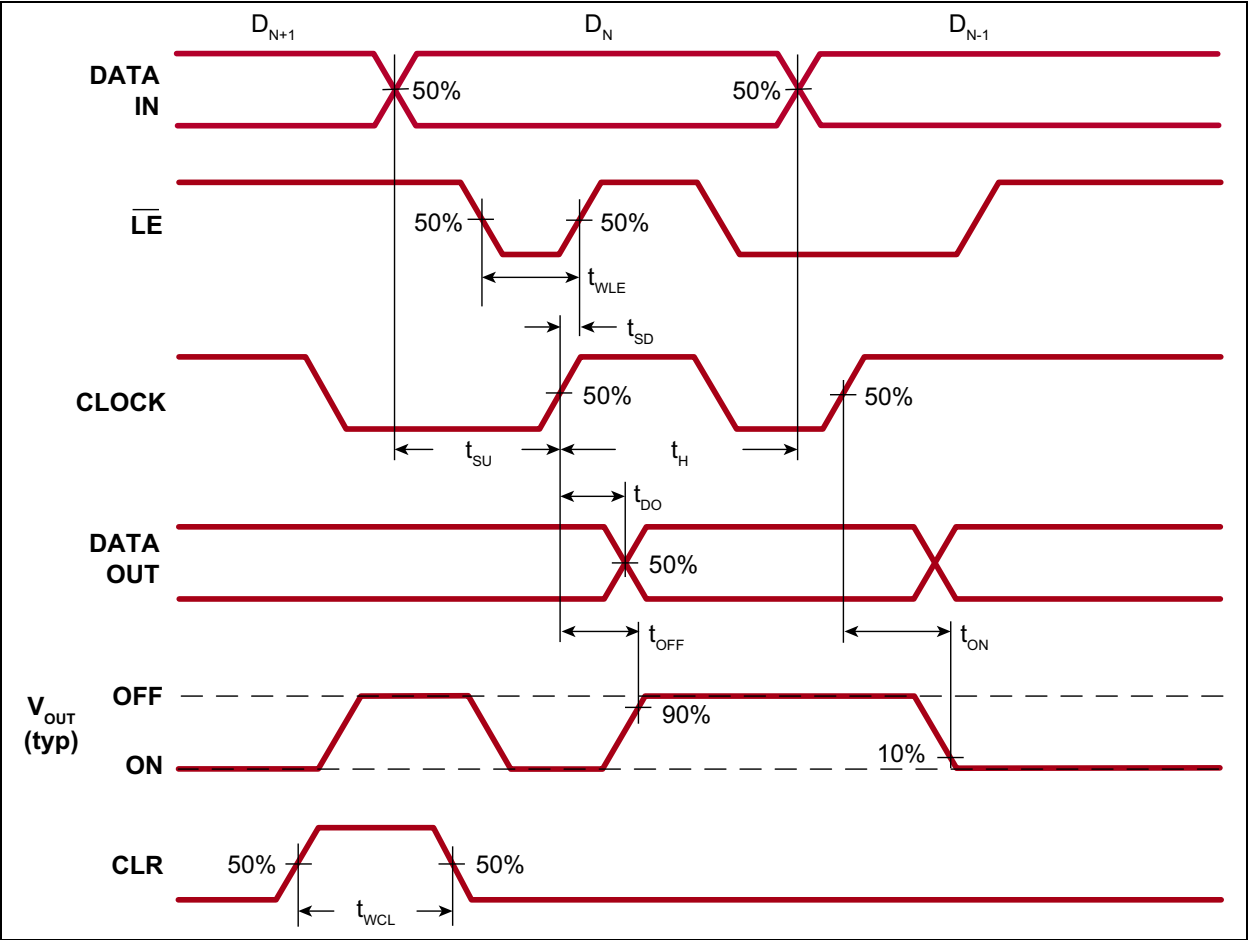


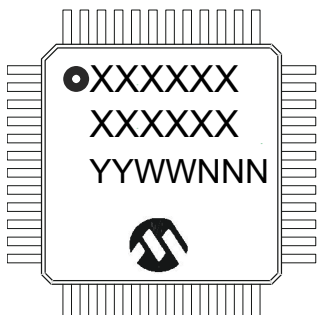
FIGURE 3-7: Logic Timing Waveforms

4.0 PACKAGING INFORMATION†

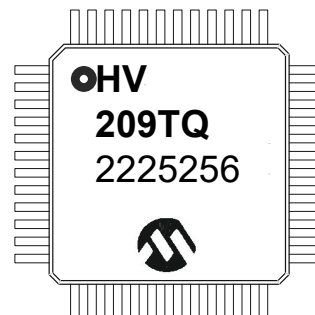
4.1 Package Marking Information

† **Notice:** The LQFP package is not recommended for new designs. Please use TQFP package as an alternative.

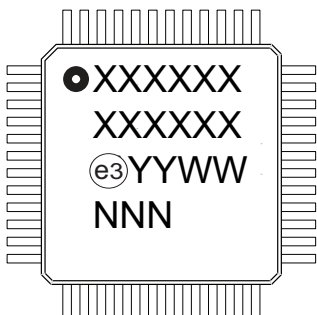
48-Lead TQFP



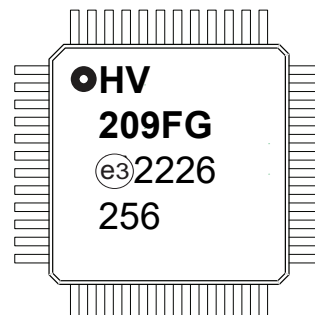
Example



48-Lead LQFP



Example

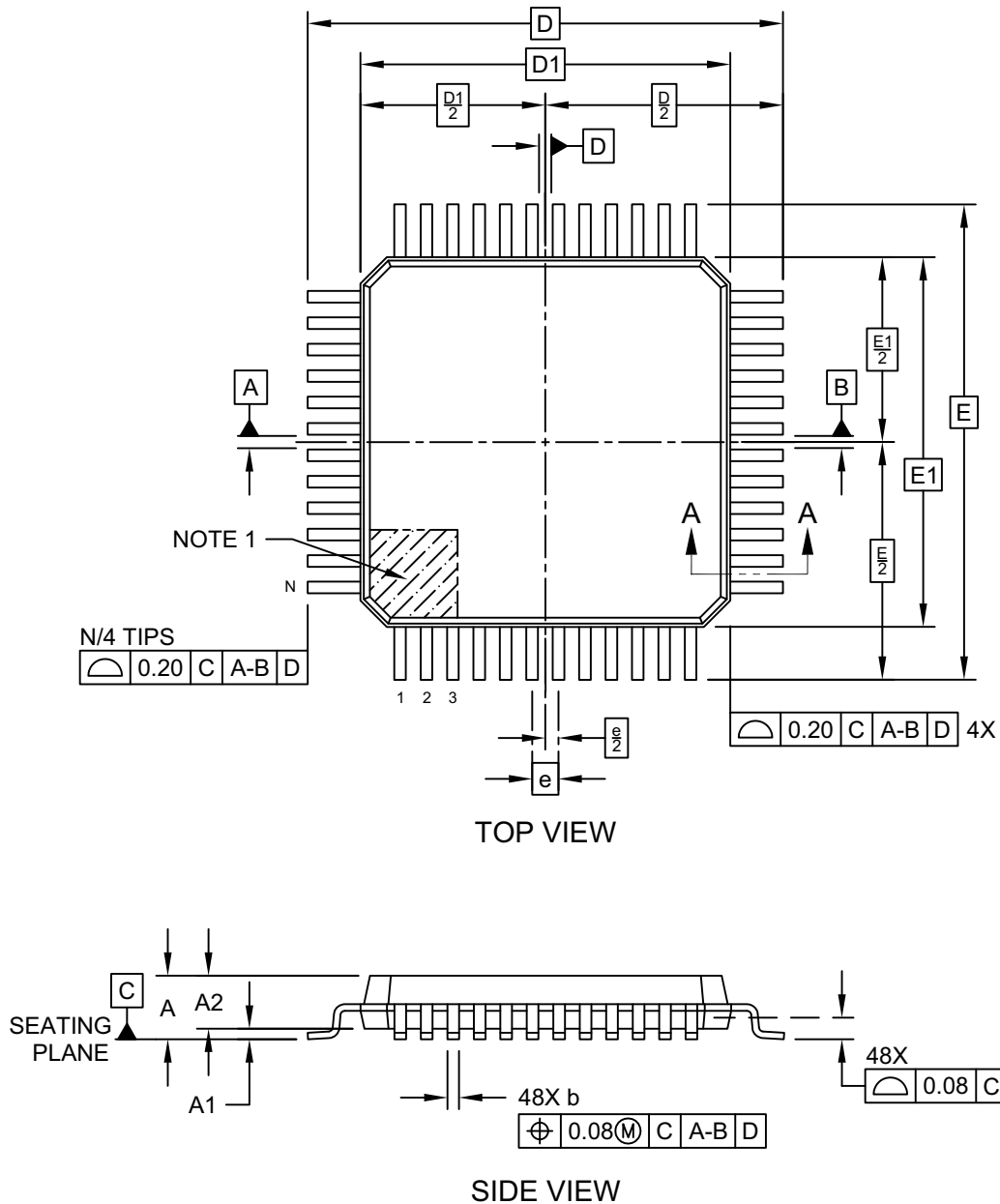


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

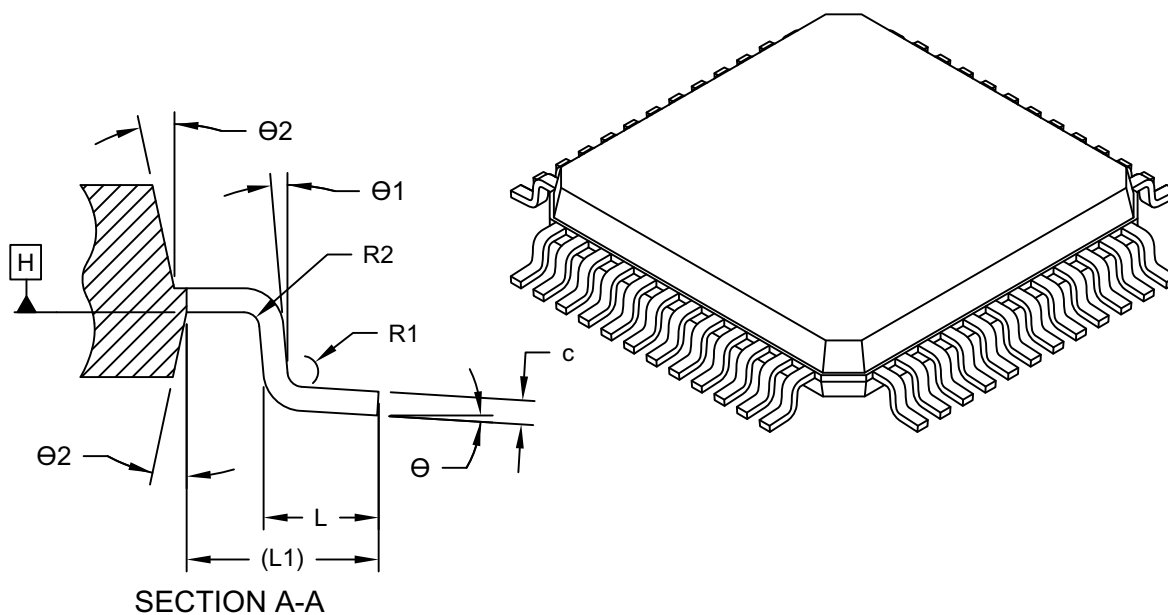
48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



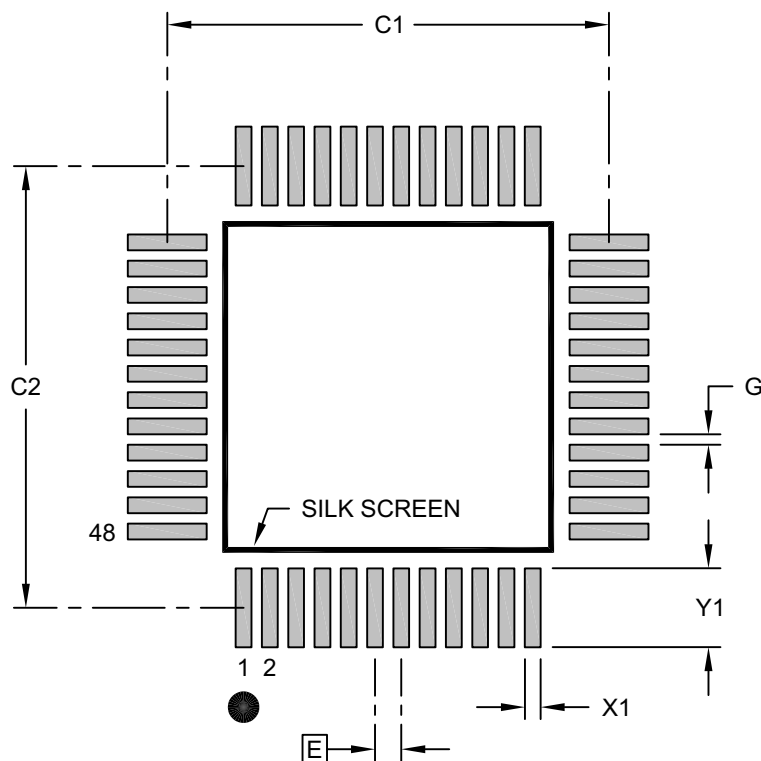
Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	48		
Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D	9.00 BSC		
Molded Package Length	D1	7.00 BSC		
Overall Width	E	9.00 BSC		
Molded Package Width	E1	7.00 BSC		
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		0.50 BSC		
Contact Pad Spacing	C1			8.40	
Contact Pad Spacing	C2			8.40	
Contact Pad Width (X48)	X1				0.30
Contact Pad Length (X48)	Y1				1.50
Distance Between Pads	G		0.20		

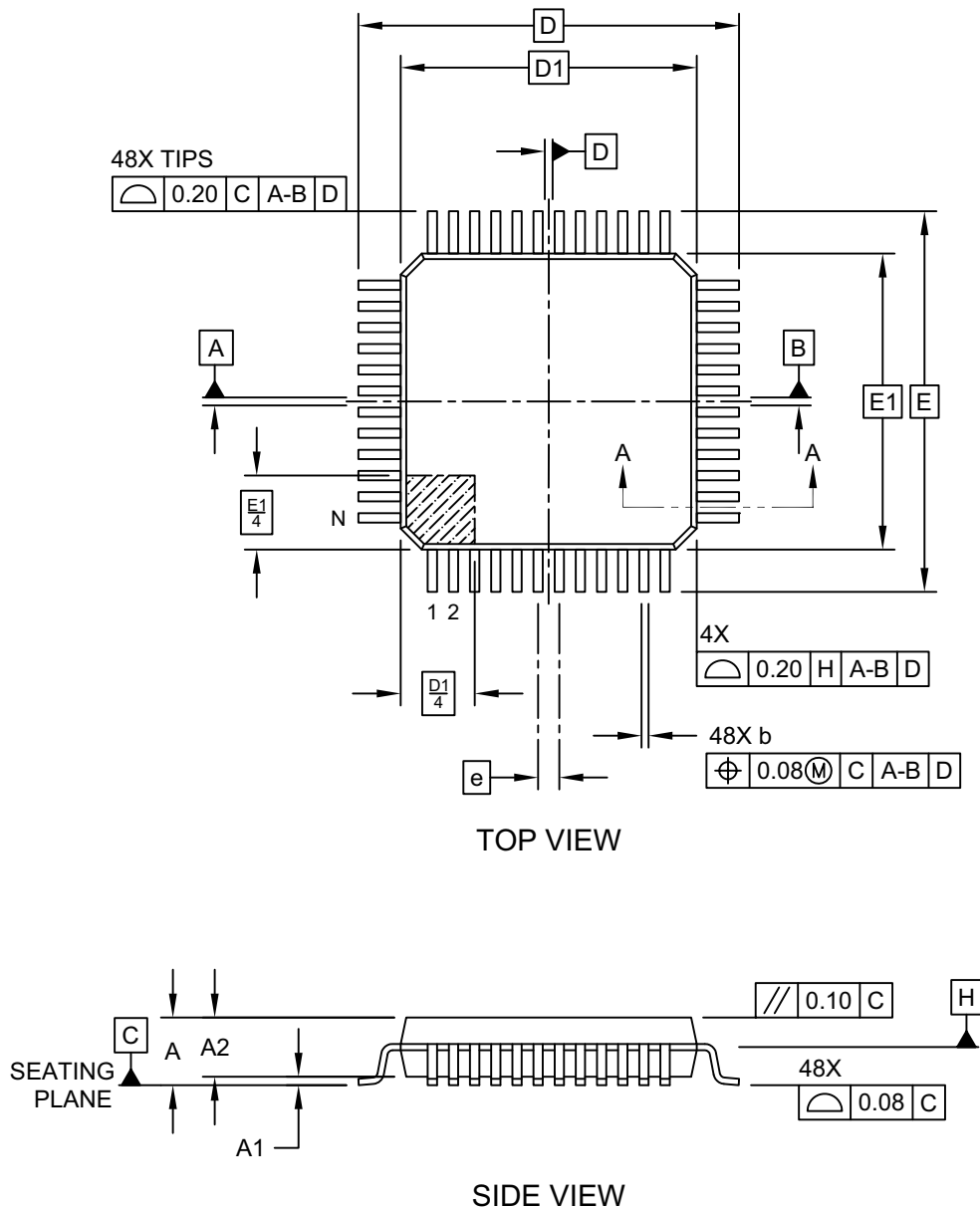
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-Y8X Rev D

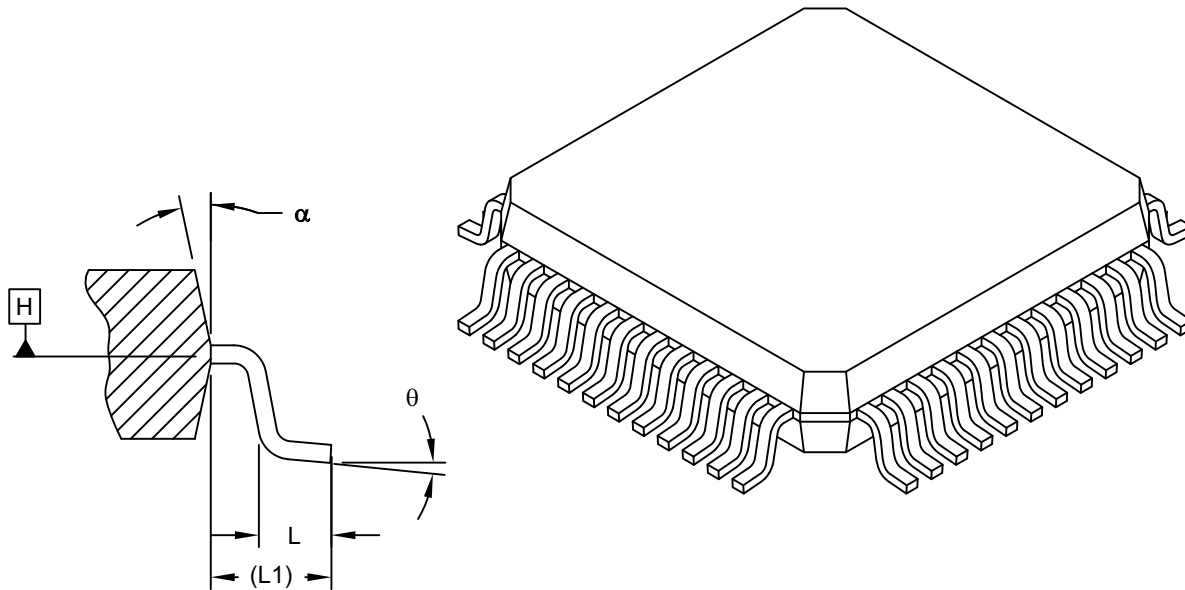
48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	48		
Lead Pitch	e	0.50 BSC		
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	θ	0°	3.5°	7°
Overall Width	E	9.00 BSC		
Overall Length	D	9.00 BSC		
Molded Package Width	E1	7.00 BSC		
Molded Package Length	D1	7.00 BSC		
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

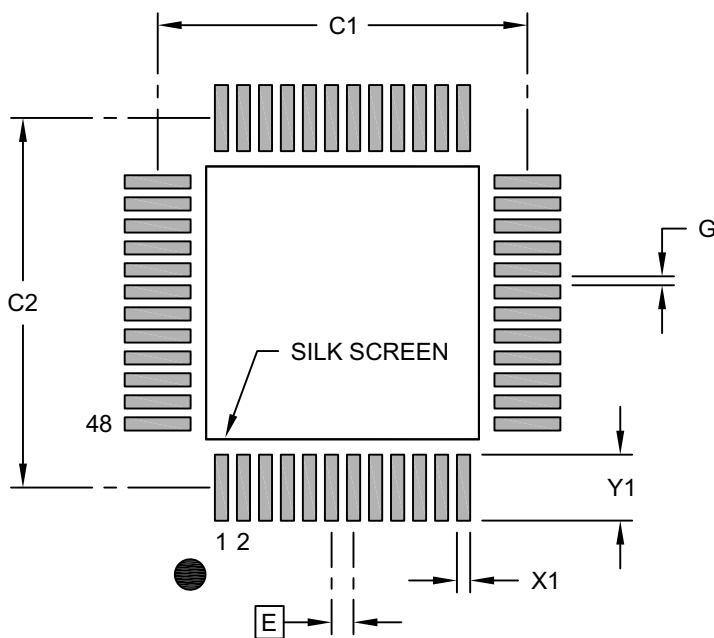
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-278A

HV209

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Converted Supertex Inc. Doc. # DSFP-HV209 B070213 to Microchip DS20006712A.
- Made minor edits for grammar.
- Added [Applications](#) and updated [Description](#).
- Added 48-Lead TQFP package.
- Updated [Package Marking Information](#).
- Added 48-Lead LQFP package notice to [Package Types[†]](#) and [Packaging Information[†]](#).

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	<u>-X</u>
Device	Package	Environmental
Devices:	HV209:	12-Channel High Voltage Analog Switch
Packages:	FG = 48-Lead LQFP	
	TQ = 48-Lead TQFP	
Environmental:	G =	Lead (Pb)-free/RoHS-compliant package

Examples:

a) HV209FG-G: 12-Channel High Voltage Analog Switch, 48-Lead LQFP Package, 250/Tray

b) HV209TQ-G: 12-Channel High Voltage Analog Switch, 48-Lead TQFP Package, 250/Tray

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
 - Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
 - Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
 - Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.
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