TITLE : HV050V01-100
Product Specification

Rev. O

BOE HYDIS TECHNOLOGY

REVISION HISTORY

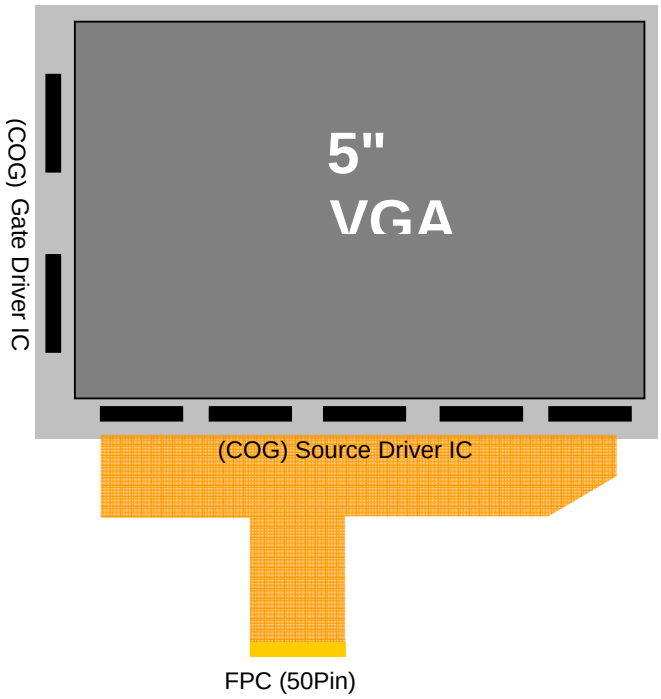
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
O	-	Initial Release	06.01.25	J.K. Han

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HV050V01-100 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as active switching devices. This module has a 5.0inch diagonally measured active area with VGA resolutions (640 horizontal by 480 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe. This module consists of a TFT-LCD panel manufactured by BOE HYDIS with COG Technique for Data and Gate.



1.2 Features

▷ Product Feature: HV050V01 Panel (Wide Temperature LC and AR Pol.) with COG and FPC

*PCB & BLU will be assembled by Customer.

- Wide Temperature Operations enable
- High Contrast Ratio and Wide Viewing Angle
- Thermal Heater and Sensor Adopted
- Portrait Type (O Mode Adopted)
- RoHS

1.3 Applications

- Marine Side / Avionics

1.4 General Specifications

The followings are general specifications at the model HV050V01-100.

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Panel Outline Dimension	110.9(H) × 87.45(V)	mm	
CF Outline Dimension	108.7(H) × 83.25(V)	mm	
Active area	101.76(H) X 76.32(V)	mm	
Number of pixels	640(H) × 480(V)	pixels	
Pixel pitch	0.0159(H) × 0.0159(V)	mm	
Pixel arrangement	RGB Vertical stripe	-	
Display mode	Normally Black (FFS)	-	
Operation Type	Portrait Type	-	O-Mode
Surface treatment	AR	-	
Liquid Crystal clearing temperature	≥ 103	℃	
Color filter chromaticity	x=0.312, y=0.342	-	
Panel Transmittance	6.0	%	Note. 1
ITO Resistance	25 ~ 40	Ohm/□	Note. 2

*Note 1) This value includes the recycling factor.

2.0 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

< Table 2. Environmental Maximum Specifications >

Parameter	Symbol	Min	Max	Unit	Remark
Operating Temperature	T_{OP}	-20	+85	℃	Note. 1

Note. 1) As compromised with Customer, D-IC and Polarizer are excluded within the range of guarantee for Operating Temperature.
D-IC : -10 ~ 75℃, Polarizer : -20 ~ 80℃

3.0 OPTICAL SPECIFICATIONS

3.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and ϕ equal to 0°. We refer to $\theta_{\phi=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{\phi=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{\phi=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{\phi=270}$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or ϕ, the center of the measuring spot on the display surface shall stay fixed. The measurement should be executed after 30 minutes with power-on of LED back-light at 18VDC voltage for warm-up period. The test setup, geometry, and measurement location are shown at FIGURE 1 and FIGURE 2 in Appendix.

3.2 Optical Specifications

To get the value in the following optical specifications, the electronics and back-light driving circuit must be optimized.

< Table 3. Optical Specifications >

Parameter		Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	CR > 10	-	89	90	Deg	Note 1
			-	89	90	Deg	
	Vertical		-	89	90	Deg	
			-	89	90	Deg	
Contrast Ratio		Θ = 0°	-	550	-		Note 2
Contrast Ratio (at 80° V.A.)		Θ = 80°	-	100	-		
CR Symmetry		Θ ≥ 60°	-	75	-		
Contrast Uniformity			-	75	-		
Black Level Uniformity			-	85	-		
CF Color Reproduction			-	45	-	%	
Response time (at 45℃)		Ttotal (Tr + Td)	-	-	35	msec	Note. 3
Cross talk			-	-	2.0	%	Note 4

Note)

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1 shown in Appendix).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The electro-optical response time measurements shall be made as FIGURE 2 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

4. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See FIGURE 3 shown in Appendix).

4.0 ELECTRICAL SPECIFICATIONS

4.1 Recommended electrical specification

Parameter		Min.	Typ.	Max.	Unit	Remarks
Digital Power Supply Voltage	VDD, VDD2	3.0	3.3	3.6	V	
Analog Power Supply Voltage	VDD1	7.98	8.05	8.07	V	For 2.2 Gamma Curve
γ 1-corrected Power Supply Voltage	GMA1	7.81	7.88	7.95	V	
γ 2-corrected Power Supply Voltage	GMA2	6.55	6.62	6.69	V	
γ 3-corrected Power Supply Voltage	GMA3	6.01	6.07	6.13	V	
γ 4-corrected Power Supply Voltage	GMA4	5.52	5.58	5.64	V	
γ 5-corrected Power Supply Voltage	GMA5	4.16	4.21	4.26	V	
γ 6-corrected Power Supply Voltage	GMA6	3.79	3.84	3.89	V	
γ 7-corrected Power Supply Voltage	GMA7	2.43	2.47	2.51	V	
γ 8-corrected Power Supply Voltage	GMA8	1.94	1.98	2.02	V	
γ 9-corrected Power Supply Voltage	GMA9	1.40	1.43	1.46	V	
γ 10-corrected Power Supply Voltage	GMA10	0.14	0.17	0.20	V	
Panel Common Power Supply	PCOM	2.94	3.19	3.44	V	Note 1.2.
Gate Driver Positive Power Supply	VCOM	22	23	24	V	
Gate Driver Negative Power Supply	VEE	-6.7	-7.2	-7.7	V	
Permissible Input Ripple Voltage	VRF			100	mV	At VDD = 3.3V

Note 1 : Panel common power(PCOM) has to optimize at flicker pattern with variable voltage circuit.
This circuit has to be composed of variable resister.

Note 2 : Flicker pattern is one pixel skip green pattern. Green
6bits data is 100000. The other data is 000000.

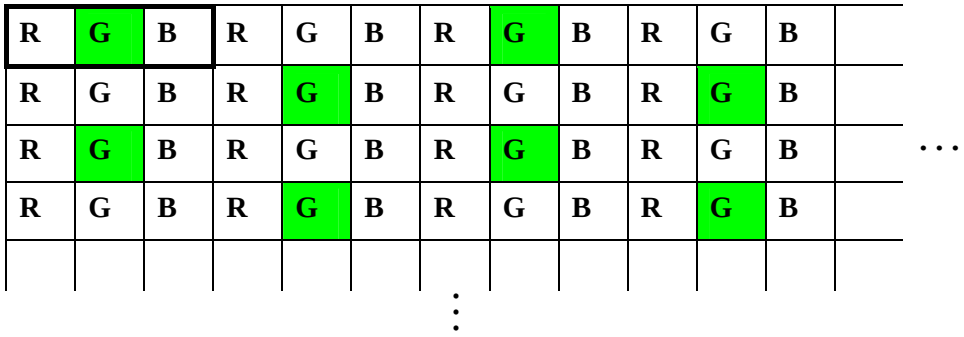


Figure. Flicker pattern

※ The others electrical specifications are refered to APPENDIX.

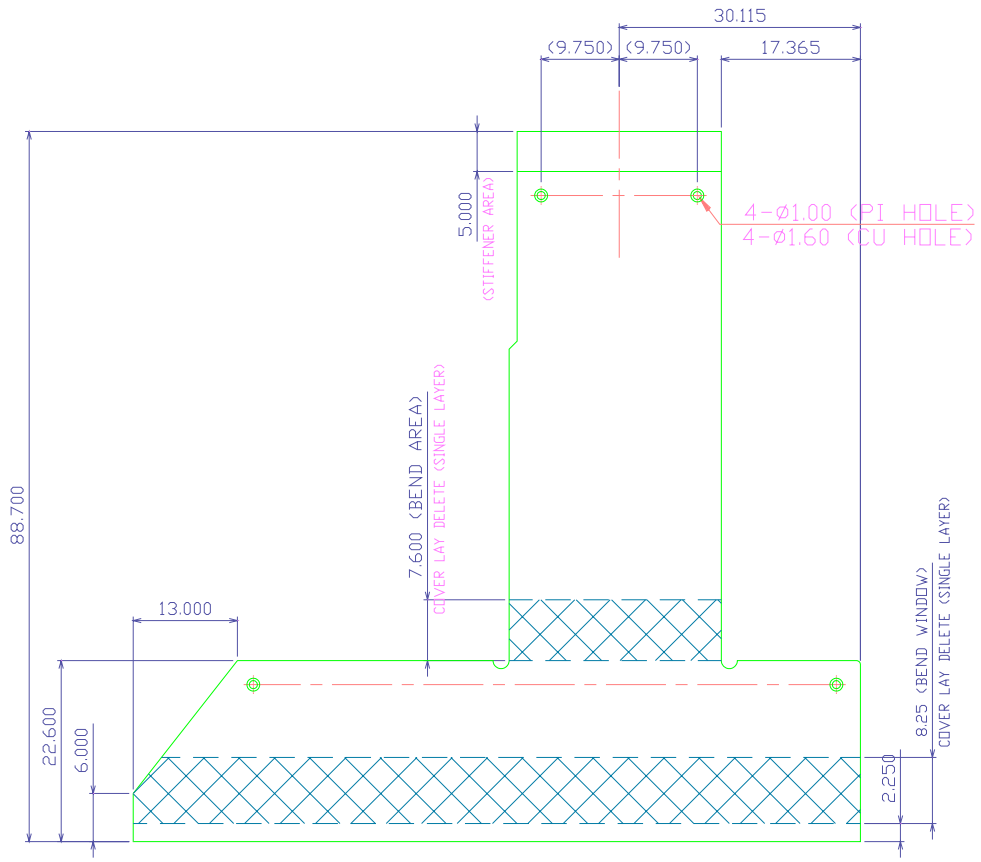
5.0 FPC

5.1 FPC PIN ASSIGNMENTS

No.	Signal Name	Signal Descriptions	Comment
1	VCOM_1	Vcom	
2	GND	GND	
3	TS1_IN	Thermal Sensor 1 In	+12V
4	TS1_OUT	Thermal Sensor 1 Out	5 Mohm to Ground
5	VDD_5	VDD	Analog Voltage
6	GMANB	Gamma Negative Bottom	
7	GMANC	Gamma Negative Center	
8	GMANT	Gamma Negative Top	
9	VTT_9	VTT	
10	EIO2	Source Start Pulse2	
11	XLR	Left / Right	
12	VTT_12	VTT	
13	LV0A	LVDS 0 A	
14	LV0B	LVDS 0 B	
15	GND	GND	
16	LV1A	LVDS 1 A	
17	LV1B	LVDS 1 B	
18	GND	GND	
19	LVCLKA	LVDS Clock A	
20	LVCLKB	LVDS Clock B	
21	GND	GND	
22	LV2A	LVDS 2 A	
23	LV2B	LVDS 2 B	
24	GND	GND	
25	LV3A	LVDS 3 A	
26	LV3B	LVDS 3 B	
27	TS2_IN	Thermal Sensor 2 In	+12V
28	TS2_OUT	Thermal Sensor 2 Out	5 Mohm to Ground
29	VTT_29	VTT	
30	GND	GND	
31	POL	Inversion Polarity	
32	TP1	Timing/Control Pulse	
33	EIO1	Source Start Pulse 1	
34	VTT_34	VTT	
35	GMAPB	Gamma Positive Bottom	
36	GMAPC	Gamma Positive Center	
37	GMAPT	Gamma Positive Top	
38	VDD_38	VDD	
39	GND	GND	
40	VCOM_40	Vcom	
41	VGL_41	VGL	Gate Off Voltage
42	VGH	VGH	Gate On Voltage
43	GSC	Gate Clock	

44	DIO2	Gate Start Pulse2	
45	DIS	Gate Clock Disable	
46	VTT_46	VTT	
47	VGL_47	VGL	
48	VCOM_48	Vcom	
49	DIR	Up / Down	
50	DIO1	Gate Start Pulse1	

5.2 FPC Drawing



6.0 X-Driver IC

6.1.Pin Description

Pin Name	I/O	Description	Function
LVCLKA/B	I	Clock (mini-LVDS)	Shift clock input (Reeiver) Getting a clock by mini-LVDS signal.
LVCLKAT1/BT1 LVCLKAT2/BT2	O	Clock (mini-LVDS)	Shift clock output(Transmitter). Output of same clock from receiver input. The function is controlled by XLR_LV.
LV0A/B to LV3A/B	O	Display Data (mini-LVDS)	Display data input (Receiver). Getting a display data with gray-scale data (6bit) and control signal. (RST=reset).
LV0AT1/BT1 to LV3AT1/BT1 LV0AT2/BT2 to LV3AT2/BT2	O	Display data (mini-LVDS)	Display data output (Transmitter). Output of same data from receiver input. The function is controlled by XLR_LV.
XLR	I	Shift direction	Control the direction of the loaded data at the shift-register.
XLR_LV	I	mini-LVDS output control	Control output definition of mini-LVDS display data and clock terminals.
EIO1 , EIO2	I/O	Start pulse	Input/Output definition of address shift-register
TP1_1 TP1_2	I	Input mode and output timing control	Change the input mode, latched the registered data and transfer to DAC at the rising edge. And supplied voltage to LCD pixel is output at falling edge. TP1_1 or TP1_2 is selected by XLR_LV.
POL_1 POL_2	I	Polarity control	Control the polarity of the output. Define by the POL signal at TP1 as "H". TP1_1 or TP1_2 is selected by XLR_LV.
LP_1 LP_2	I	Low power mode selection	Decrease the charge/discharge current to output load. LP_1/2=H : Low power mode LP_1/2=L : Normal mode TP1_1 or TP1_2 is selected by XLR_LV.
SQINV	I	Inversion mode selection	Select inversion mode between dot inversion or square inversion. SQINV=L : dot inversion SQINV=H :square inversion
LCH	O	Drivability control	Control LCD output drivability. LCH=H : Normal mode LCH=L : Light load mode
VBDATA	I	Output BIAS current control (option pin)	Control output BIAS current VBDATA=L : default VBDATA=H : more current mode
VLB	I	Rx BIAS current control (option pin)	Control mini-LVDS receiver's BIAS current. VLB=L : default
TEST1 TEST2	I	Test (option pin)	For testing Both TEST1 and TEST2 should be connected to VSS2* for the normal operation.
VCOM 1 VCOM2	I/O	VCOM through terminal	Each VCOM1 and VCOM2 are connected inside driver IC.

OUT1 to OUT384	O	LCD output	Output of supplied voltage to each LCD pixels
VDD1 VSS1	I	Power supply (Output circuits)	Power supply for output (driving) circuits
VDD2(ANA) VDD2(LOG) VSS2(ANA) VSS2(LOG) VSS* VDD2* VSS2*	I	Power supply (Control=logic Circuits)	VDD2(ANA) is for mini-LVDS's I/F and VDD2(LOG) is for other logic circuits. Supply the stable voltage to VDD2(ANA). VDD2(ANA) and VDD2(LOG) should be same electric potential. Possible to wire VSS2(ANA) between each mini-LVDS signal line from VSS* terminal. Though no-wiring, no-relation to function, itself. VDD2* and VSS2* can set XLR , XLR_LV , LP , SQINV , LCH and option pins to "H" or "L" by connecting. No need to supply to ,VDD2* and VSS2* from external power supply.
GMAPT/PC/PB to GMANT/NC/NB	I	γ -corrected power supplies	Input the γ -corrected power supplies from out- side by using operational-amplifier. Maintain the recommended operating conditions.

6.2. Function table (XLR_LV and mini-LVDS input/output)

Pin Name	XLR_LV = H	XLR_LV = L
LVCLKA (LVCLK+)	Input	
LVCLKB (LVCLK-)	Input	
LVCLKAT1 (LVCLK+)	-	Output
LVCLKBT1 (LVCLK-)	-	Output
LVCLKAT2(LVCLK+)	Output	-
LVCLKBT2(LVCLK-)	Output	-
LV0A (LV0+)	Input	
LV0B (LV0-)	Input	
LV1A (LV1+)	Input	
LV1B (LV1-)	Input	
LV2A (LV2+)	Input	
LV2B (LV2-)	Input	
LV3A (LV3+)	Input	
LV3B (LV3-)	Input	
LV0AT1 (LV0+)	-	Output
LV0BT1 (LV0-)	-	Output
LV0AT2 (LV0+)	Output	-
LV0BT2 (LV0-)	Output	-
LV1AT1 (LV1+)	-	Output
LV1BT1 (LV1-)	-	Output
LV1AT2 (LV1+)	Output	-
LV1BT2 (LV1-)	Output	-
LV2AT1 (LV2+)	-	Output
LV2BT1 (LV2-)	-	Output
LV2AT2 (LV2+)	Output	-
LV2BT2 (LV2-)	Output	-
LV3AT1 (LV3+)	-	Output
LV3BT1 (LV3-)	-	Output
LV3AT2 (LV3+)	Output	-
LV3BT2 (LV3-)	Output	-

Note : Suffix "+" indicates positive potential and "- " indicates negative potential at each differential signal input pair.

6.3 Function Table (XLR and EIOn)

XLR	EIO1	EIO2	Shift Direction
H	Right shift : In	Right shift : Out	OUT1 -> OUT 384
L	Left shift : Out	Left shift : In	OUT384 -> OUT 1

Note : shows the direction of mini-LVDS signals and display data sampling as an example.

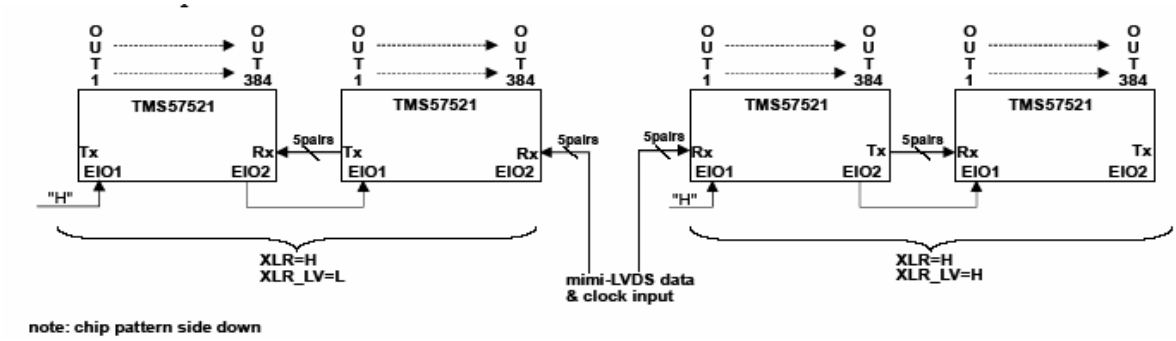


Figure . The direction of mini-LVDS signals and display

6.4 Function Table (XLR_LV and TP1/2 / POL_1/2 / LP_1/2)

XLR_LV	TP1_1	TP1_2	POL_1	POL_2	LP_1	LP_2
H	-	Input	-	Input	-	Input
L	Input	-	Input	-	Input	-

6.5 Dot Inversion Function Table (POL_1/2 and reference GAMMA)

POL_1/2	ODD numbered output	EVEN numbered output
H	GMANT to GMANB	GMAPT to GMAPB
L	GMAPT to GMAPB	GMANT to GMANB

6.6 Square inversion function Table (POL_1/2 and reference GAMMA)

POL_1/2	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	…….	OUT384
L	+	-	-	+	+	-	…….	+
L	+	-	-	+	+	-	…….	+
H	-	+	+	-	-	+	…….	-
H	-	+	+	-	-	+	…….	-

+ : GMAPT to GMAPB

7.0 Y-Drive IC

7.1.Pin Description

Pin Name	I/O	Function
VGH	Input	Voltage source for LCD panel control output (High level).
VDD	Input	Voltage source for input signal
VSS	Input	GND for input signal
VGL	Input	Voltage source for LCD panel control output (Low level)
CLK(CLK_L)	Input	Vertical shift clock input. It is used as shift clock of shift register. Data is synchronized with the rising edge of this signal.
DIR(DIR_L)	Input	Data shift direction control pin. Data shift direction; DIR = High : DIO1 →OUT1 →OUT2 ……OUT239 →OUT240 →DIO2 DIR = Low : DIO2 →OUT240 →OUT239 ……OUT2 →OUT1 →DIO1.7
OEB(OEB_L)	Input	Output enable control pins. When OEB pin is ` H`, the LCD panel control outputs are fixed at `VGL`, with shift register not cleared. OEB signal is asynchronous with CLK.
DIO1,DIO2	Input / Output	Input /Output pin for vertical synchronous signal. According to the status of DIR input, these pins can be used as input pin for vertical synchronous signal or output pin for carry signal to the next cascaded gate driver IC. The carry signal is used as vertical synchronous signal of next cascaded gate driver and synchronized with falling edge of CLK. Pin assignment DIR = L DIO1 is output pin for carry signal. DIO2 is input pin for vertical synchronous signal. DIR = H : DIO1 is input pin for vertical synchronous signal. DIO2 is output pin for carry signal.
OUT1~OUT240	Input	Output pins for LCD panel driving.

7.2. Operation Description

7.2.1. Voltage Level of Input And Output Signals.

-The voltage levels of input signals are as follows:

`H` level = VDD

`L` level = VSS

-The voltage levels of carry output signal (DIO1, 2) are as follows:

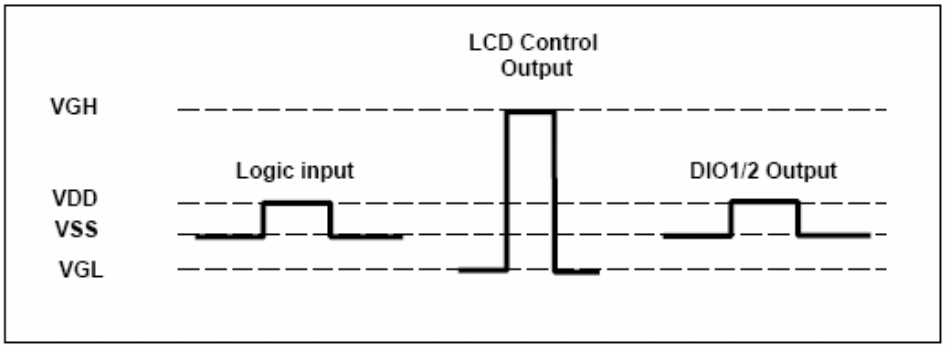
`H` level = VDD

`L` level = VSS

-The voltage levels of LCD control outputs are as follows:

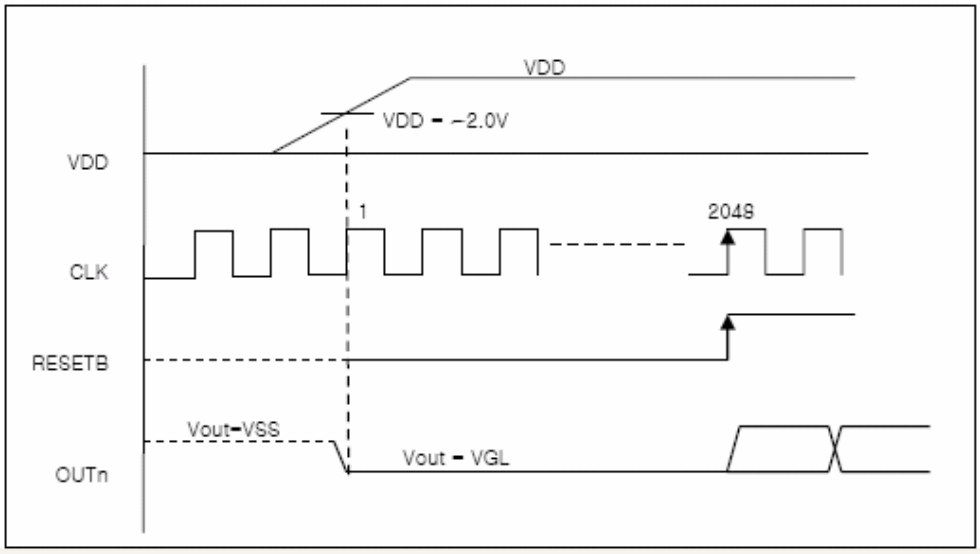
`H` level = VGH

`L` level = VGL



Voltage Level of Input and Output Signals.

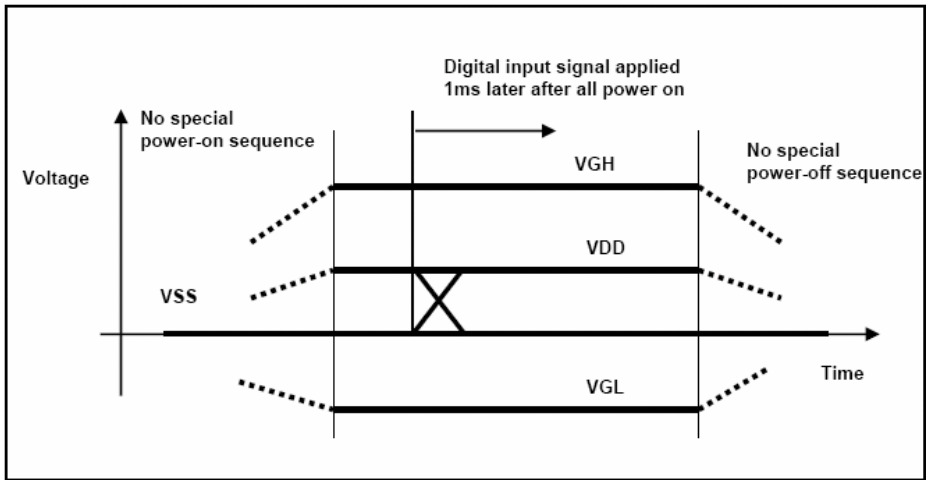
7.2.2 Power–on-reset function



note . Power-on-reset function of HM10G240A provide that all output voltage keep VGL level until 2048 clocks in to the device after the VDD reached about 2.0V.

7.3 Power On/Off sequence

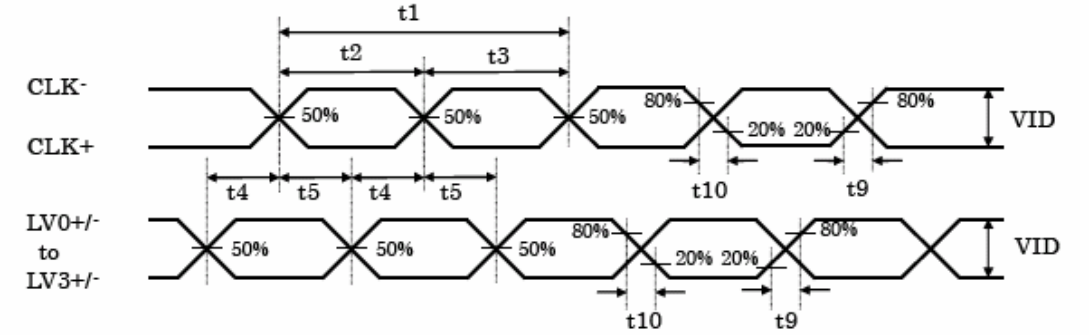
7.3.1. No special power ON/OFF sequences are required.
7.3.2. If possible, it is recommended that all digital input signals are stay in VSS, or VDD level until all powers are applied.
7.3.3. If there is some glitch during the power-on, or power-off stage, the voltage of glitch voltage must be less than as following voltage range ;
VGH Terminal Glitch Voltage : -0.3V ~ 40V
VDD Terminal Glitch Voltage : -0.3V ~ 7.0V
VGL Terminal Glitch Voltage : 0.3V ~ -20V
VGH-VGL Voltage Difference : -0.3V ~ 40V
Signal Input Glitch Voltage : -0.3V ~ 7.0V



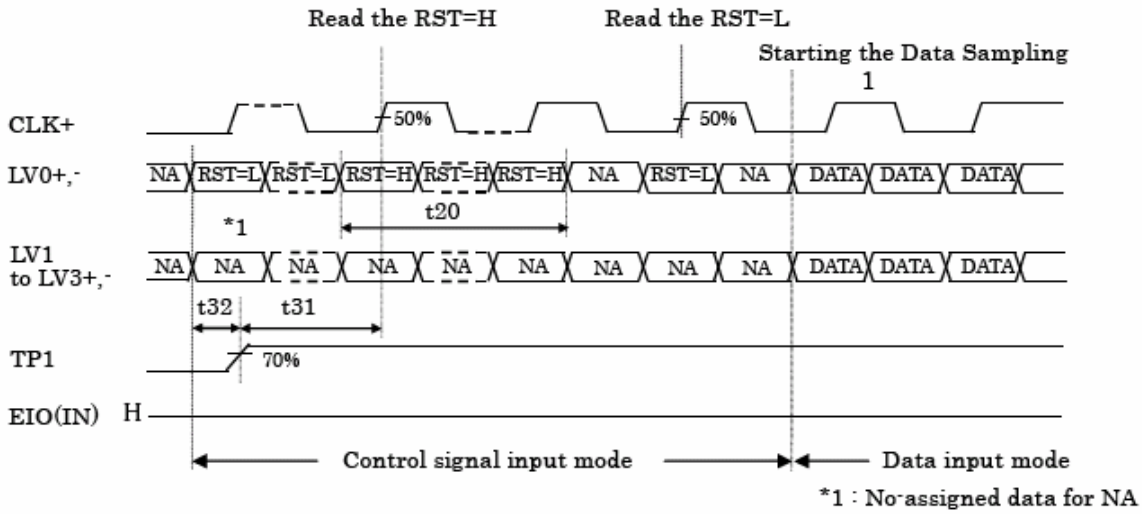
8.0 SIGNAL TIMING SPECIFICATION

8.1 X-Driver Timing Chart

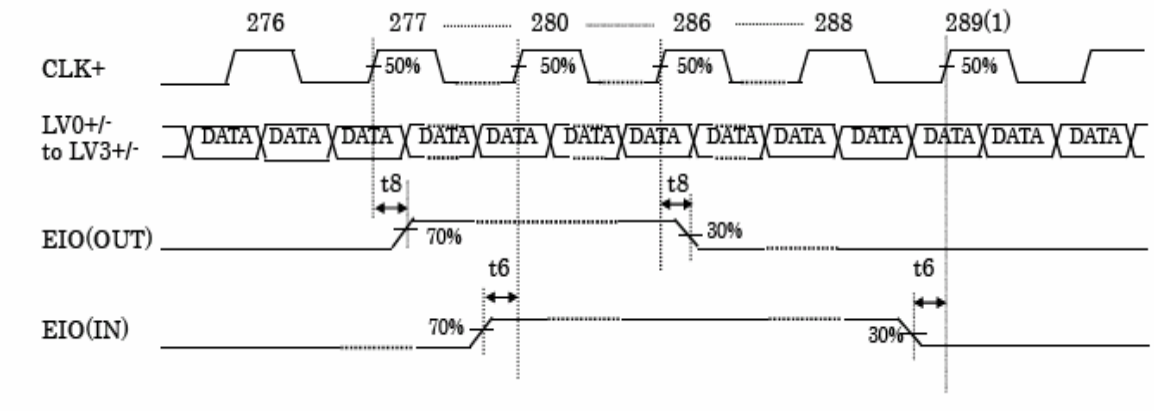
8.1.1 Timing of taking data in



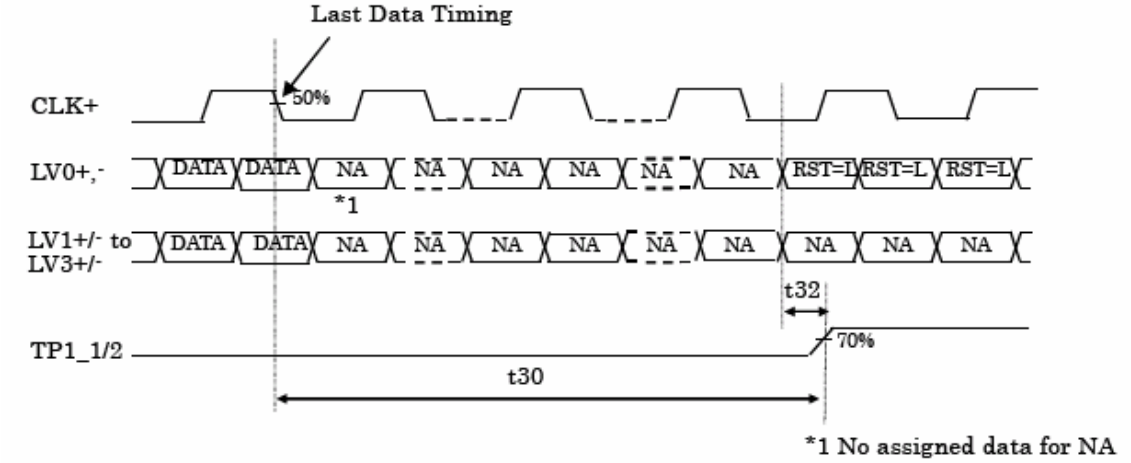
8.1.2. Input data timing (Lead chip)



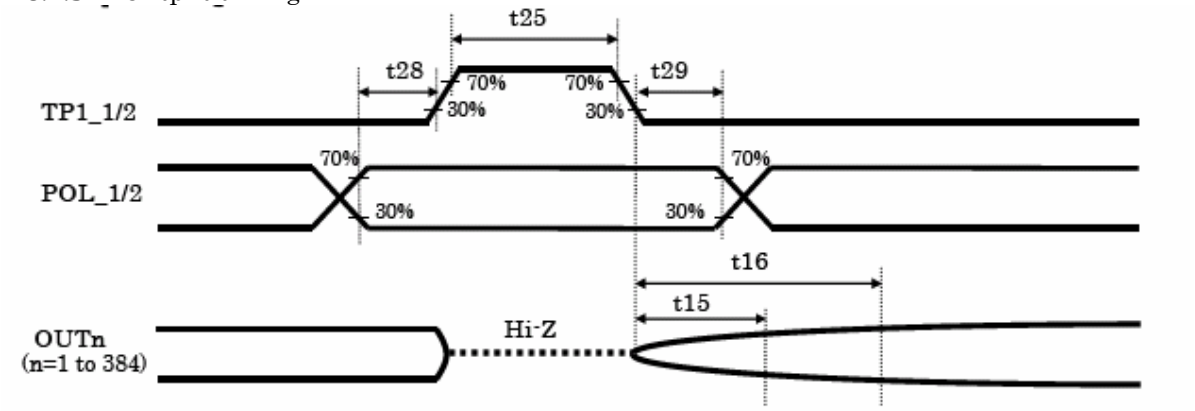
8.1.3. Input data timing (Cascade port)



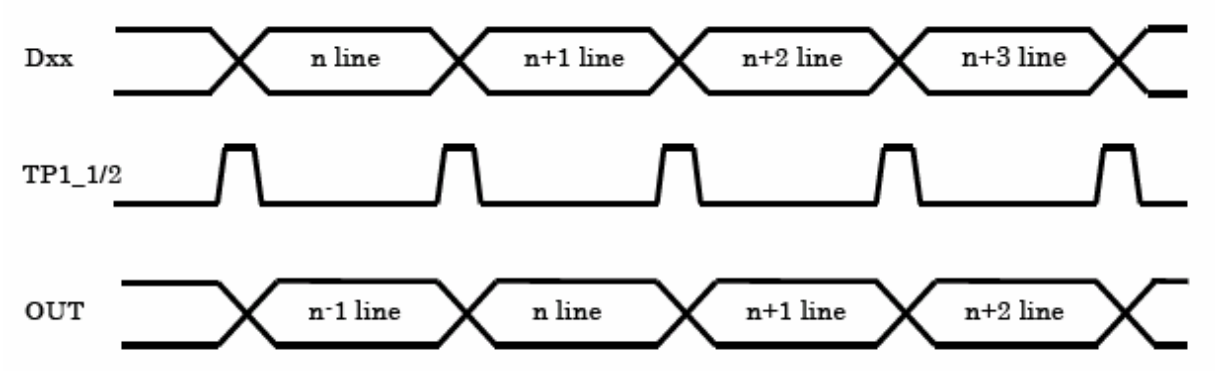
8.1.4. Last data sampling to TP1 timing



8.1.5 _ Output timing



8.1.6. Relation between input data and output



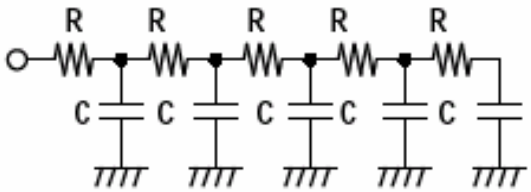
8.1.7. AC electrical characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
Clock Pulse Cycle	t1		6.25	6.58		ns
Clock Pulse High Period	t2		2.5			ns
Clock Pulse Low Period	t3		2.5			ns
Data Setup Time	t4		1.1			ns
Data Hold Time	t5		1.1			ns
EIO Setup Time	t6		-1.0			ns
EIO Signal Delay Time	t8	Load=10pF			19.5	ns
CLK, LV0 to LV3 Rising Time	t9				0.8	ns
CLK, LV0 to LV3 Falling Time	t10				0.8	ns
Driver Output Delay Time *1	t15	Target Voltage ±0.1 VDD1			4	µs
	t16	6 bit Accuracy			8	µs
Reset (RST) High Period	t20		Over 50ns, moreover 3CLK cycle			-
TP1 High Period	t25		0.2			µs
POL Setup Time	t28		-5.0			ns
POL Hold Time	t29		3.0			ns

Receiver off to TP1 Timing	t30		9			CLK cycle
TP1 to Reset Input Time	t31		200			ns
Reset Low to TP1 Rising Time	t32		0			ns

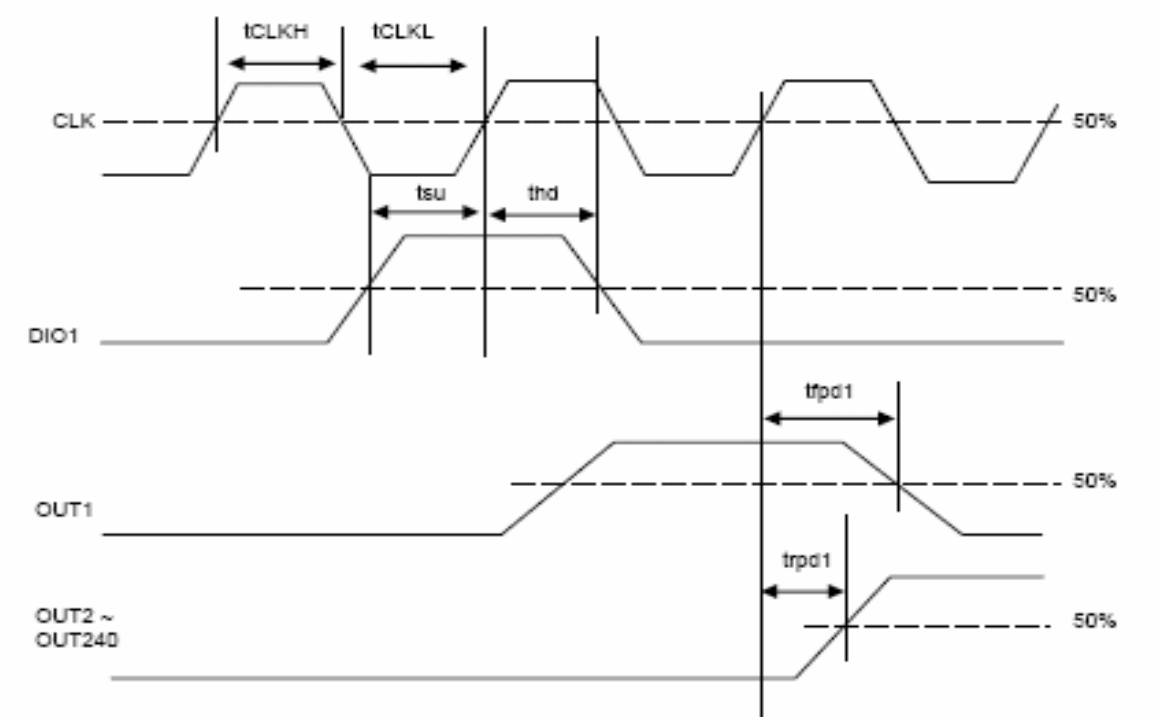
Note. Output Load Condition

$R = 6k\Omega$
$C = 20pF$

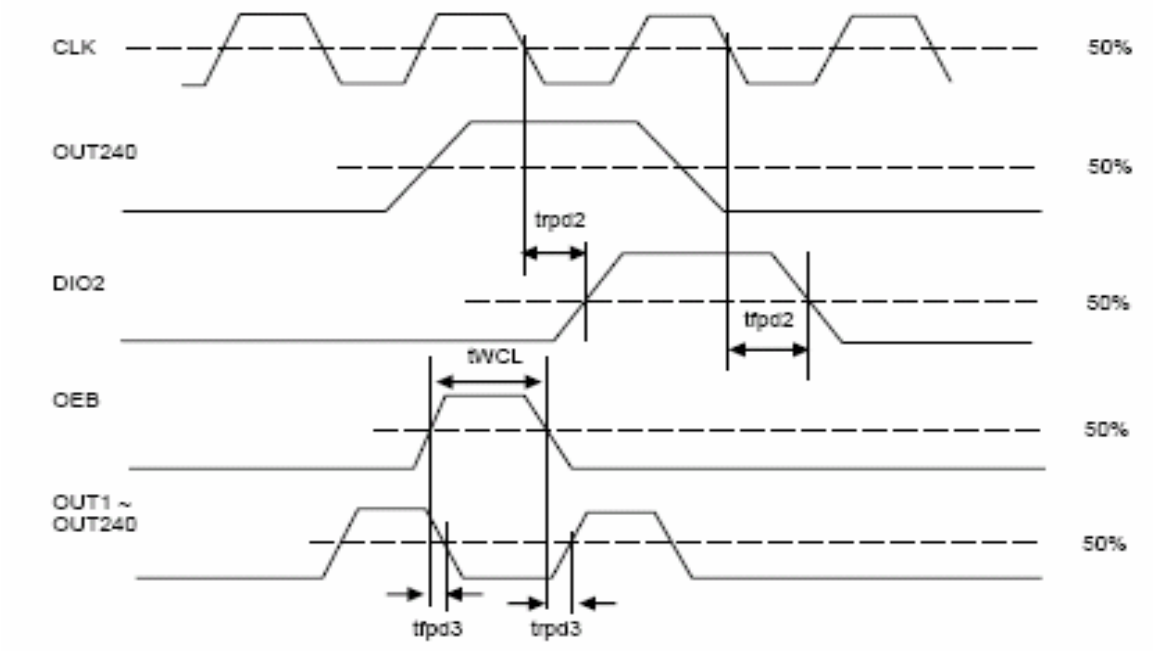


8.2. Y-Driver Timing Chart

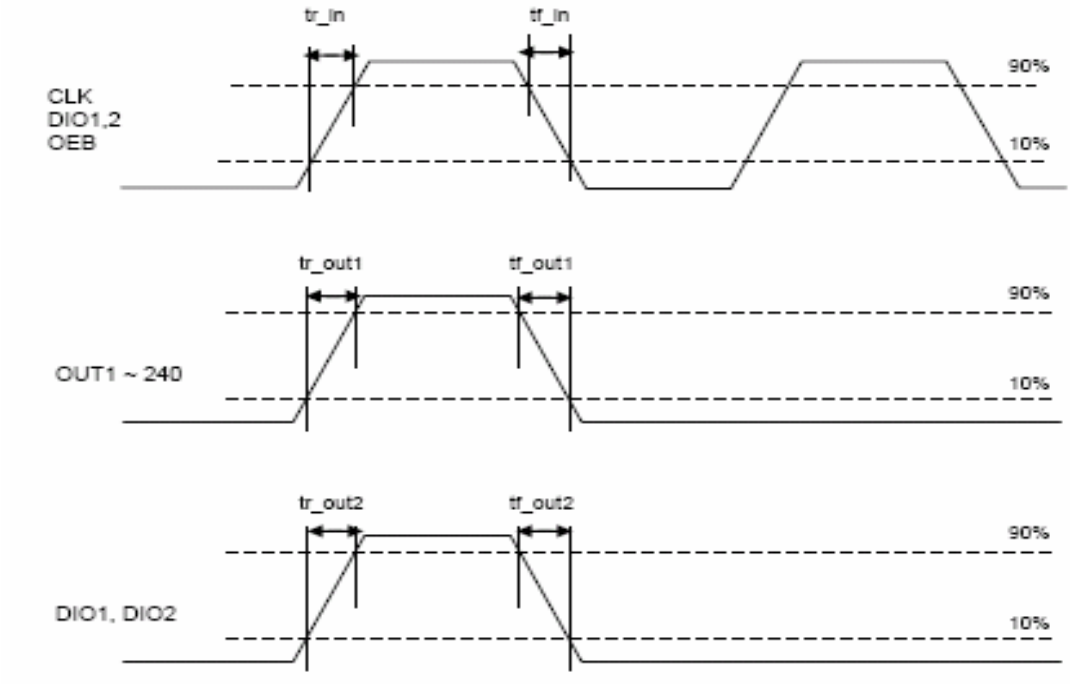
8.2.1. LCD output propagation delay



8.2.2. Vertical synchronous output propagation delay



8.2.3. Definition of rising time and falling time



8.2.4. AC Characteristics under recommended operating conditions

ITEM	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Clock frequency	fCLK			500	kHz
CLK clock pulse width	tCLKH, tCLKL	Duty=50%	3.0		us
OEB signal pulse width	tWCL		1.0		us
Data setup time	tsu		700		ns
Data hold time	thd		700		ns
Output delay time1	trpd1	CL=300pF		500	ns
Output delay time2	tfpd1	CL=300pF		500	ns
Output delay time3	trpd2	CL=30pF		500	ns
Output delay time4	tfpd2	CL=30pF		500	ns
Output delay time5	trpd3	CL=300pF		500	ns
Output delay time6	tfpd3	CL=300pF		500	ns
Input signal rising time	tr_in			150	ns
Input signal falling time	tf_in			150	ns
Output signal rising time	tr_out1	CL=300pF		350	ns
Output signal falling time	tf_out1	CL=300pF		350	ns
Output signal rising time	tr_out2	CL=30pF		150	ns
Output signal falling time	tf_out2	CL=30pF		150	ns

9.0 RELIABILITY TEST

9.1 BOE HYDIS Test condition

The following test is performed with the HV050V01-100 .

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 °C, 240 hrs
2	Low temperature storage test	Ta = -20 °C, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 °C, 80 %RH, 240 hrs
4	High temperature operation test	Ta = 50 °C, 240 hrs
5	Low temperature operation test	Ta = 0 °C, 240 hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (30 min), 100 cycle
7	Vibration test (non-operating)	Frequency : 10 ~ 300 Hz Gravity/AMP : 1.5G Period : X, Y, Z 30 min
8	Shock test (non-operating)	Gravity : 150G Pulse width : 6ms, half sine wave ±X, ±Y, ±Z Once for each direction

*As Guarantee Range of Specific part (Pol. / D-IC / LC), BOEHYDIS have responsibility within this range of these parts.

9.2 Customer Test condition

The following test is performed with the HV050V01-100

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 80 °C, 50%, 240 hrs	
2	Low temperature storage test	Ta = -30 °C, 240 hrs	
3	High temperature & high humidity operation test	Ta = 50 °C, 90 %RH, 240 hrs (Ta = 70 °C, 50 %RH, 24 hrs)	
4	Low temperature operation test	Ta = 0 °C, 240 hrs (Ta = 0 °C, 24 hrs)	
5	Thermal shock	Ta = -54 °C / 85 °C (120 / 120 min), 6 cycle	
6	Vibration test (non-operating)	1st step Frequency : 5 ~ 500 Hz Gravity/AMP : 1 G, 0.5 oct/min Period : Z, 27 min 2nd step Frequency : Max. resonance frequency at 1st step Gravity/AMP : 1 G, 0.5 oct/min Period : X, Y, Z 30 min 3rd step Frequency : Random (5 ~ 500 Hz) Gravity/AMP : 1.06Grms Period : X, Y, Z 30 min 4th step Drop Test : Free fall at 76cm height	

10.0 HANDLING & CAUTIONS

10.1 Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel is made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Put the module display side down on a flat horizontal plane.

10.2 Other cautions

- Do not disassemble and/or re-assemble LCD module.
- When returning the module for repair or etc, please pack the module not to be broken. We recommend using the original shipping packages.

11.0 APPENDIX

11.1 Drive IC detail specification

11.1.1. X-Drive IC Function Description

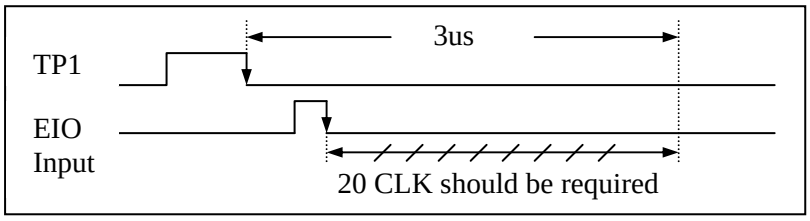
11.1.1.1. Acquisition of image data

EIO2= ”H” is acquired at the first CLK rising edge after EIO2 is biased high. After EIO2 is biased low, acquisition of image data into internal latch begins at the next CLK rising edge. Once all data for 384 outputs are input, device become stand-by automatically and it refrains from acquiring more data despite any CLK inputs until input EIO2 again.

11.1.1.2. Remark for EIO and CLK signal input

(1) EIO must be input only one pulse during 1H period.

(2) CLK must be input more than 20 pulses (on XGA driven by 8 chips) from falling edge of EIO input to 3us after falling edge of TP1.



11.1.1.3.Extend Outputs

Connect the EIO1 pin of previous device to the EIO2 pin of the next device and all input pins except EIO1 and EIO2 are connected commonly by each device.

11.1.1.4.Relationship between the input data and output voltage

Output voltage are defined by the input data value and 10 γ correction voltage(GMA1-10). Supporting dot inversion driving, the polarities of input gray scale voltage of even pins and odd pins that refer to common electrode voltage can be reversed.

(1) γ corrective reference voltage input(GMA1-10)

Should be input externally. Maintain the stable reference voltage during output gray scale voltage. Refer to “Recommended Operating Conditions” for the order of each voltage.

(2) Image signal data mapping

Data format : 6bit x 2RGB

Input width : 36bit (2 pixels data)

MSB LSB

Dx5	Dx4	Dx3	Dx2	Dx1	Dx0

11.1.1.5.Relation between input data and output pins

This relationship is irrespective of L/R condition.

Output	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	. . .	OUT384
Data	D00~D05	D10~D15	D20~D25	D30~D35	D40~D45	D50~D55	. . .	D50~D55

11.1.2. Y-Drive IC operation

The output of LCD control (OUT1 to OUT768) are driven “VCOM” or “VEE” level controlled by the input signals (STV,CPV). The STV data is latched and transferred to OUT1 on the rising edge of CPV, and OUT1 data is shifted to OUT2 and new STV data is also transferred to OUT1 on the next rising edge of CPV. In this way, the data is shifted synchronized to the rising edge of CPV.

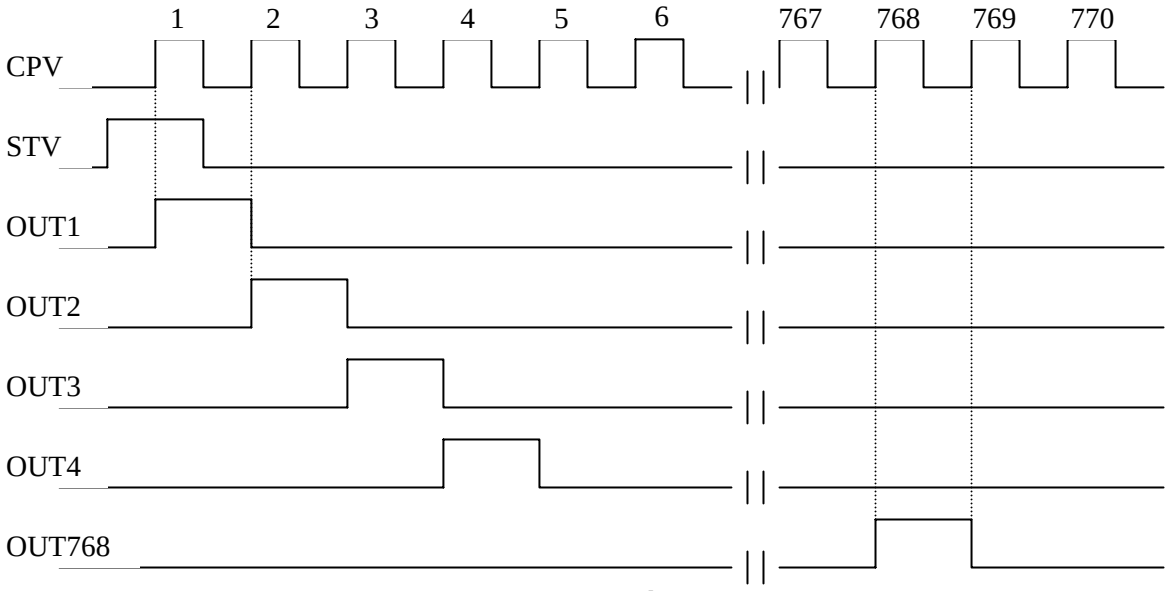
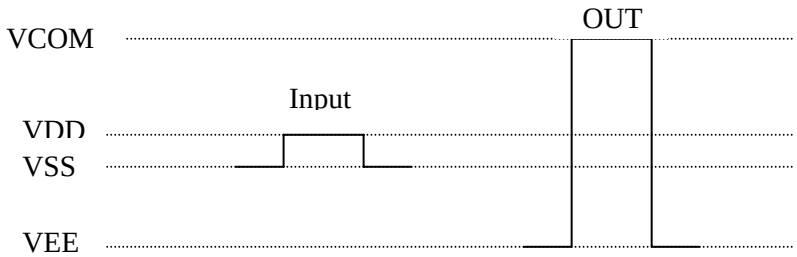


Fig. 5.1.6 Timing Chart

11.1.2.1 LCD control output voltage of Y-Drive IC

The negative voltage output for the liquid crystal control is available.

(Example)



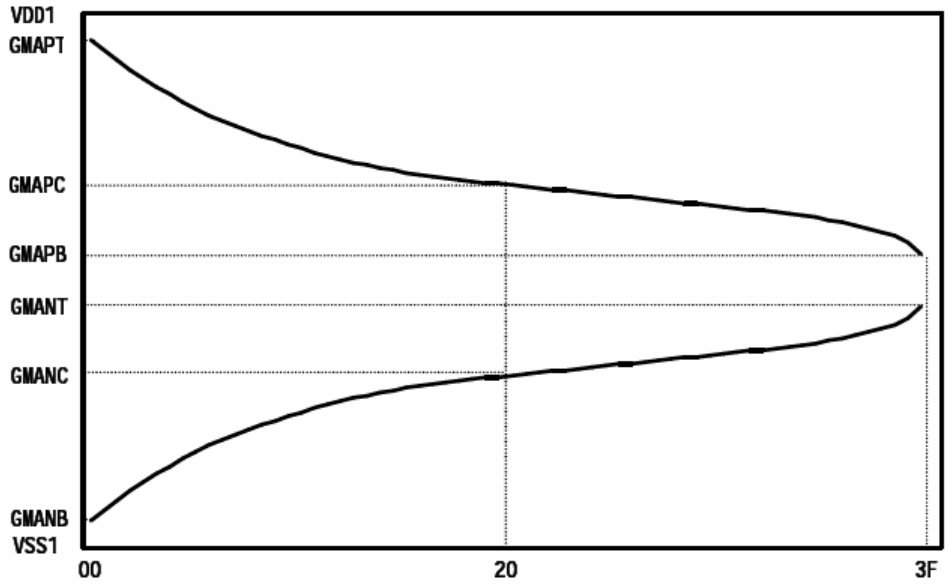
The voltage of input signals (CPV, STV) is VSS(“L”) of VDD(“H”).

The voltage of output signals (OUT1 ~ OUT768) is VEE or VCOM.

11.1.3.Relation between input data and output voltage at X-Drive IC

11.1.3.1. γ correction curve

The relationship between input data and γ voltage is shown in below Figure 9.1.3-1.

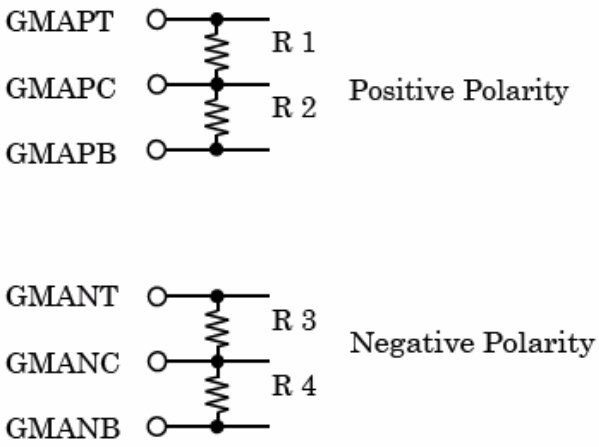


Input Data (HEX)

Figure 9.1.3-1 γ correction Curve

11.1.3.2. GMA resistors

Resistors as specified in below table are connected in series to each γ correction reference power supplies. If γ correction reference power supply of LCD panel matches each resistance ratio, the parts of GMA external power supplies are not required.



Resistor	Ratio
R1	5137
R2	3350
R3	3350
R4	5137

Figure 9.1.3-2 Ladder resistors Connection

Table 9.1.3-1 Resistor Ratio

11.1.3.3. Relation between input data and output voltage

The relationship between input data and output voltage that is converted by GMA voltage is shown in below table. The input data are described in Hexa-decimal.

Data (HEX)	Output Voltage	Data (HEX)	Output Voltage
00	GMAPT	20	GMAPC
01	GMAPC+(GMAPT-GMAPC) x 4634/5137	21	GMAPB+(GMAPC-GMAPB) x 3283/3350
02	GMAPC+(GMAPT-GMAPC) x 4299/5137	22	GMAPB+(GMAPC-GMAPB) x 3216/3350
03	GMAPC+(GMAPT-GMAPC) x 3997/5137	23	GMAPB+(GMAPC-GMAPB) x 3149/3350
04	GMAPC+(GMAPT-GMAPC) x 3729/5137	24	GMAPB+(GMAPC-GMAPB) x 3082/3350
05	GMAPC+(GMAPT-GMAPC) x 3494/5137	25	GMAPB+(GMAPC-GMAPB) x 3015/3350
06	GMAPC+(GMAPT-GMAPC) x 3259/5137	26	GMAPB+(GMAPC-GMAPB) x 2948/3350
07	GMAPC+(GMAPT-GMAPC) x 3024/5137	27	GMAPB+(GMAPC-GMAPB) x 2881/3350
08	GMAPC+(GMAPT-GMAPC) x 2823/5137	28	GMAPB+(GMAPC-GMAPB) x 2814/3350
09	GMAPC+(GMAPT-GMAPC) x 2622/5137	29	GMAPB+(GMAPC-GMAPB) x 2747/3350
0A	GMAPC+(GMAPT-GMAPC) x 2421/5137	2A	GMAPB+(GMAPC-GMAPB) x 2680/3350
0B	GMAPC+(GMAPT-GMAPC) x 2253/5137	2B	GMAPB+(GMAPC-GMAPB) x 2613/3350
0C	GMAPC+(GMAPT-GMAPC) x 2085/5137	2C	GMAPB+(GMAPC-GMAPB) x 2546/3350
0D	GMAPC+(GMAPT-GMAPC) x 1917/5137	2D	GMAPB+(GMAPC-GMAPB) x 2479/3350
0E	GMAPC+(GMAPT-GMAPC) x 1785/5137	2E	GMAPB+(GMAPC-GMAPB) x 2412/3350
0F	GMAPC+(GMAPT-GMAPC) x 1653/5137	2F	GMAPB+(GMAPC-GMAPB) x 2345/3350
10	GMAPC+(GMAPT-GMAPC) x 1521/5137	30	GMAPB+(GMAPC-GMAPB) x 2278/3350
11	GMAPC+(GMAPT-GMAPC) x 1420/5137	31	GMAPB+(GMAPC-GMAPB) x 2211/3350
12	GMAPC+(GMAPT-GMAPC) x 1319/5137	32	GMAPB+(GMAPC-GMAPB) x 2144/3350
13	GMAPC+(GMAPT-GMAPC) x 1218/5137	33	GMAPB+(GMAPC-GMAPB) x 2077/3350
14	GMAPC+(GMAPT-GMAPC) x 1117/5137	34	GMAPB+(GMAPC-GMAPB) x 2010/3350
15	GMAPC+(GMAPT-GMAPC) x 1016/5137	35	GMAPB+(GMAPC-GMAPB) x 1943/3350
16	GMAPC+(GMAPT-GMAPC) x 915/5137	36	GMAPB+(GMAPC-GMAPB) x 1842/3350
17	GMAPC+(GMAPT-GMAPC) x 814/5137	37	GMAPB+(GMAPC-GMAPB) x 1741/3350
18	GMAPC+(GMAPT-GMAPC) x 713/5137	38	GMAPB+(GMAPC-GMAPB) x 1640/3350
19	GMAPC+(GMAPT-GMAPC) x 612/5137	39	GMAPB+(GMAPC-GMAPB) x 1539/3350
1A	GMAPC+(GMAPT-GMAPC) x 511/5137	3A	GMAPB+(GMAPC-GMAPB) x 1438/3350
1B	GMAPC+(GMAPT-GMAPC) x 410/5137	3B	GMAPB+(GMAPC-GMAPB) x 1304/3350
1C	GMAPC+(GMAPT-GMAPC) x 328/5137	3C	GMAPB+(GMAPC-GMAPB) x 1136/3350
1D	GMAPC+(GMAPT-GMAPC) x 246/5137	3D	GMAPB+(GMAPC-GMAPB) x 968/3350
1E	GMAPC+(GMAPT-GMAPC) x 164/5137	3E	GMAPB+(GMAPC-GMAPB) x 599/3350
1F	GMAPC+(GMAPT-GMAPC) x 82/5137	3F	GMAPB

Table . Positive polarity (GMAPT ~ GMAPB)

Data (HEX)	Output Voltage	Data (HEX)	Output Voltage
00	GMANB	20	GMANC
01	GMANB+(GMANC-GMANB) x 503/5137	21	GMANC+(GMANT-GMANC) x 67/3350
02	GMANB+(GMANC-GMANB) x 838/5137	22	GMANC+(GMANT-GMANC) x 134/3350
03	GMANB+(GMANC-GMANB) x 1140/5137	23	GMANC+(GMANT-GMANC) x 201/3350
04	GMANB+(GMANC-GMANB) x 1408/5137	24	GMANC+(GMANT-GMANC) x 268/3350
05	GMANB+(GMANC-GMANB) x 1643/5137	25	GMANC+(GMANT-GMANC) x 335/3350
06	GMANB+(GMANC-GMANB) x 1878/5137	26	GMANC+(GMANT-GMANC) x 402/3350
07	GMANB+(GMANC-GMANB) x 2113/5137	27	GMANC+(GMANT-GMANC) x 469/3350
08	GMANB+(GMANC-GMANB) x 2314/5137	28	GMANC+(GMANT-GMANC) x 536/3350
09	GMANB+(GMANC-GMANB) x 2515/5137	29	GMANC+(GMANT-GMANC) x 603/3350
0A	GMANB+(GMANC-GMANB) x 2716/5137	2A	GMANC+(GMANT-GMANC) x 670/3350
OB	GMANB+(GMANC-GMANB) x 2884/5137	2B	GMANC+(GMANT-GMANC) x 737/3350
OC	GMANB+(GMANC-GMANB) x 3052/5137	2C	GMANC+(GMANT-GMANC) x 804/3350
OD	GMANB+(GMANC-GMANB) x 3220/5137	2D	GMANC+(GMANT-GMANC) x 871/3350
OE	GMANB+(GMANC-GMANB) x 3352/5137	2E	GMANC+(GMANT-GMANC) x 938/3350
OF	GMANB+(GMANC-GMANB) x 3484/5137	2F	GMANC+(GMANT-GMANC) x 1005/3350
10	GMANB+(GMANC-GMANB) x 3616/5137	30	GMANC+(GMANT-GMANC) x 1072/3350
11	GMANB+(GMANC-GMANB) x 3717/5137	31	GMANC+(GMANT-GMANC) x 1139/3350
12	GMANB+(GMANC-GMANB) x 3818/5137	32	GMANC+(GMANT-GMANC) x 1206/3350
13	GMANB+(GMANC-GMANB) x 3919/5137	33	GMANC+(GMANT-GMANC) x 1273/3350
14	GMANB+(GMANC-GMANB) x 4020/5137	34	GMANC+(GMANT-GMANC) x 1340/3350
15	GMANB+(GMANC-GMANB) x 4121/5137	35	GMANC+(GMANT-GMANC) x 1407/3350
16	GMANB+(GMANC-GMANB) x 4222/5137	36	GMANC+(GMANT-GMANC) x 1508/3350
17	GMANB+(GMANC-GMANB) x 4323/5137	37	GMANC+(GMANT-GMANC) x 1609/3350
18	GMANB+(GMANC-GMANB) x 4424/5137	38	GMANC+(GMANT-GMANC) x 1710/3350
19	GMANB+(GMANC-GMANB) x 4525/5137	39	GMANC+(GMANT-GMANC) x 1811/3350
1A	GMANB+(GMANC-GMANB) x 4626/5137	3A	GMANC+(GMANT-GMANC) x 1912/3350
1B	GMANB+(GMANC-GMANB) x 4727/5137	3B	GMANC+(GMANT-GMANC) x 2046/3350
1C	GMANB+(GMANC-GMANB) x 4809/5137	3C	GMANC+(GMANT-GMANC) x 2214/3350
1D	GMANB+(GMANC-GMANB) x 4891/5137	3D	GMANC+(GMANT-GMANC) x 2382/3350
1E	GMANB+(GMANC-GMANB) x 4973/5137	3E	GMANC+(GMANT-GMANC) x 2751/3350
1F	GMANB+(GMANC-GMANB) x 5055/5137	3F	GMANT

Table. Negative polarity (GMANB ~ GMANT)

11.1.4. Electrical Characteristics

Basically, the ground-level voltage is VSS=VSS1=VSS2=GND=0V.

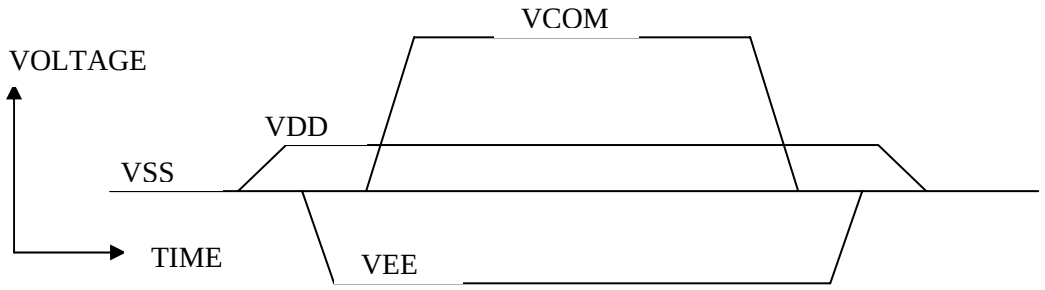
11.1.4.1. Absolute maximum rating over operating free-air temperature (unless otherwise noted)

	Parameter	Applied Port	Rating	Unit
X-Drive IC	Supply Voltage at Logic Port	VDD2	-0.5 to + 5.0	V
	Supply Voltage at Driver Port	VDD1	-0.5 to + 13.5	V
	Input Voltage	GMAPT to GMANB	-0.5 to VDD1 + 0.5	V
		VCOM1,VCOM2		
		Except GMA, VCOM	-0.5 to VDD2 + 0.5	V
	Output Voltage	EIO1, EIO2	-0.5 to VDD2 + 0.5	V
		OUT1 to OUT384	-0.5 to VDD1 + 0.5	V
Y-Drive IC	Power Supply	VDD	-0.3 to + 7.0	V
	Power Supply	VGL	-20 to + 0.3	V
	Power Supply	VGH-VGL	-0.3 to + 40	V
	Power Supply	VDD-VGL	4.5 to 25	V
Storage Temperature (Tstg)			-55 to 125	°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these of any other conditions beyond those indicated under recommended operation conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Keep the power on sequence of VDD2, Control input, VDD1 and GMA1 to GMA10. During power off, this must be reversed.

The order of power on is VDD→VEE→Input signal→VCOM and the order of power off is reverse as shown below figure.



11.1.4.2. Operating condition

	Parameter	Applied Port	Min.	Typ.	Max.	Unit
X-DriveIC	Supply Voltage	VDD1	8.0		12.0	V
	Supply Voltage	VDD2	2.7	3.0	3.6	V
	γ-corrected Supply Voltage	GMAPT ~ GMAPB	1/2VDD1		VDD1-0.2	V
		GMANT ~ GMANB	VSS1+0.2		1/2VDD1	V
	VCOM Input Voltage	VCOM1,VCOM2	VSS1		VDD1	V
	CLK Frequency	CLK	152		160	MHz
	Output Load Capacitance (CL)	OUT1 ~ OUT384			100	pF
Y-DriveIC	Power Supply	VDD	2.5		3.6	V
	Power Supply	VGH	10		28	V
	Power Supply	VGL	-15		-2	V
	Power Supply	VGH-VGL	17		38	V
	Power Supply	VDD-VGL	5		20	V
	Operating Frequency	fCLK			150	kHz
Operating free-air Temperature Range			-30		85	°C

Note : Relation of γ-corrected input voltage

VDD1 > GMAPT ≥ GMPC ≥ GMPB ≥ GMANT ≥ GMANC ≥ GMANB > VSS1

11.1.4.3. DC characteristics of X-Drive IC

Parameter	Applied Port	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage	EIO1,EIO2,XLR, XLR_LV,LP_1/2	VIH1		0.7·VDD2		VDD2	V
Low-level Input Voltage	TP1_1/2,POL_1/2, SQINV,LCH,VLB, VBDATA,TEST1/2	VIL1		0		0.3·VDD2	V
Input Leakage Current	EIO1,EIO2,XLR, XLR_LV,LP_1/2, TP1_1/2,POL_1/2, SQINV,LCH,VLB, VBDATA,TEST1/2, LVCLKA/B, LV0A/B to LV3A/B	IIL		-1		1	μA
mini-LVDS Input Voltage (Center)	LVCLKA/B, LV0A/B to LV3A/B	VI		0.3 +(VID/2)		(VDD2-1.2) -VID/2	V
mini-LVDS Differential Voltage (Amplitude: peak to peak)	LVCLKA/B, LV0A/B to LV3A/B	VID		0.2		0.6	V
Output Current (Note)	OUT1 to OUT384	ICHG	VX=VDD1-0.2 VOUT=VDD1 -0.2V-1.0V		-250	-100	μA
		IDIS	VX=VSS+0.2 VOUT=0.2V +1.0V	200	350		μA
Output Swing Difference Deviation (Note)	OUT1 to OUT384	ΔVO	*1		±20	±35	mV
			*2		±16	±25	
			*3		±5	±10	
Averaged Output Voltage Deviation	OUT1 to OUT384	ΔVA	*4		±5	±10	mV
Ladder Resistance	GMAPT-GMAPB GMANT-GMANB	RGMA		7900	15850	23800	Ω
Output Voltage Range	OUT1 to OUT384	VOUT		VSS1+0.2		VDD1-0.2	V
Driver Port Dynamic Current Consumption (Note)	VDD1-VSS1	Didd1	Raster pattern VDD1=12.0V 1H=10μs *5 No Load		12	16	mA
Driver Port Static Current Consumption (Note)	VDD1-VSS1	Sidd1	Raster pattern VDD1=12.0V No Load		10	14	mA
Logic Port Dynamic Current Consumption (Note)	VDD2-VSS2	Didd2	1H=10μs *5 fCLK=152MHz Checkered		18	22	mA
Logic Port Static Current Consumption (Note)	VDD2-VSS2	Sidd2	No Clock&Input After data Sampling		0.3	0.6	mA

<Note>

Conditions *1 : Vout=VDD1-0.2V to VDD1-0.9V, VSS+0.2V to VSS+0.9V
*2 : Vout=VDD1-0.9V to VDD1-2.5V, VSS+0.9V to VSS+2.5V
*3 : Vout=VDD1-2.5V to VSS+2.5V
*4 : Vout=VDD1-0.2V to VSS+0.2V
*5 : "1H" means one horizontal period.

* Input the same value to all pairs of mini-LVDS input and mini-LVDS differential voltage ports.

11.1.4.4. DC characteristics of Y-Drive IC

ITEM	SYMBOL	CONDITIONS	RATINGS			UNIT	PINS
			MIN.	TYP.	MAX.		
'0' input voltage	VIL		VSS		0.2×VDD	V	All inputs
'1' input voltage	VIH		0.65×VDD		VDD	V	All inputs
'0' output voltage(1)	VOL	IOL=40μA	VSS		VSS+0.1	V	DIO1,2
'1' output voltage(2)	VOH	IOH= 0μA	VDD-0.1		VDD	V	DIO1,2
'0' output resistance	ROL	VOUT= VGL+0.5V			95	Ω	OUT1~ OUT240
'1' output resistance	ROH	VOUT= VGH-0.5V			110	Ω	OUT1~ OUT240
'0' output resistance deviation	dROL	(MAX-MIN) /AVG	-10		10	%	OUT1~ OUT240
'1' output resistance deviation	dROH	(MAX-MIN) /AVG	-10		10	%	OUT1~ OUT240
input current	IIL		-5.0		+5.0	μA	All inputs
current consumption(1)	IDD	(Note1)			100	μA	VDD
current consumption(2)	IGH	(Note1)			500	μA	VGH

Figure 1. Measurement Set Up

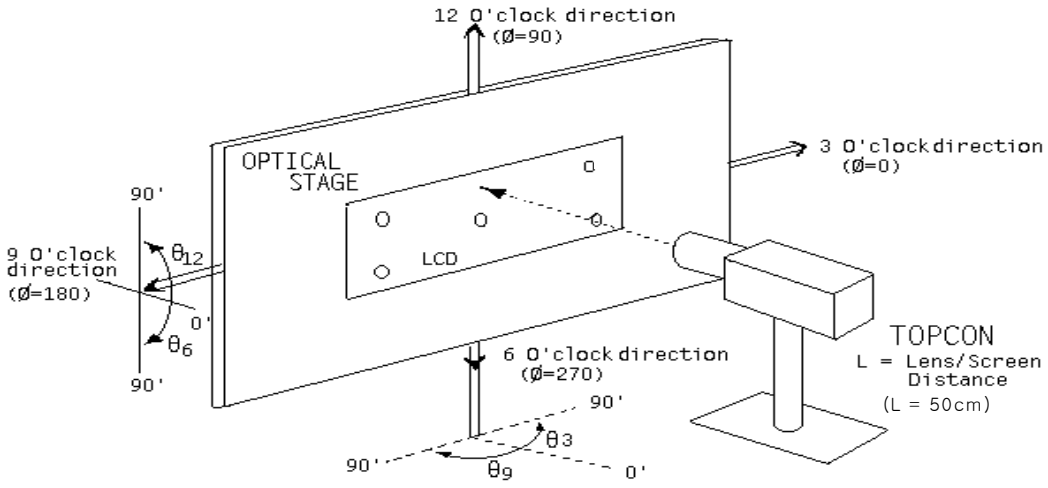


Figure 2. Response Time Testing

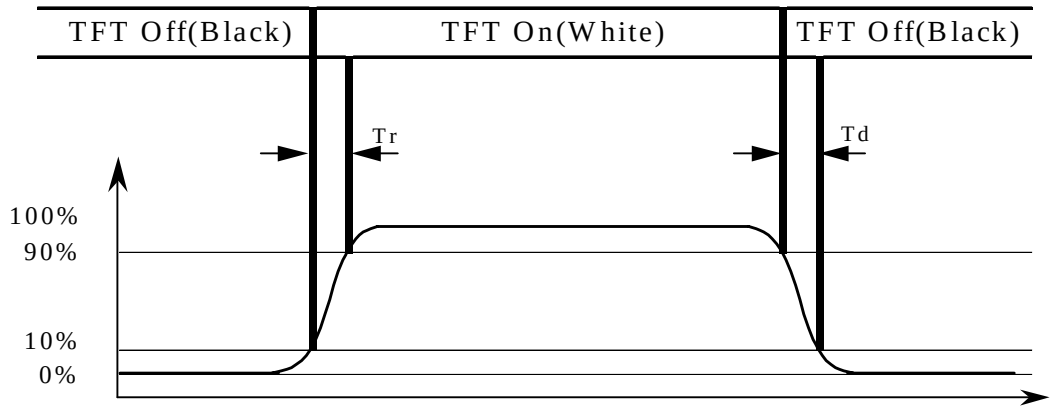
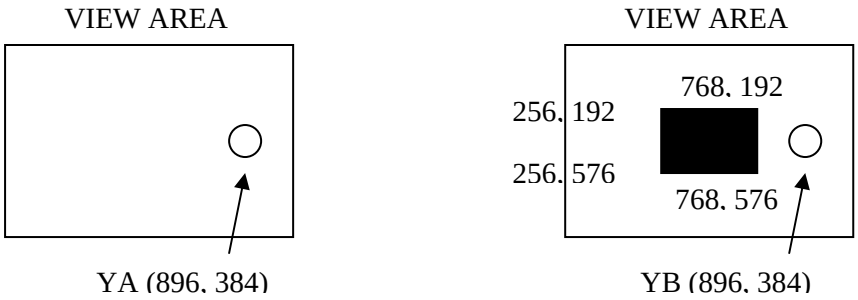


Figure 3. Cross Modulation Test Description



$$\text{Cross-Talk} = \left| \frac{YB - YA}{YA} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns.

Figure 4. Packing Sequence of HV050V01-100

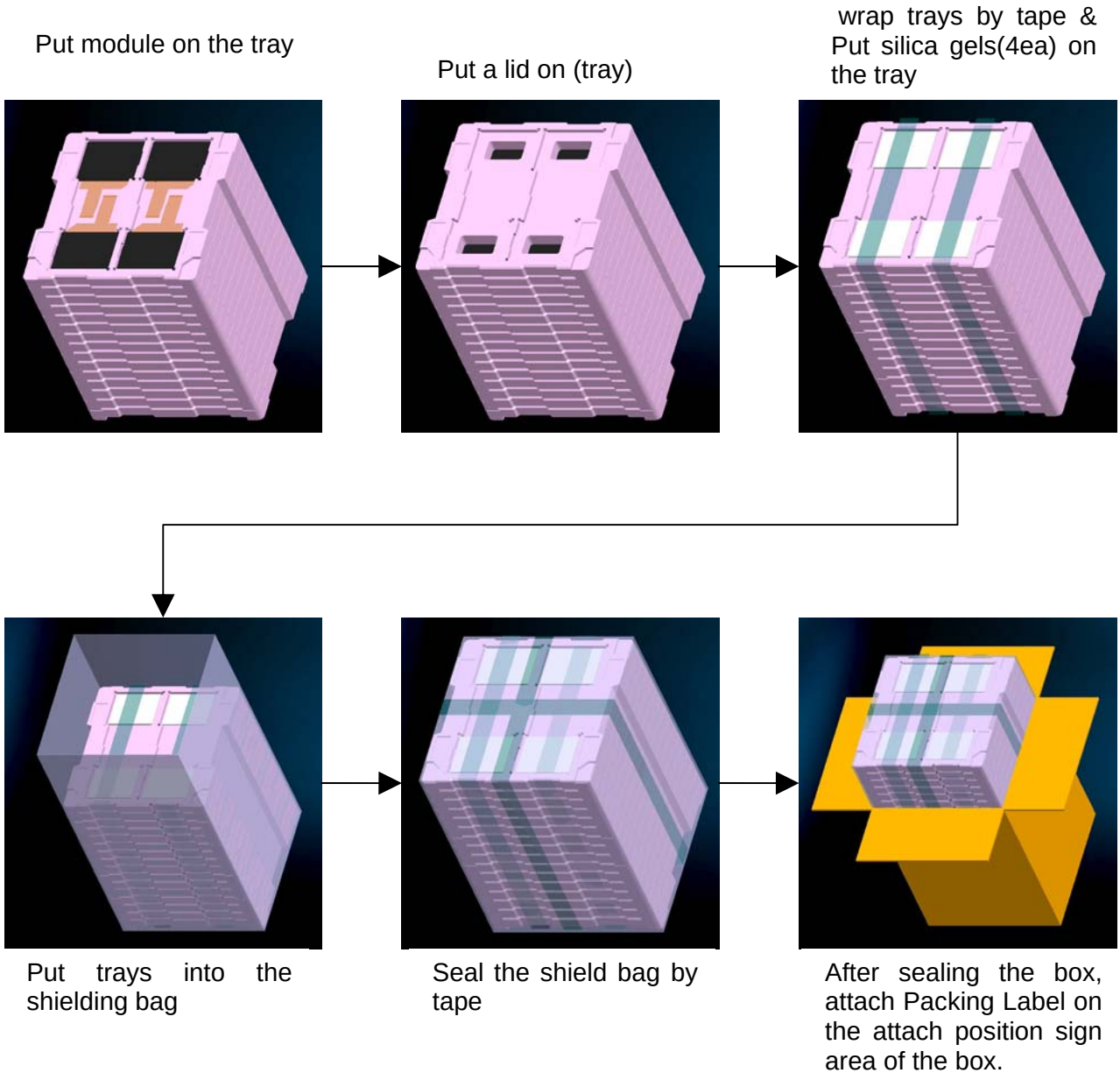
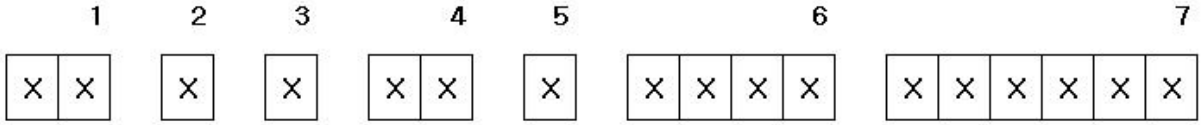


Figure 5. Product Serial Number



Type

No 1. Control

No 2. Rank

No 3. Line Classification(BOE HYDIS : H, LCM : L, BOE OT : A/B/C)

No 4. Year(2001 : 01, 2002 : 02,…)

No 5. Month(1, 2, 3, …,9 X, Y, Z)

No 6. FG Code

No 7. Serial No.

*. Packing Note

- Box Dimension: 333mm(W)X 333mm(D)X 435(H)
- Package Quantity in one Box: 60pcs
- Total weight : 4.8kg

Figure 6. Box Label

- Label Size: 108 mm (L) × 56 mm (W)
- Contents
  Model: HV050V01-100
  Q`ty: Module Q`ty in one box
  Serial No.: Box Serial No. See next page for detail description.
  Date: Packing Date
  FG Code: FG Code of Product

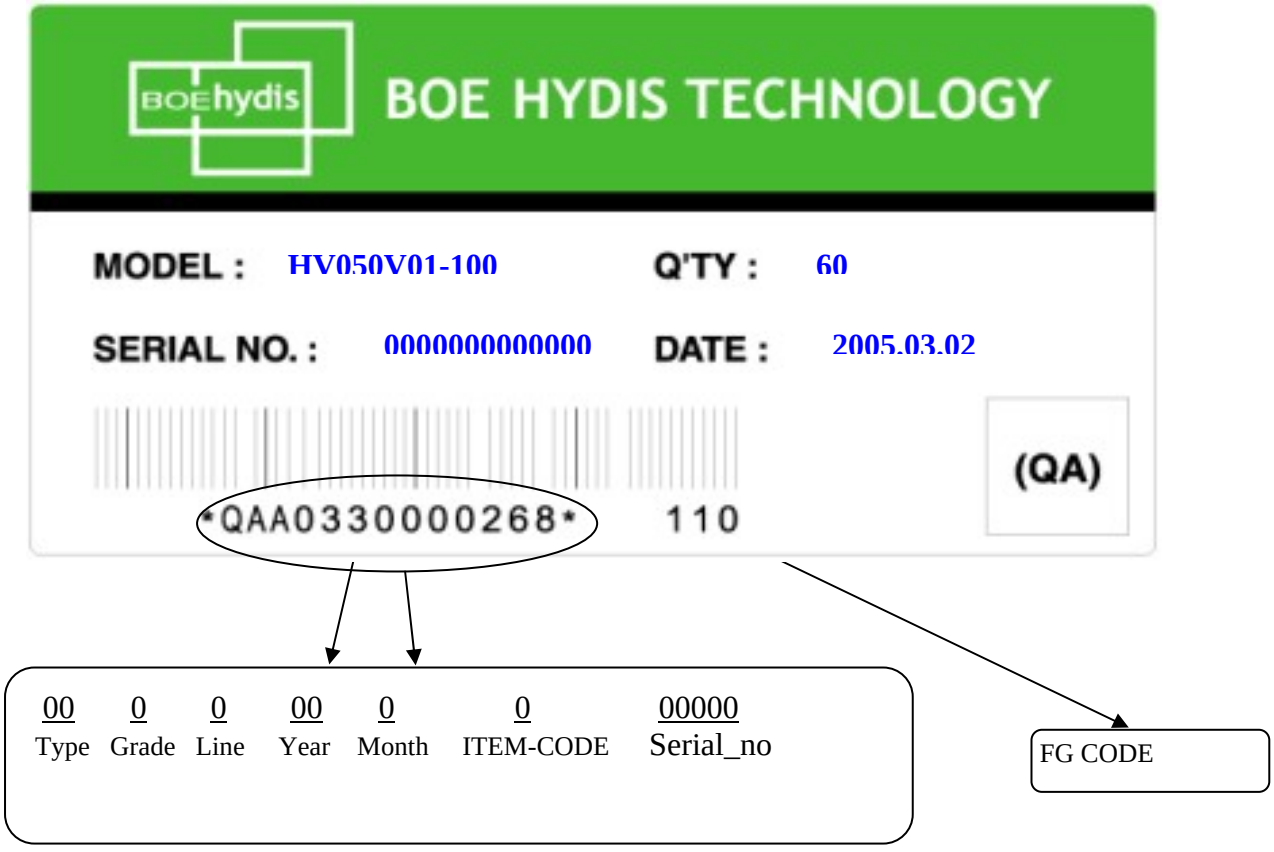


Figure 7. TFT-LCD Panel Outline Dimension