USB Type-C and PD Source Controller

Hynetek Semiconductor Co., Ltd.

HUSB361

FEATURES

- USB Type-C 2.1 and USB PD3.1 source Compliance certified, TID: 5547
  - Support 5 FPDOs with programmable voltage and current
  - Support 2 APDOs with programmable voltage and current
- Support BC1.2 DCP and HVDCP protocols
  - BC1.2 DCP mode
  - Divider3 mode
  - QC2.0/3.0 Class A
  - AFC, FCP and SCP
- Support driving external N-MOSFET or P-MOSFET
- Support constant voltage (CV) loop and constant current(CC) loop
- Accurate constant power limit
- Additional 7 power levels are configured by PS0 and PS1 pins
- Integrated OVP, UVP, UVLO, OCP, FOCP and TSD protections
- Small packages: QFN3x3-16L, QFN4x4-16L and SSOP-10L
- ±5 kV HBM ESD rating for all pins

APPLICATIONS

AC-DC power adaptor

Car charger

GENERAL DESCRIPTION

The HUSB361 is a high performance, high integration USB Type-C Power Delivery Source Controller.

The HUSB361 supports PD2.0, PD3.0, PPS, QC2.0/3.0, Divider3, BC1.2 DCP, AFC, FCP and SCP protocols. It supports up to 5 FPDOs with programmable voltage and current and 2 APDOs which are fully compliant with USB Power Delivery Specification Revision 3.1, version 1.0.

The HUSB361 integrates all of required protections such as Over Voltage Protection (OVP), Under Voltage Protection (UVP), Under Voltage Lock Out (UVLO), Over Current Protection (OCP), Fast Over Current Protection (FOCP) and Thermal Shut Down (TSD).

It is available in SSOP-10L, QFN-16L, 3 mm x 3 mm and QFN-16L, 4 mm x 4 mm packages.

TYPICAL APPLICATION CIRCUIT

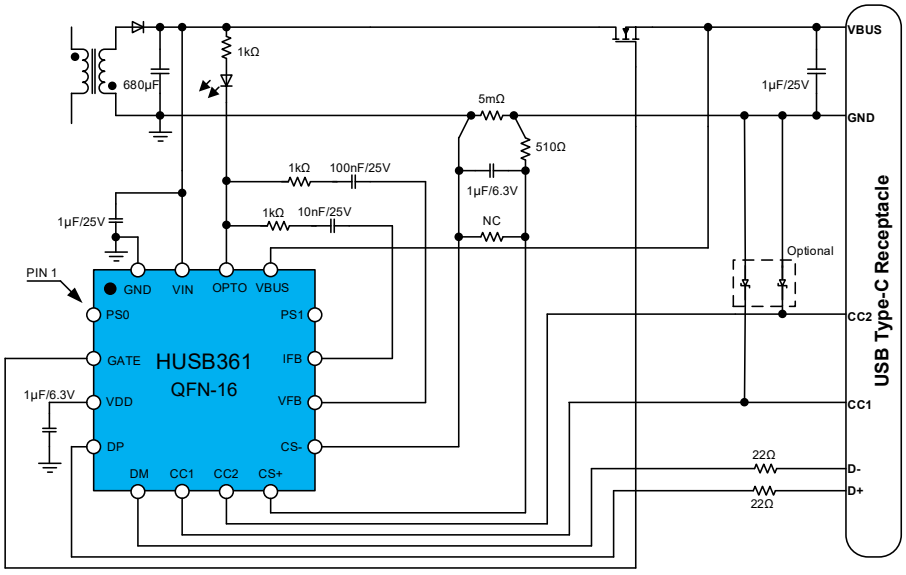

Figure 1. Typical Application Circuit

Rev. 1.1

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	01/2023	Initial version
Rev. 1.1	08/2023	Update package marking

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

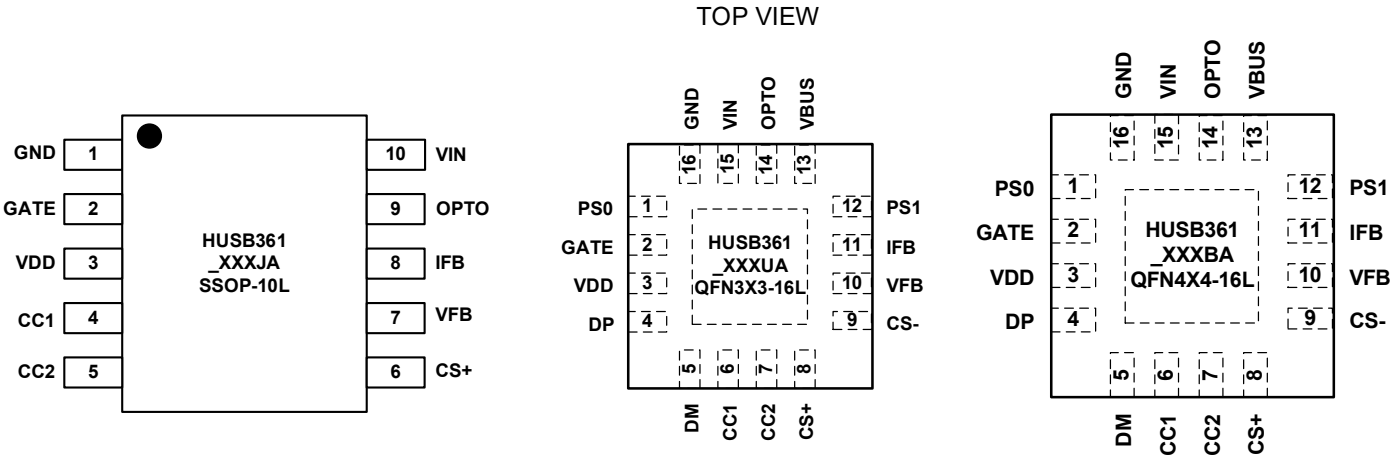


Figure 2. Pin Configuration (Top View)

Table 1. HUSB361_XXXJA Pin Function Descriptions

Pin No.	Pin Name	Type[1]	Description
1	GND	P	Power ground.
2	GATE	AO	N-MOSFET Gate driver output for VBUS load switch.
3	VDD	P	Internal 3.3 V regulator output for system power.
4	CC1	AIO	USB Type-C CC1 line.
5	CC2	AIO	USB Type-C CC2 line.
6	CS+	AI	Positive input of the current sense amplifier.
7	VFB	AI	Feedback point of constant voltage (CV) loop, connect CV compensation network to this pin.
8	IFB	AI	Feedback point of constant current (CC) loop, connect CC compensation network to this pin.
9	OPTO	AI	OPTO driver.
10	VIN	P	Supply voltage input. Connect this pin to GND via a recommended 1 μF ceramic capacitor.

Table 2. HUSB361_XXXUA, HUSB361_XXXBA Pin Function Descriptions

Pin No.	Pin Name	Type	Description
1	PS0	AI	Power selection input 0. Connect to ground or VDD, or keep floating can determine the output power level, combined with PS1 pin.
2	GATE	AO	N-MOSFET Gate driver output for VBUS load switch.
3	VDD	P	Internal 3.3V regulator output for system power.
4	DP	DIO	USB DP line.
5	DM	DIO	USB DM line.
6	CC1	AIO	USB Type-C CC1 line.
7	CC2	AIO	USB Type-C CC2 line.
8	CS+	AI	Positive input of the current sense amplifier.
9	CS−	AI	Negative input of the current sense amplifier.
10	VFB	AI	Feedback point of constant voltage (CV) loop, connect CV compensation network to this pin.
11	IFB	AI	Feedback point of constant current (CC) loop, connect CC compensation network to this pin.
12	PS1	AI	Power selection input 1. Connect to ground or VDD, or keep floating can determine the output power level, combined with PS0 pin.
13	VBUS	AI	VBUS sense and discharge pin.

Pin No.	Pin Name	Type	Description
14	OPTO	AI	OPTO driver.
15	VIN	P	Supply voltage input. Connect this pin to GND via a recommended 1 μF ceramic capacitor.
16	GND	P	Power ground.
-	PAD	P	QFN package pad. It is recommended to connect this pin to GND.

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameter	Rating
VIN Input Voltage	3.15 V to 22.05 V
Operating Temperature Range (Junction) (T_J)	−40 °C to 125 °C
Ambient Temperature Range (T_A)	−40 °C to 105 °C

SPECIFICATIONS

V_{IN} = 5 V, T_A = 25 °C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage	V_{IN}		3.15		22.05	V
Supply Voltage UVLO Threshold	V_{IN_UVLO}	Rising edge		3.1		V
Supply Voltage UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$			150		mV
Supply Current	I_{CC}	CC is attached with a R_d, normal operation		2.6		mA
Quiescent Current	I_Q	CC1 and CC2 pins are floating		550		µA
VDD						
Internal Regulator Output	V_{DD}			3.3		V
Type-C						
1.5 A Mode Pull-Up Current Source	I_{RP_1P5}		165.6	180	194.4	µA
3.0 A Mode Pull-Up Current Source	I_{RP_3P0}		303.6	330	356.4	µA
UFP Detection Threshold at 1.5A Current	$vR_{d\_OPEN\_1.5A}$			1.6		V
UFP Detection Threshold at 3.0A Current	$vR_{d\_OPEN\_3A}$			2.6		V
BMC COMMAN PARAMETERS						
Bit Rate	$f_{BitRate}$		270	300	330	kbps
BMC Tx PARAMETERS						
Falling Time	t_{Fall}	10% and 90% amplitude points, unloaded condition	300			ns
Rising Time	t_{Rise}	10% and 90% amplitude points, unloaded condition	300			ns
Voltage Swing	V_{Swing}	CC pull down resistor > 800Ω	1.05	1.125	1.2	V
Transmitter Low Voltage	V_{Low}	CC pull down resistor > 800Ω	-75		75	mV
Transmitter Output Impedance	Z_{Driver}	Source output impedance at 750kHz with CC attached	35	55	75	Ω
BMC Rx PARAMETERS						
Rx Bandwidth Limiting Filter	$t_{RXFilter}$	Time constant of a single pole filter	100			ns
Receiver Input Impedance	Z_{BMC_RX}		1			MΩ
BC1.2 DCP MODE						
DP and DM Shorting Resistance	R_{DPM_SHORT}	V_{DP} = 0.6 V		30		Ω
DP Leakage Resistance	R_{DP_LKG}	V_{DP} = 0.6 V		800		kΩ
DM Leakage Resistance	R_{DM_LKG}	V_{DM} = 0.6 V		800		kΩ

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIVIDER3 MODE						
DP Output Voltage	V_{DP_APP}	V_{IN} = 5 V		2.7		V
DM Output Voltage	V_{DM_APP}	V_{IN} = 5 V		2.7		V
DP Output Impedance	R_{DP_PAD}	I_{DP} = −5 μA		30		kΩ
DM Output Impedance	R_{DM_PAD}	I_{DM} = −5 μA		30		kΩ
HVDCP MODE						
Output Voltage Selection Reference	V_{SEL_REF}			2.0		V
Data Detect Voltage	V_{DAT_REF}			0.325		V
DP High Glitch Filter Time	$T_{GLITCH\_BC\_MODE}$		1	1.25	1.5	s
DM Low Glitch Filter Time	$T_{GLITCH\_DM\_LOW}$		1	2		ms
Output Voltage Glitch Filter Time	$T_{GLITCH\_V\_CHANGE}$		20	40	60	ms
DM Pull-Down Resistance	R_{DM_DWM}			15		kΩ
QC MODE						
Pulse Glitch Filter Time	$T_{GLITCH\_CONT\_CHANGE}$	For QC3.0 in continues mode	100	150	200	μs
FCP MODE						
DM FCP TX Valid Output High	V_{TX_VOH}		2.55		3.6	V
DM FCP TX Valid Output Low	V_{TX_VOL}				0.3	V
DM FCP RX Valid Input High	V_{RX_VIH}		1.4		3.6	V
DM FCP RX Valid Input Low	V_{RX_VIL}				1	V
DM Output Pull-Low Resistance	R_{DPL}			500		Ω
Unit Interval for FCP	UI			160		μs
VOLTAGE CONTROL (VFB PIN)						
Voltage Sense Scaling Factor				10		
VIN Step LSB				20		mV
Default Voltage	V_{IN_DEF}	CC is unattached. Default setting.		5.12		V
VIN Regulation Accuracy		V_{IN}=3.15 V to 22.05 V		±1.5		%
CURRENT CONTROL (CS+, CS−, IFB PINs)						
Current Sense Resistor				5		mΩ
GATE PIN						
Driver Voltage		Refer to V_{IN}		5		V
Sourcing Current		EN_GATE = 1		20		μA
Pull Down Resistance		GATE transition from ON to OFF		200		Ω
OPTO PIN						
Minimum OPTO Current				30		μA
Maximum Pull Down Current				3		mA
OVER VOLTAGE PROTECTION						
OVP Protection Threshold	V_{IN_OV}	Reference to internal V_{IN} reference, no offset voltage applied. Default setting	115	120	125	%
OVP De-bounce Time	t_{OVP_DEB}			10		μs
UNDER VOLTAGE PROTECTION						
UVP Protection Threshold	V_{IN_UV}	Reference to internal V_{IN} reference	75	80	85	%
UVP De-bounce Time	t_{UVP_DEB}			1		ms
OVER CURRENT PROTECTION						

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OCP Protection Threshold	I_{IN_OC}	Reference to internal I_{IN} reference. Default setting. Nominal output current=3 A		120		%
OCP De-bounce Time	t_{OC_DEB}			2.5		ms
FOCP Protection Threshold	I_{IN_FOCP}			6		A
THERMAL SHUT DOWN						
Thermal Shut Down Threshold	T_{TSD}			140		ºC
Thermal Shut Down Hysteresis	T_{TSD_HYS}			20		ºC

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VIN, VBUS, GATE	−0.3 V to 30 V
OPTO, CC1, CC2	−0.3 V to 24 V
VDD, DP, DM, CS+, CS−, VFB, IFB, PS0, PS1	−0.3 V to 7 V
Operating Temperature Range (Junction) (T_J)	−40°C to 125°C
Soldering Conditions	JEDEC J-STD-020
Soldering Reflow Peak Temperature	260°C
Electrostatic Discharge (ESD)	
Human Body Model (VBUS)	±5000 V
Human Body Model (OTHER PINS)	±6000 V
Charged Device Model(CDM)(QFN)	±1000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN-16L, 3 mm x 3 mm	77	38	°C/W
QFN-16L, 4 mm x 4 mm	47	22	°C/W
SSOP-10L	88	38	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

VIN PIN

VIN pin is the power supply input, which is derived from the output of the AC-DC or DC-DC converter. Connect a 1 μF decoupling MLCC between VIN pin and GND pin.

The VIN pin is also connected to an internal MOSFET and discharge resistor, which is used as a bleeder to help discharge the energy stored in the output capacitor. With this bleeder, VIN can be regulated to vSafe5V upon the detachment of a connected device, or to a lower desired output voltage level upon a request command received from the Sink, such as from 20 V to 5 V.

VDD PIN

An internal liner regulator is used to provide 3.3 V for internal circuits. Connect a 1 μF MLCC to VDD pin for decoupling.

CONTROL LOOP COMPENSATION CIRCUIT (VFB, CS+, CS−, IFB, OPTO PINS)

In the HUSB361, the constant voltage(CV) loop compensation and constant current(CC) loop compensation are implemented. VIN voltage is scaled by a resistor divider to be as the feedback voltage. It is compared with the internal voltage reference to generate an error signal. The CV loop can compensate this error signal. And then the compensated signal is employed to drive the primary side of the opto-coupler and control the AC-DC power loop.

SLEW RATE CONTROL

The HUSB361 implements multiple fixed voltage slew rates, which are 250 mV/ms, 167 mV/ms, 100 mV/ms and 83 mV/ms. The default setting is 83 mV/ms.

IR COMPENSATION

IR compensation is only available when VIN is set to 5 V. If PPS is available in any power level, IR compensation will be disabled even if 5 V APDO is selected. There are 4 IR compensation options, 0 mV/A, 50 mV/A, 100 mV/A and 150 mV/A. The default IR compensation is 100 mV/A.

For example, if 100 mV/A IR compensation is selected, then for the 5 V/3 A condition (except 5 V APDO), the actual VIN voltage is:

$$5\ V + 3\ A \times 100\ mV/A = 5.3\ V$$

CURRENT SENSE RESISTOR

The recommended current sense resistor is 5 mΩ. The sensed current information is employed to perform OCP, FOCP and constant current(CC) control.

CC1 AND CC2 PINS

CC1 and CC2 pins are used to detect Type-C connection, BMC communication.

TYPE-C CC FUNCTION

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

The HUSB361 monitors the status of CC1 and CC2 pins and decide which state the HUSB361 should enter.

CC1 and CC2 are configured as Source only mode with 1.5 A and 3 A current advertising. The default R_p current on CC1 and CC2 is I_{CC_3P0}, which means 3 A current advertising.

The CC1 and CC2 can tolerance a voltage up to 24 V. This is helpful for the HUSB361 to survive in the failure when the CC1 or CC2 is shorted to the VBUS pin.

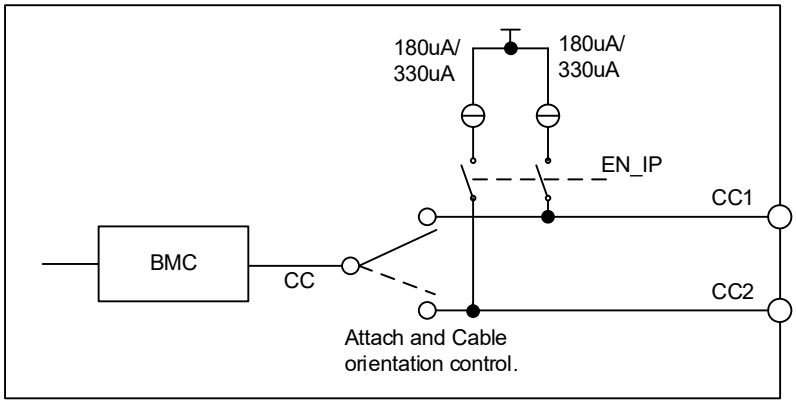


Figure 3. CCx Hardware Diagram

BMC DRIVER

Through the Type-C detection, one of the CC pins will be connected to the internal BMC block to achieve PD communication.

VBUS PIN

This pin is used to sense VBUS presence and discharge VBUS voltage on USB Type-C receptacle side.

VSAFE0V DETECTION

When the HUSB361 is attached with a Sink, it detects whether the VBUS voltage is within vSafe0V. If yes, the HUSB361 enters Attached.SRC state. If no, it will stay at AttachWait.SRC state.

VBUS DISCHARGE

The VBUS pin is also connected to an internal MOSFET and discharging circuitry, which is used as a bleeder to help dissipate the energy stored in the VBUS capacitor. With this bleeder, VBUS is discharged to vSafe0V upon the detachment of a connected device, or to a lower desired output voltage level upon a request command received from the Sink, such as from 20 V to 5 V.

GATE PIN

The GATE pin of the HUSB361 is designed to drive an external N-MOSFET or a P-MOSFET (N-MOSFET in default, for P-MOSFET configuration, please contact Hynetek). When the HUSB361 is attached and is ready to enable VBUS. The GATE pin outputs a voltage to turn on the external N-MOSFET. The turn on time of the external N-MOSFET may be impacted by the external N-MOSFET's characteristics. For P-MOSFET, the GATE pin is pulled down to enable VBUS.

POWER SELECTION

The HUSB361 has multiple power configurations by the connection of PS0 and PS1 pins. When PS0 and PS1 pins are floating, the HUSB361 performs default power configuration. For HUSB361_001XX, the default power configuration is 65 W (as shown in Table 7) while for HUSB361_102XX, it is 35 W, as shown in Table 8.

Table 7. HUSB361_001UA, HUSB361_001BA and HUSB361_001JA Default Power Configurations

Power Parameters	Note
FPDO1	5 V3 A
FPDO2	9 V3 A
FPDO3	12 V3 A
FPDO4	15 V3 A
FPDO5	20 V3.25 A
APDO1	NA
APDO2	NA
IR Comp@5 V	100 mV/A
OCP Rating	120%
OVP Rating	120%

Power Parameters	Note
DPDM Modes	QC2.0/3.0, Divider3, BC1.2 DCP, AFC, FCP and SCP

Table 8. HUSB361_102UA and HUSB361_102BA Default Power Configurations

Power Parameters	Note
FPDO1	5 V3 A
FPDO2	9 V3 A
FPDO3	12 V2.91 A
FPDO4	15 V2.33 A
FPDO5	20 V1.75 A
APDO1	3.3 V-11 V/3 A
APDO2	3.3 V-16 V/2 A
IR Comp@5 V	100 mV/ A
OCP Rating	120%
OVP Rating	120%
DPDM Modes	QC2.0/3.0, Divider3, BC1.2 DCP, AFC, FCP and SCP

Besides, the source output power can be set into different power levels and different PDP options through different combination of the configurations of the PS0 and PS1 pins, as shown in Table 9 and Table 10.

Table 9. HUSB361_001UA, HUSB361_001BA and HUSB361_001JA Power Configurations

PS0	PS1	Source Power Level
Floating	Floating	Refer to Table 7
Floating	GND	18 W (5 V/3 A, 9 V/2 A, 12 V/1.5 A)
Floating	VDD	20 W (5 V/3 A, 9 V/2.22 A)
GND	Floating	20 W (5 V/3 A, 9 V/2.22 A, 12 V/1.66 A)
GND	GND	25 W (5 V/3 A, 9 V/2.77 A)
GND	VDD	27 W (5 V/3 A, 9 V/3 A)
VDD	Floating	30 W (5 V/3 A, 9 V/3 A, 12 V/2.5 A, 15 V/2 A, 20 V/1.5 A)
VDD	GND	45 W (5 V/3 A, 9 V/3 A, 12 V/3 A, 15 V/3 A, 20 V/2.25 A)
VDD	VDD	60 W (5 V/3 A, 9 V/3 A, 12 V/3 A, 15 V/3 A, 20 V/3 A)

Table 10. HUSB361_102UA and HUSB361_102BA Power Configurations

PS0	PS1	Source Power Level
Floating	Floating	Refer to Table 8
Floating	GND	18 W (5 V/3 A, 9 V/2 A, 12 V/1.5 A, 3.3 V-5.9 V/3 A, 3.3 V-11 V/2 A)
Floating	VDD	20 W (5 V/3 A, 9 V/2.22 A, 3.3 V-5.9 V/3 A, 3.3 V-11 V/2.2 A)
GND	Floating	20 W (5 V/3 A, 9 V/2.22 A, 12 V/1.66 A, 3.3 V-5.9 V/3 A, 3.3 V-11 V/2.2 A)
GND	GND	25 W (5 V/3 A, 9 V/2.77 A, 3.3 V-5.9 V/3 A, 3.3 V-11 V/2.75 A)
GND	VDD	30 W (5 V/3 A, 9 V/3 A, 3.3 V-11 V/3 A, 3.3 V-16 V/2 A)
VDD	Floating	30 W (5 V/3 A, 9 V/3 A, 12 V/2.5 A, 15 V/2 A, 20 V/1.5 A, 3.3 V-11 V/3 A, 3.3 V-16 V/2 A)
VDD	GND	45 W (5 V/3 A, 9 V/3 A, 12 V/3 A, 15 V/3 A, 20 V/2.25 A, 3.3 V-16 V/3 A, 3.3 V-21 V/2.25 A)
VDD	VDD	60 W (5 V/3 A, 9 V/3 A, 12 V/3 A, 15 V/3 A, 20 V/3 A, 3.3 V-21 V/3 A)

OVER VOLTAGE PROTECTION

The HUSB361 detects the VIN pin voltage to achieve over-voltage protection function. The threshold to trigger over-voltage protection is 120% of the VIN_REF. When the over-voltage condition occurs, the HUSB361 disables the GATE pin. When the over-voltage condition is removed, the HUSB361 is reset to default mode and will automatic recover again.

UNDER VOLTAGE PROTECTION

The HUSB361 detects the VIN pin voltage to achieve under-voltage protection function. The threshold to trigger under-voltage protection is 80% of the VIN_REF. When the under-voltage condition occurs, the HUSB361 disables

the GATE pin. When the under-voltage condition is removed, the HUSB361 is reset to default mode and will automatic recover again.

OVER CURRENT PROTECTION

When the current sensed by the sense resistor exceeds the 120% of IIN_REF, the over-current protection takes action and the GATE is also disabled. When the over-current condition is removed, the HUSB361 is reset to default mode and will automatic recover again.

FAST OVER CURRENT PROTECTION

The HUSB361 integrates FOCP protection function. When the VBUS is hard shorted to GND by fault, the output current increases sharply. When the output current reaches the FOCP threshold, the protection circuit takes action and turns off the external load switch. When the short condition is removed, the HUSB361 is reset to default mode and will automatic recover again.

THERMAL SHUT DOWN

When the junction temperature rises across T_{TSD}, thermal shut down takes action and the GATE is disabled. When the junction temperature falls across $T_{TSDM}T_{TSD\_HYS}$, the HUSB361 is reset to default mode and will automatic recover again.

CHARGING PROTOCOLS AUTO SELECTION (DP AND DM PIN)

The HUSB361 supports various fast charging protocols including BC1.2 DCP, Divider3, QC 2.0/3.0 Class A, AFC, FCP and SCP. According to the different status of DP and DM pins, the HUSB361 recognizes the attached sink and apply the fast charging protocol automatically.

DPDM_APP MODE

The DPDM_APP mode is the mode that the HUSB361 supports the Divider3 charging protocol. In the DPDM_APP mode, the HUSB361 outputs 2.7 V DC voltage on both DP and DM pins. The 2.7 V can be pulled down by the attached Sink. If DP or DM pin is pulled down below V_{SEL_REF}, the HUSB361 exits the DPDM_APP mode and enters into DPDM_DCP mode.

DPDM_DCP MODE

The DPDM_DCP mode is the mode that the HUSB361 supports BC1.2 DCP protocol. The 2.7 V DC sources are removed and the DP and DM pins are shorted through R_{DPM_SHORT} resistor. It is possible for the attached sink to start primary, secondary and HVDCP detection processes when the HUSB361 is in DPDM_DCP mode.

DPDM_HVDCP MODE

After successful detection of the DCP, the HUSB361 notify the sink that the HUSB361 enters into HVDCP mode.

In the HVDCP mode, the HUSB361 monitors the status of DP and DM pins and enters into different modes depending on the status of DP and DM pins.

TYPICAL APPLICATION CIRCUITS

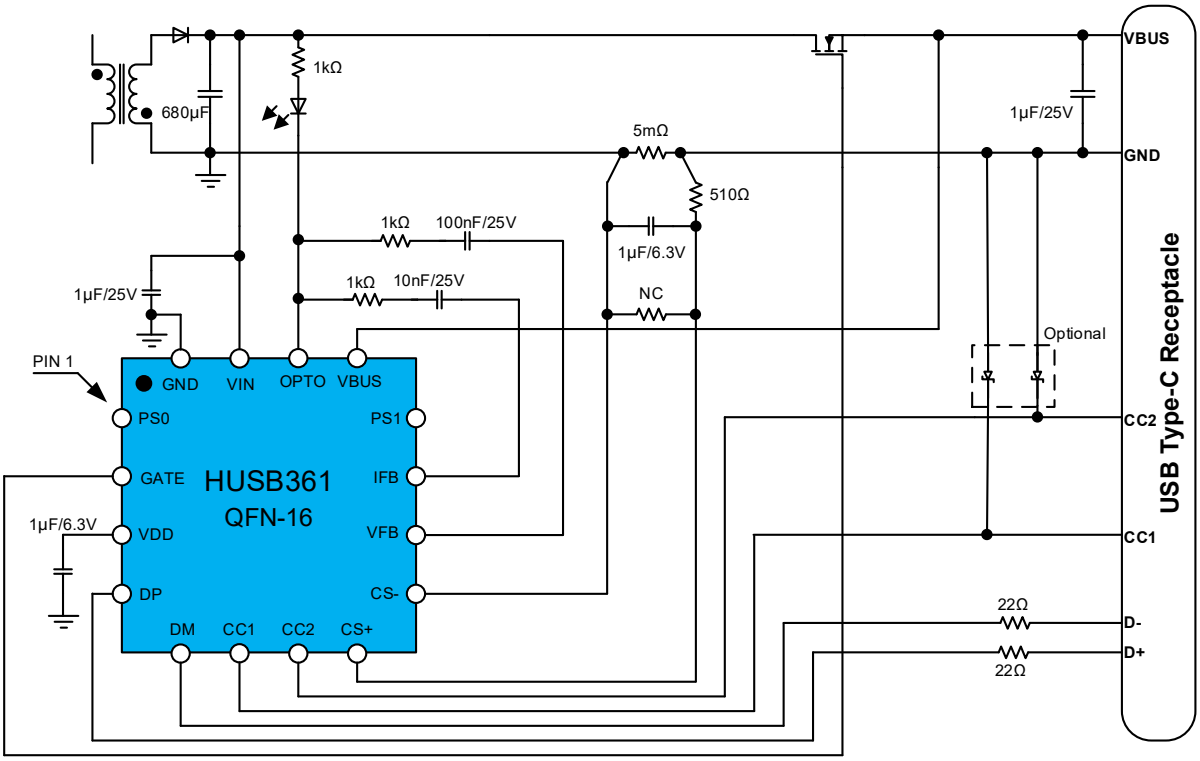


Figure 4. USB PD Source with HVDCP Protocol Supported Application Diagram(QFN-16L Package, 4 mm x 4 mm and 3 mm x 3 mm)

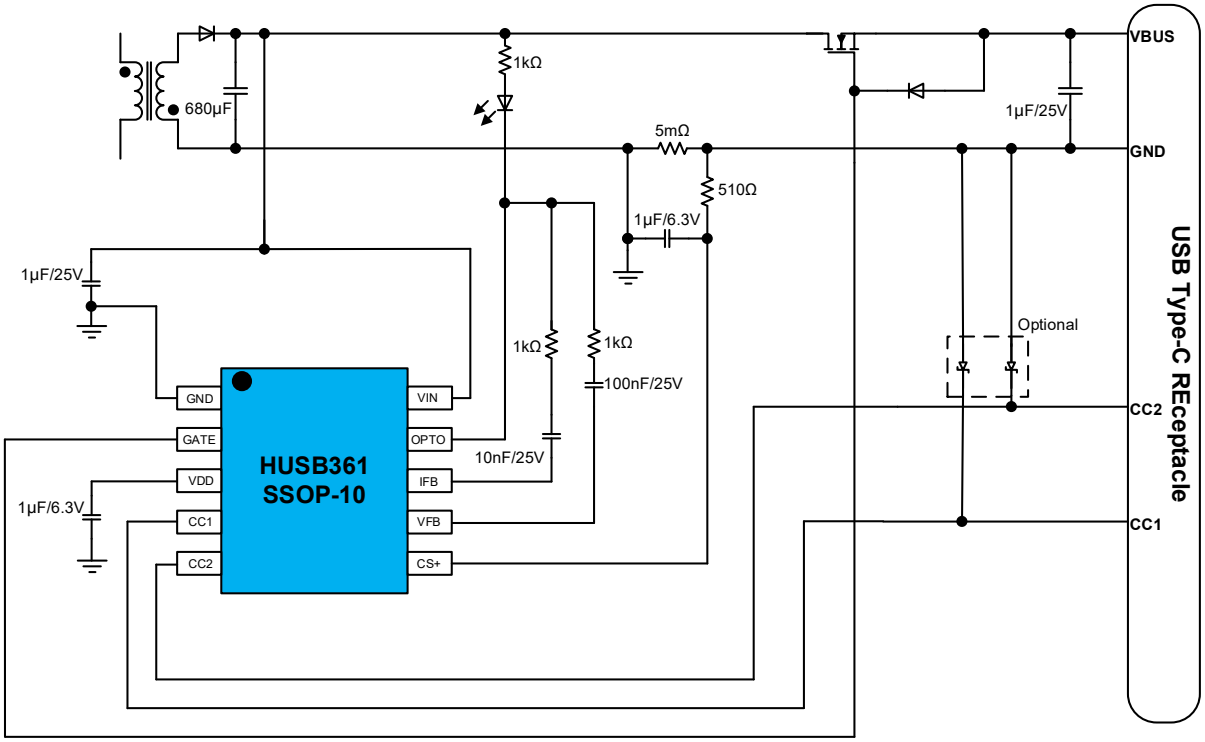
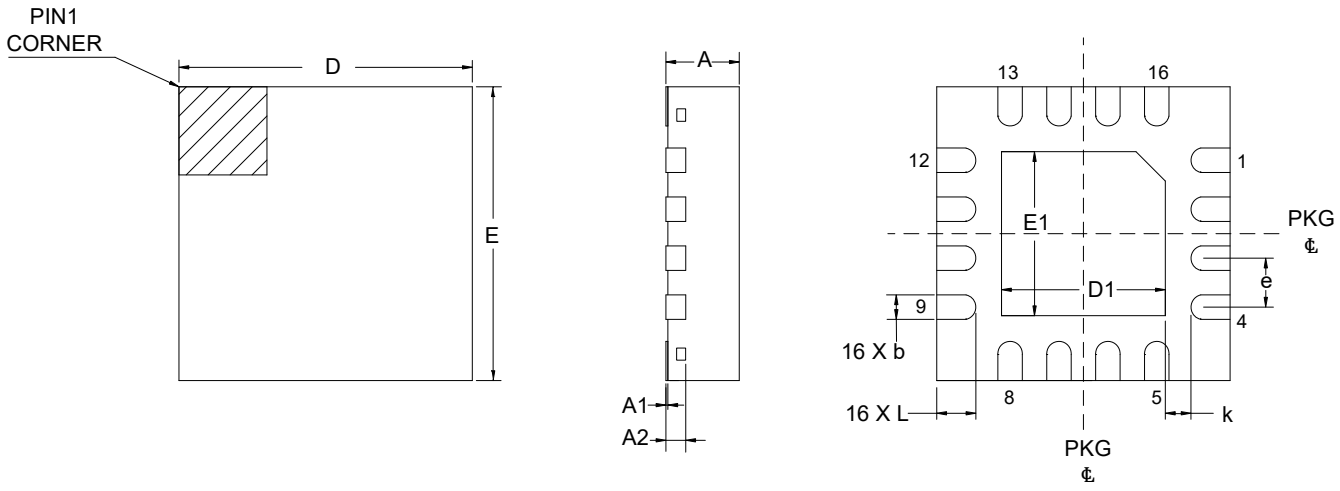


Figure 5. USB PD Source without HVDCP Protocol Supported Application Diagram(SSOP-10L Package)

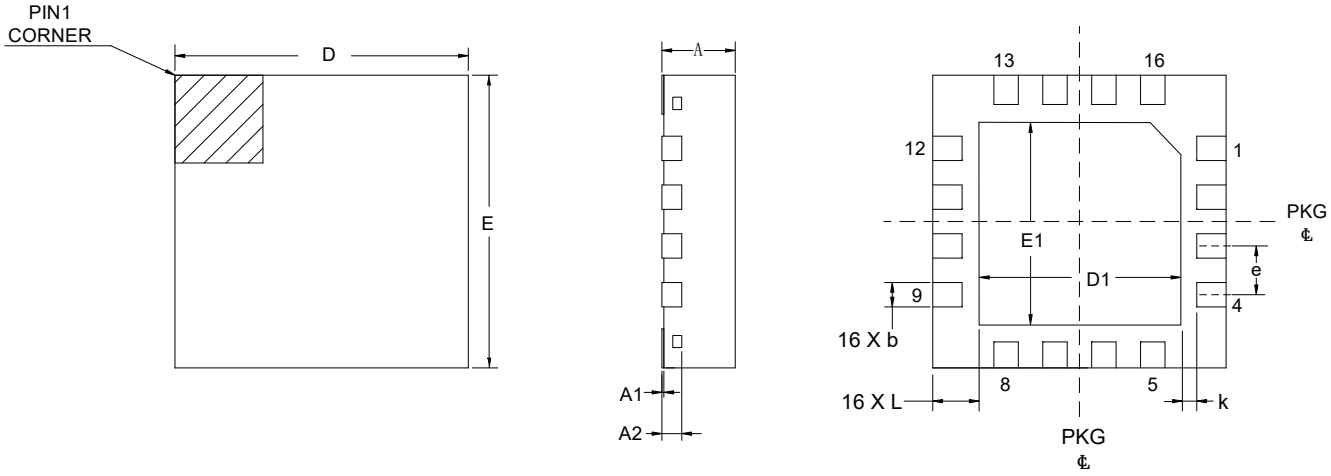
PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
D1	1.55	1.70	1.80
E1	1.55	1.70	1.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN.	

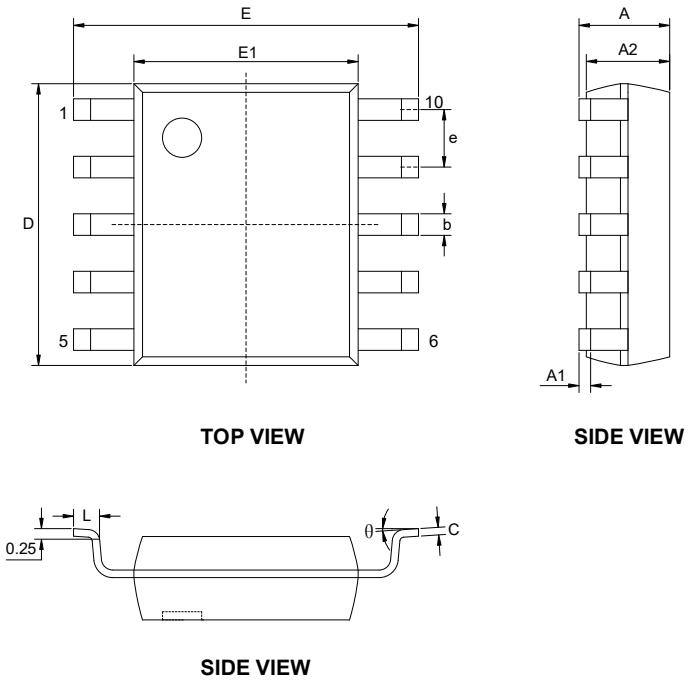
Figure 6. QFN-16L Package, 3 mm x 3 mm



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203 REF	
b	0.25	0.30	0.35
D		4.00 BSC	
E		4.00 BSC	
D1	2.60	2.70	2.80
E1	2.60	2.70	2.80
e		0.65 BSC	
L	0.30	0.40	0.50
k		0.25 REF	

Figure 7. QFN-16L Package, 4 mm x 4 mm



SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.35	1.45	1.55
b	0.30	-	0.45
C	0.17	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.00 BSC		
L	0.40	-	1.27
θ	0°	-	8°

Figure 8. SSOP-10L Package

PACKAGE TOP MARKING

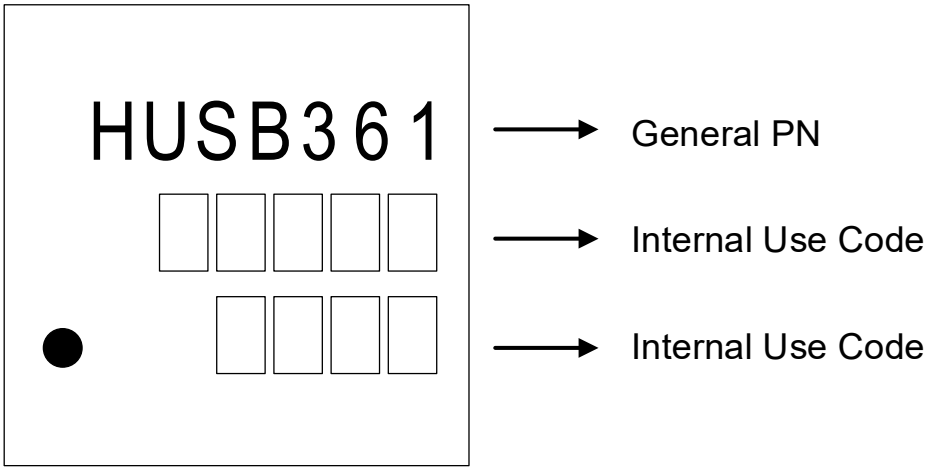


Figure 9. HUSB361 Package Top Marking (QFN-16L Package, 4 mm x 4 mm and 3 mm x 3 mm)

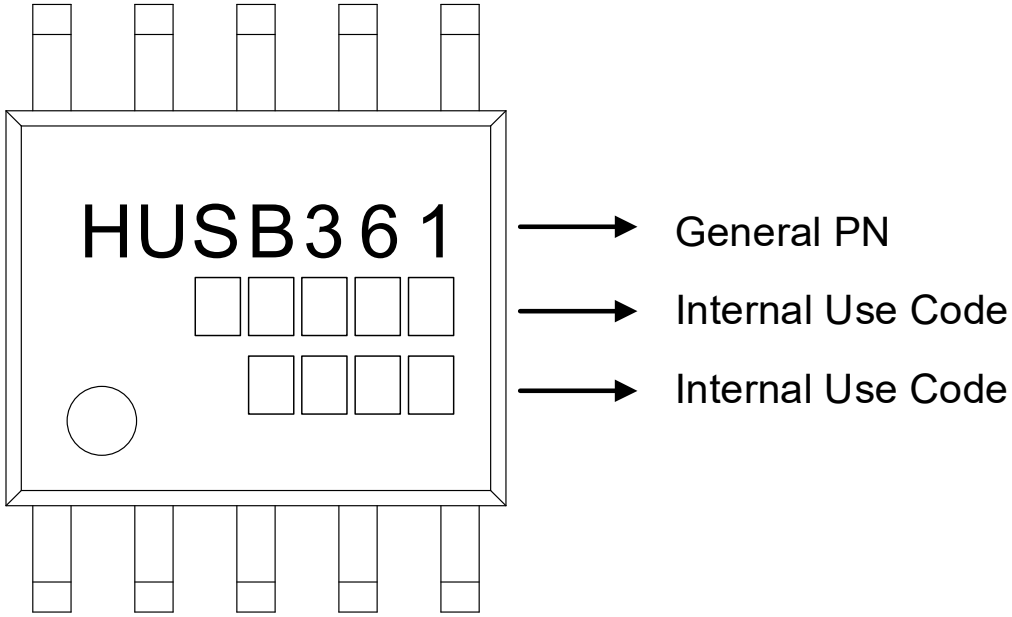
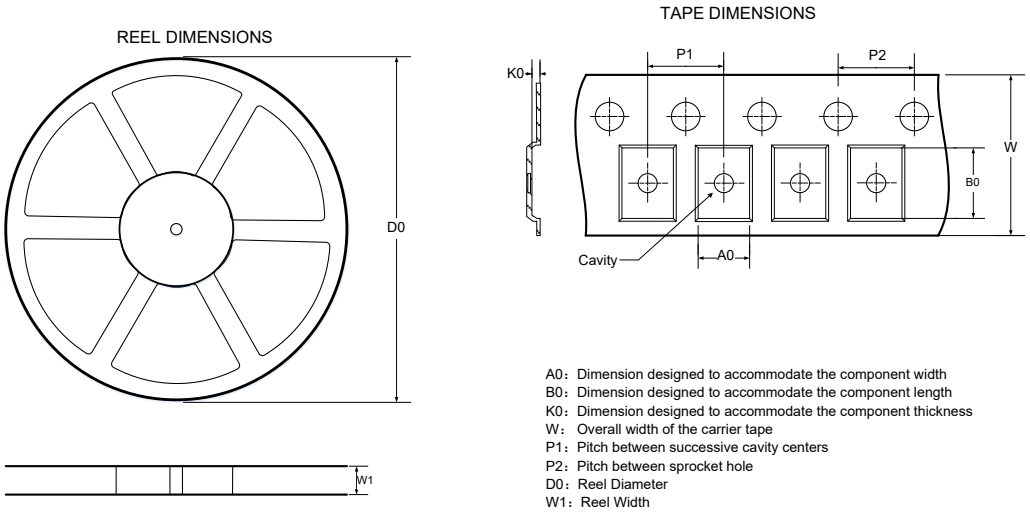


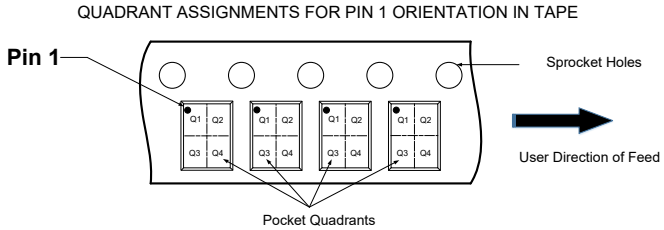
Figure 10. HUSB361 Package Top Marking (SSOP-10L Package)

ORDERING GUIDE

Model	Power Configurations	T_J Temp (°C)	Package Type	Package Option	Package Qty
HUSB361_001UA	Refer to Table 9	-40 to 125	QFN-16L, 3 mm x 3 mm	Tape & Reel	5000
HUSB361_001BA	Refer to Table 9	-40 to 125	QFN-16L, 4 mm x 4 mm	Tape & Reel	5000
HUSB361_001JA	Refer to Table 9	-40 to 125	SSOP-10L	Tape & Reel	4000
HUSB361_102UA	Refer to Table 10	-40 to 125	QFN-16L, 3 mm x 3 mm	Tape & Reel	5000
HUSB361_102BA	Refer to Table 10	-40 to 125	QFN-16L, 4 mm x 4 mm	Tape & Reel	5000
HUSB361_XXXUA	Customizable, Contact Hynetek	-40 to 125	QFN-16L, 3 mm x 3 mm	Tape & Reel	5000
HUSB361_XXXBA	Customizable, Contact Hynetek	-40 to 125	QFN-16L, 4 mm x 4 mm	Tape & Reel	5000
HUSB361_XXXJA	Customizable, Contact Hynetek	-40 to 125	SSOP-10L	Tape & Reel	4000

TAPE AND REEL INFORMATION





DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HUSB361_XXXUA	QFN3X3-16L	330.00	12.40	3.35	3.35	1.13	8.00	4.00	12.00	Q1	5000
HUSB361_XXXBA	QFN4X4-16L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000
HUSB361_XXXJA	SSOP10L	330.00	12.40	6.40	5.40	2.10	8.00	4.00	12.00	Q1	4000

All dimensions are nominal

Figure 11. Tape and Reel Information

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