HT6551

Super I/O Controller

Features

- 100% compatible to IBM PC AT/XT
- Fully IBM–BIOS compatible floppy disk controller
  - 48mA floppy drive interface buffers
  - Support two floppy drives with capability of supporting up to four drives with an external decoder
  - Support 360K/720K/1.2M/1.44M/2.88M formats
  - Support 250Kb/s, 300Kb/s, 500Kb/s, 1Mb/s data rate
- Digital data separator eliminates critical analog adjustments
- Two 16550 compatible UARTs
  - Independent control of transmit,receive,line status and data set interrupts on each channel
  - Individual modem control signals for each channel
  - Programmable serial interface characteristics for each channel:
    16 Byte FIFOS
    5-, 6-, 7-, or 8-bit characters
    Even,odd or no parity bit generation and detection
    1-, 1.5-, or 2-stop bit generation
  - Programmable baud rate generator for each channel which allows division of the timing reference clock input by 1 to $(2^{16}-1)$
- Only one 24MHz crystal for FDC and UARTs
- One IBM PC bidirection parallel port for printer
- Support AT full function Game port
- Support AT hard disk IDE interface
- Hardware/software configuration setup available
- Individual disable feature available
- Power saving feature available
- 100 pin PQFP package

Applications

- Super (Multi) I/O interface card

General Description

The HT6551 super Multi I/O chip, is an advanced CMOS single chip controller offering the complete I/O solutions for the IBM AT environments. It incorporates one floppy disk controller (FDC), two full function UARTs, one parallel port, one bus mouse port, one game port controller, IDE hard disk drive interface, standard AT address decoding for on–chip function and four configuration registers in one chip. It is fabricated with HOLTEK's high–reliability CMOS technology.

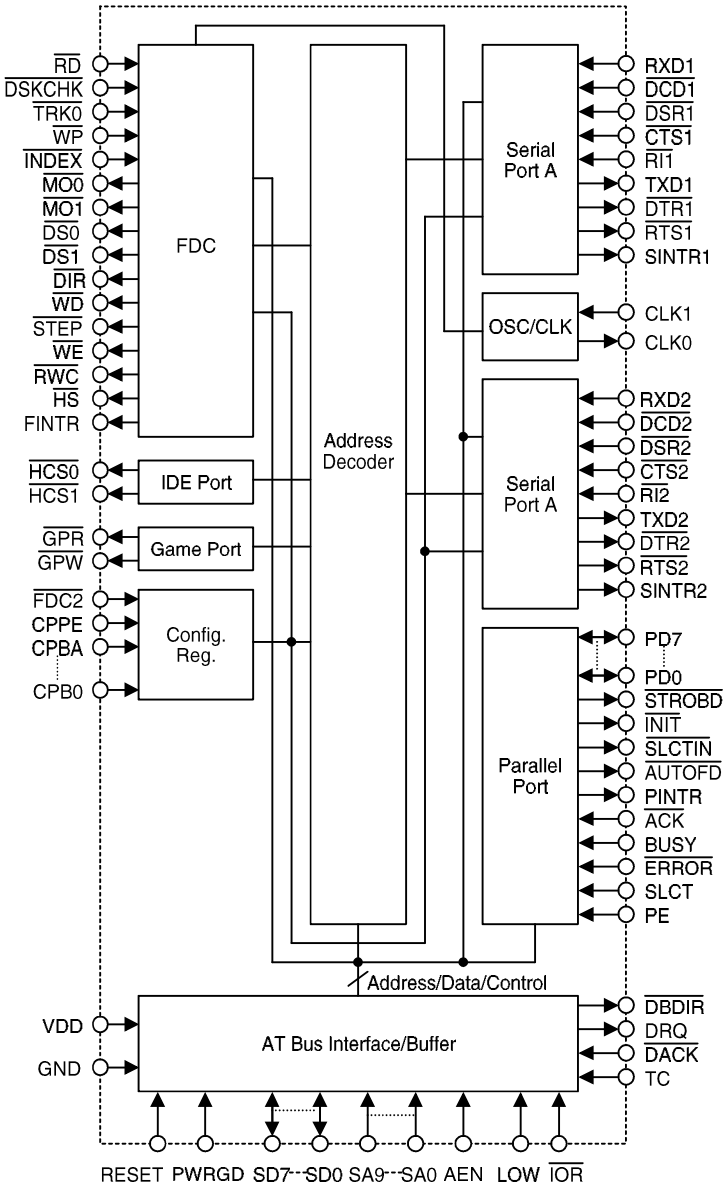
The HT6551 super Multi I/O chip contains one floppy disk controller which supports two floppy drives with capability of supporting up to four drives with an external decoder and is compatible to support 360K, 720K, 1.2M, 1.44M, 2.88M formats. Two full function fast UARTs of HT6551 which can be programmed serial interface characteristics for each channel, and a programmable baud rate generator is also included that can divide the timing reference clock input by a divisor between 1 and (2^{16}–1) and can produce a 16X clock for driving the internal transmitter logic. Provisions are also included to use this 16X clock to drive the receiver logic.

The IDE (Intelligent Drive Electronics) port of HT6551 provides address decoding and chip selects for a IDE fixed disk interface. The Game port controller decoding strobes Game port for read and write. The HT6551 has 4 very flexible and easy to select configuration registers. It will be also easy to enable or disable any supported functions. For a cost effective and space efficient design, the HT6551 is packaged in an industry standard 100-pin EIA-J PQFP package.

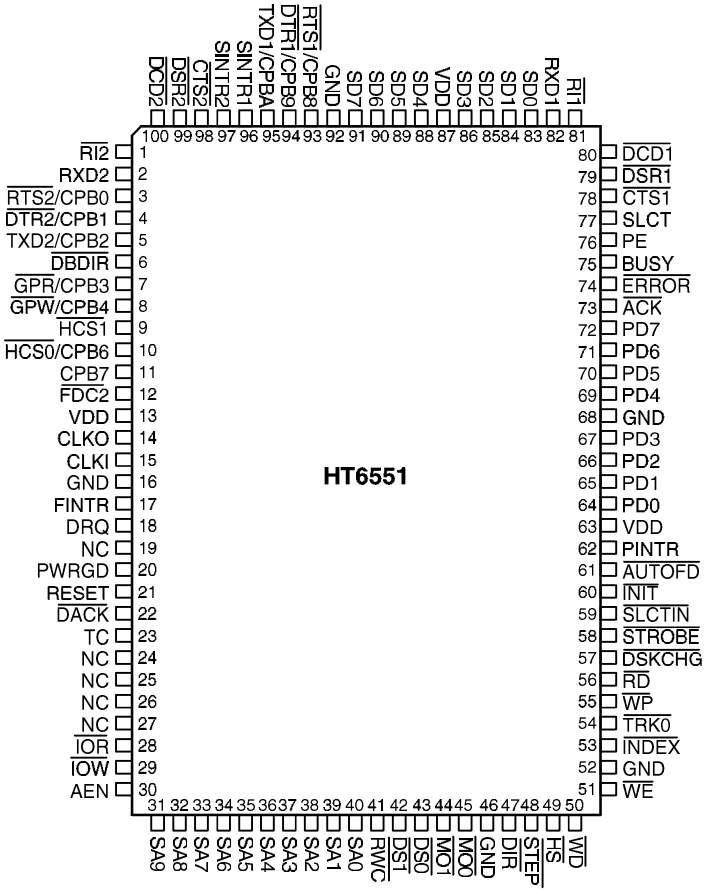
Note:

- HT6570 is incorporates the RS-232 transceiver and NE558 Timer and packaged in an 80 pin PQFP package.
- HT6571 is the RS-232 transceiver and packaged in an 20 pin PDIP package.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	I/O	Description
Host Interface (29 pins)			
31~40	SA9~SA0	I	Host address bus
83~86, 88~91	SD0~SD7	I/O	Host data bus
28	$\overline{\text{IOR}}$	I	Active low I/O read
29	$\overline{\text{IOW}}$	I	Active low I/O write
21	RESET	I	Schmitt-trigger input reset from host
30	AEN	I	DMA address enable active high
22	$\overline{\text{DACK}}$	I	Active low DMA acknowledge from host

Pin No.	Pin Name	I/O	Description
18	DRQ	O	DMA request to host
23	TC	I	Terminate DMA data transfer
19	NC		
17	FINTR	O	Floppy controller interrupt request
96	SINTR1	O	Serial port COM1 interrupt request
97	SINTR2	O	Serial port COM2 interrupt request
62	PINTR	O	Parallel port interrupt request
Parallel port Interface (17 pins)			
58	$\overline{\text{STROBE}}$	O	Data strobe, This signal indicates to the peripheral that the data at the parallel port is valid
59	$\overline{\text{SLCTIN}}$	O	Line printer select, This signal is used to select the printer when it is low
60	$\overline{\text{INIT}}$	O	Printer initialize, This signal initializes the printer when it is low
61	$\overline{\text{AUTOFD}}$	O	Autofeed, When this output is low the printer should automatically line feed after each line printed
73	$\overline{\text{ACK}}$	I	Acknowledge. This signal is set low by the printer to indicate that it has received data and is ready for next data
74	$\overline{\text{ERROR}}$	I	Printer error. This input is set by the printer when it has detected an error
75	BUSY	I	Printer busy. This input is set high by the printer when it can't accept another character
76	PE	I	Paper empty. This input is set high by the printer when it is out of paper
77	SLCT	I	Printer select. This input is set by the printer when it is selected
64~67, 69~72	PD0~PD7	I/O	Parallel port data bus
Bus Mouse Controller/Game Port Intreface (6 pins)			
24~27	NC		
11	CPB7	I/O	This pin is input pin for IDE hardware setup, when RESET is high. Output is for test
12	$\overline{\text{FDC2}}$	I/O	This pin is input pin for FDC secondary port selection, when RESET is high. Output is for test

Pin No.	Pin Name	I/O	Description
IDE Interface (2 pins)			
10	$\overline{\text{HCS0}}$/CPB6	I/O	During normal operation this pin is IDE port enable to enable 1F0~1F7H/170~177H(AT), 320~323H(XT) When RESET is high this pin becomes CPB6 input and reads data for FDC hardware setup
9	$\overline{\text{HCS1}}$	O	This pin is IDE port enable to enable 3F6~3F7H/376~377H
Game port Interface (2 pins)			
7	$\overline{\text{GPR}}$/CPB3	I/O	During normal operation this pin is game port read signal When RESET is high this pin becomes CPB3 input and reads data for IDE hardware setup
8	$\overline{\text{GPW}}$/CPB4	I/O	During normal operation this pin is game port write signal When RESET is high this pin becomes CPB4 input and reads data for game port hardware setup
Floppy Interface (15 pins)			
45	$\overline{\text{MO0}}$	O	FDD motor A enable, active low open drain output
44	$\overline{\text{MO1}}$	O	FDD motor B enable, active low open drain output
43	$\overline{\text{DS0}}$	O	FDD drive A enable, active low open drain output
42	$\overline{\text{DS1}}$	O	FDD drive B enable, active low open drain output
47	$\overline{\text{DIR}}$	O	Direction of the head stepper motor, open drain output, 1=outward, 0=inward motion movement
50	$\overline{\text{WD}}$	O	Write data, active low open drain output
48	$\overline{\text{STEP}}$	O	Step output pulses, active low open drain output.
51	$\overline{\text{WE}}$	O	Enable write to FDD, active low open drain output
41	$\overline{\text{RWC}}$	O	Reduced write current, open drain output used to select the transfer rate, 0=250 Kb/s, 1=500 Kb/s
49	$\overline{\text{HS}}$	O	Head select, open drain output
56	$\overline{\text{RD}}$	I	Read data from FDD, schmitt-trigger input
57	$\overline{\text{DSKCHG}}$	I	Diskette change, schmitt-trigger input
54	$\overline{\text{TRK0}}$	I	Track 00, head is on track 0, schmitt-trigger input

Pin No.	Pin Name	I/O	Description
55	$\overline{WP}$	I	Write protected, schmitt-trigger input
53	$\overline{INDEX}$	I	FDC index,indicates the beginning of a disk track
Serial port interface (16 pins)			
78	$\overline{CTS1}$	I	Serial 1 clear to send input, active low
79	$\overline{DSR1}$	I	Serial 1 data set ready input, active low
80	$\overline{DCD1}$	I	Serial 1 data carrier detect input, active low
81	$\overline{RI1}$	I	Serial 1 ring indicator input active low
82	RXD1	I	Serial 1 receive data input
93	$\overline{RTS1}$/CPB8	I/O	During normal operation this pin is serial 1 request to send. When RESET is high this pin becomes CPB8 input and reads data for UARTs hardware setup
94	$\overline{DTR1}$/CPB9	I/O	During normal operation this pin is serial 1 data terminal ready. When RESET is high this pin becomes CPB9 input and reads data for UARTs hardware setup
95	TXD1/CPBA	I/O	During normal operation this pin is serial 1 transmit data. When RESET is high this pin becomes CPBA input and reads data for UARTs hardware setup
98	$\overline{CTS2}$	I	Serial 2 clear to send input, active low
99	$\overline{DSR2}$	I	Serial 2 data set ready input, active low
100	$\overline{DCD2}$	I	Serial 2 data carrier detect input, active low
1	$\overline{RI2}$	I	Serial 2 ring indicator input, active low
2	RXD2	I	Serial 2 receive data input
3	$\overline{RTS2}$/CPB0	I/O	During normal operation this pin is serial 2 request to send. When RESET is high this pin becomes CPB0 input and reads data for parallel port hardware setup
4	$\overline{DTR2}$/CPB1	I/O	During normal operation this pin is serial 2 data terminal ready. When RESET is high this pin becomes CPB1 input and reads data for parallel port hardware setup
5	TXD2/CPB2	I/O	During normal operation this pin is serial 2 transmit data. When RESET is high this pin becomes CPB2 input and reads data for parallel port hardware setup

Pin No.	Pin Name	I/O	Description
Miscellaneous (19 pins)			
6	$\overline{\text{DBDIR}}$	O	This pin is data bus direction control signal
20	PWRGD	I	HT6551 is fully function when PWRGD is high. If PWRGD is low and VDD still active then HT6551 is isolated from the reset of the circuit, all inputs are disabled and all outputs tri-stated
11	CPB7	I/O	This pin is input pin for IDE hardware setup, when RESET is high. Output is for test
12	$\overline{\text{FDC2}}$	I/O	This pin is input pin for FDC secondary port selection, when RESET is high. Output is for test
15	CLKI	I	Oscillator input (24 MHz)
14	CLKO	O	Oscillator driver output
13,63,87	VDD	I	+5V supply
19,24~27	NC	—	No connection
16,46,52, 68,92	GND	I	Ground

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature.....–50°C to 125°C
Operating Temperature..... 0°C to 70°C

Electrical Characteristics

DC Characteristics

(V_{DD}=5V, TA=25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Host Interface (SD0~SD7, DRQ, FINTR, SINTR1, SINTR2 PINTR)						
V_{OLB}	Output Low Voltage	I_{OL}=10mA	—	—	0.4	V
V_{OHB}	Output High Voltage	I_{OH}=–2mA	2.4	—	V_{DD}	V
I_{LOB}	Leakage Current	V_{IN}=5V	—	—	10	μA
		V_{IN}=0V	—	—	–10	μA
Clock Input (CLKI)						
V_{ILX}	Clock Input Low Voltage	—	–0.3	—	0.8	V
V_{IHX}	Clock Input High Voltage	—	2	—	V_{DD}	V
Floppy Interface Output						
V_{OLF}	Output Low Voltage	I_{OL}=48mA	—	—	0.4	V
IDE Interface Output						
V_{OLH}	Output Low Voltage	I_{OL}=10mA	—	—	0.4	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OHH}	Output High Voltage	I_{OH}=–2mA	2.4	—	V_{DD}	V
I_{LOH}	Leakage Current	V_{IN}=V_{DD}	—	—	10	μA
I_{LOL}	Leakage Current	V_{IN}=0	—	—	–10	μA
Parallel Interface Output						
V_{OL}	Output Low Voltage	I_{OL}=10mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=–2mA	2.4	—	V_{DD}	V
Floppy Interface Input and RESET						
V_{ILM}	Input Low Voltage	—	–0.3	—	0.8	V
V_{IHM}	Input High Voltage	—	2.4	—	V_{DD}	V
V_H	Input Hysteresis	—	0.25	—	—	V
Game Port UART Interface output						
V_{OLG}	Output Low Voltage	I_{OL}=2mA	—	—	0.4	V
V_{OHG}	Output High Voltage	I_{OH}=–400μA	2.4	—	V_{DD}	V
All Other Input						
V_{IL}	Input Low Voltage	—	–0.3	—	0.8	V
V_{IH}	Input High Voltage	—	2.4	—	V_{DD}	V
V_{LIH}	Input Leakage Current	V_{IN}=V_{DD}	—	—	10	μA
V_{LIL}	Input Leakage Current	V_{IN}=0	—	—	–10	μA

AC Characteristics (V_{DD}=5V, TA=25°C)

• UART/PARALLEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{IRS}	Delay From Initial Irq Reset To Transmit Start	—	1/16	—	8/16	Baud Rate
T_{STI}	Delay From Stop To Interrupt	—	9/16	—	—	Baud Rate
T_{HR}	Delay From $\overline{IOW}$ To Reset Interrupt	100pf Loading	—	—	175	ns
T_{SI}	Delay From Initial $\overline{IOW}$ To Interrupt	—	9/16	—	16/16	Baud Rate
T_{IR}	Delay From $\overline{IOR}$ To Reset	100pf Loading	—	—	1	ns
T_{SINT}	Delay From Stop To Set Interrupt	—	—	—	1/2	Baud Rate
T_{RINT}	Delay Form $\overline{Ior}$ Reset Interrupt	100pf Loading	—	—	250	ns
T_{MWO}	Delay From $\overline{IOW}$ To Output	100pf Loading	—	—	200	ns

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SIM}	Set Interrupt Delay From MODEM Input	100pf Loading	—	—	250	ns
T_{RIM}	Reset Interrupt Delay From $\overline{IOR}$	100pf Loading	—	—	250	ns
T_{OAD}	Interrupt Active Delay	100pf Loading	—	—	30	ns
T_{IID}	Interrupt Inactive Delay	100pf Loading	—	—	30	ns
N	Baud Rate Divisor	100pf Loading	—	—	$2^{16}-1$	unit

• FDC : Data rate= 1000 /500 /300 /250 KB/SEC

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{AR}	SA9~SA0, AEN, $\overline{DACK}$ Setup time to $\overline{IOR}\downarrow$	—	25	—	—	ns
T_{RA}	SA9~SA0, AEN, $\overline{DACK}$ hold time from $\overline{IOR}\uparrow$	100pf Loading	0	—	—	ns
T_{RR}	IOR width	100pf Loading	200	—	—	ns
T_{FD}	Data access time from $\overline{IOR}\downarrow$	100pf Loading	—	—	80	ns
T_{DH}	Data hold time from $\overline{IOR}\downarrow$	—	10	—		ns
T_{DF}	SD to float from $\overline{IOR}\uparrow$	—	10	—	50	ns
T_{RI}	IRQ Delay from $\overline{IOR}\uparrow$	—	—	—	360/ 570/ 675	ns
T_{AW}	SA9~SA0, AEN, $\overline{DACK}$ setup time to $\overline{IOW}\downarrow$	—	25	—	—	ns
T_{WA}	SA9~SA0, AEN, $\overline{DACK}$ hold time from $\overline{IOW}\uparrow$	—	0	—	—	ns
T_{WW}	$\overline{IOW}$ width	—	200	—	—	ns
T_{DW}	Data setup time to $\overline{IOW}\uparrow$	—	60	—	—	ns
T_{WD}	Data hold time from $\overline{IOW}\uparrow$	—	0	—	—	ns
T_{WI}	IRQ delay from $\overline{IOW}\uparrow$	—	—	—	360/ 570/ 675	ns
T_{MCY}	DMA cycle time	—	27	—	—	μs
T_{AM}	DMA reset delay time from $\overline{DACK}\downarrow$	—	—	—	50	ns
T_{MA}	DRQ to $\overline{DACK}$ delay	—	0	—	—	ns
T_{AA}	$\overline{DACK}$ width	—	260/ 430/ 510	—	—	ns

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{MR}	$\overline{IOR}$ delay from DRQ	—	0	—	—	ns
T_{MW}	$\overline{IOW}$ dleay from DRQ	—	0	—	—	ns
T_{MRW}	$\overline{IOW}$ or $\overline{IOR}$ response time from DRQ	—	—	—	12/ 20 24	μs
T_{TC}	TC width	—	135/ 220/ 260	—	—	ns
T_{RST}	RESET width	—	1.8/ 3.0/ 3.5	—	—	μs
T_{IDX}	$\overline{INDEX}$ width	—	0.5/ 0.9/ 1.0	—	—	μs
T_{DST}	$\overline{DIR}$ setup time to $\overline{STEP}$	—	1.0/ 1.6/ 2.0	—	—	μs
T_{STD}	$\overline{DIR}$ hold time from $\overline{STEP}$	—	24/ 40/ 48	—	—	μs
T_{STP}	$\overline{STEP}$ pulse width	—	6.8/ 11.5/ 13.8	7.0/ 11.7/ 14	7.2/ 11.9/ 14.2	μs
T_{SC}	$\overline{STEP}$ cycle time	—	**	**	**	μs
T_{WDD}	$\overline{WD}$ pulse width	—	37/ 100/ 188/ 225	62/ 125/ 210/ 250	87/ 150/ 235/ 275	ns
T_{WPC}	Write Precompensation	—	37/ 100/ 188/ 225	62/ 125/ 210/ 250	87/ 150/ 235/ 275	μs

Notes:
* Typical nsvalues for TA=25°C and nominal value for supply voltage.
** Programmable from 2ms to 32ms in 2ms increments.

• Game Port

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{GMRW}	Game Command delay time from RD/WR Game Port	—	—	150	ns

Functional Description

• I/O port address

Function	Possible Port Address	Comment
Serial port 1	3F8~3FFH 3E8~3EFH	COM1 COM3
Serial port 2	2F8~2FFH 2E8~2EFH	COM2 COM4
Parallel port	3BC~3BEH 378~37BH 278~27BH	PRT1 PRT2 PRT3
FDC port	3F2, 3F4, 3F5, 3F7H 372, 374, 375, 377H	FDC1 FDC2
IDE port	1F0~1F7H, 3F6, 3F7H 170~177H, 376, 377H	IDE1 IDE2
Game port	201H	

Note: These ports are selected by configuration registers.

* Configuration setup

There are four configuration registers CR# 00, 01, 02, 0FH which are write only. CR# 00, 01H can be either hardware or software setup, CR# 02, 0FH can only be accessed through software.

During RESET, HT6551 is in hardware configure mode and each configure pin's state is read. After RESET, HT6551 is in software configure mode and can be programed by software.

– Hardware setup

During RESET goes high, the HT6551 will read the inputs from the following pins and setup the configuration registers CR# 00H and CR# 01H.

Pin Name	CPBA	CPB9	CPB8	CPB7	CPB6		CPB4	CPB3	CPB2	CPB1	CPB0
Pin No.	95	94	93	11	10		8	7	5	4	3

Note:

CPBA~CPB8: Serial port selection

CPBA	CPB9	CPB8	UART1	UART2
0	0	0	disable	disable
0	0	1	COM1 (3F8~3FFH)	disable
0	1	0	disable	COM2 (2F8~2FFH)
0	1	1	COM1 (3F8~3FFH)	COM2 (2F8~2FFH)
1	0	0	COM3 (3E8~3EFH)	COM4 (2E8~2EFH)
1	0	1	disable	COM1 (3F8~3FFH)
1	1	0	COM2 (2F8~2FFH)	disable
1	1	1	COM2 (2F8~2FFH)	COM1 (3F8~3FFH)

CPB7: IDE enable. 0=disable, 1=enable.
CPB6: FDC enable. 0=disable, 1=enable.
CPB4: GAME enable. 0=disable, 1=enable.
CPB3: Secondary IDE selection. 0=secondary selected, 1=primary selected.
CPB2: Printer mode selection 0=extended mode, 1=normal mode.
CPB1, 0: Parallel port selection.

– Software Setup

The procedures for setting up the configuration registers are described as follow:

(a) To enter configuration mode:
  (1) Write 55H to 2FAH.
  (2) Follow by writing AAH to 3FAH.

(b) To program configuration register:
  (1) Write XXH to 3FAH, where XXH is the configuration register index.
  (2) Follow by writing YYH to 2FAH, where YYH is the data for CR# XXH.

(c) To exit from configuration mode:
  (1) Writer 0FH to 3FAH, then write any value YYH to 2FAH.
  (2) or write AAH to 3FAH.

The following describes the bit functions of each configuration registers (CR# 00, 01, 02 and 0FH)

(1) Configuration Register – CR# 00H (Write only)

Bit No.	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPB7	CPB6	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0

Note:
CPB7: IDE enable. 0=disable, 1=enable.
CPB6: FDC enable. 0=disable, 1=enable.
CPB5: Mouse enable. 0=disable, 1=enable.
CPB4: GAME enable. 0=disable, 1=enable.
CPB3: IDE port address selection. 0=secondary selected, 1=primary selected.
CPB2: Printer mode selection. 0=extended mode, 1=normal mode.
CPB1, 0: Parallel port selection.

CPB1	CPB0	Paralled port
0	0	disable
0	1	PRT1 (3BC~3BFH)
1	0	PRT2 (378~37BH)
1	1	PRT3 (278~27BH)

(2) Configuration register – CR# 01H (Write only)

Bit No.	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	CPBA	CPB9	CPB8

Note: CPBA~CPB8: Serial port selection.

CPBA	CPB9	CPB8	UART1	UART2
0	0	0	disable	disable
0	0	1	COM1 (3F8~3FFH)	disable
0	1	0	disable	COM2 (2F8~2FFH)
0	1	1	COM1 (3F8~3FFH)	COM2 (2F8~2FFH)
1	0	0	COM3 (3E8~3EFH)	COM4 (2E8~2EFH)
1	0	1	disable	COM1 (3F8~3FFH)
1	1	0	COM2 (2F8~2FFH)	disable
1	1	1	COM2 (2F8~2FFH)	COM1 (3F8~3FFH)

(3) Configuration register – CR# 02H (Write only)

Bit No.	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENB	$\overline{\text{MPD}}$	$\overline{\text{PDD}}$	$\overline{\text{SPD}}$	$\overline{\text{FPD}}$	$\overline{\text{HPD}}$	$\overline{\text{GPD}}$	—

Where
ENB: 1=valid configuration setup.
MPD: Mouse port power down, 0=power down, 1=normal (default).
PDD: Printer port power down, 0=power down, 1=normal (default).
SPD: Serial port power down, 0=power down, 1=normal (default).
FPD: Floppy disk port power down, 0=power down, 1=normal (default).
HPD: IDE port power down, 0=power down, 1=normal (default).
GPD: Parallel port selection.

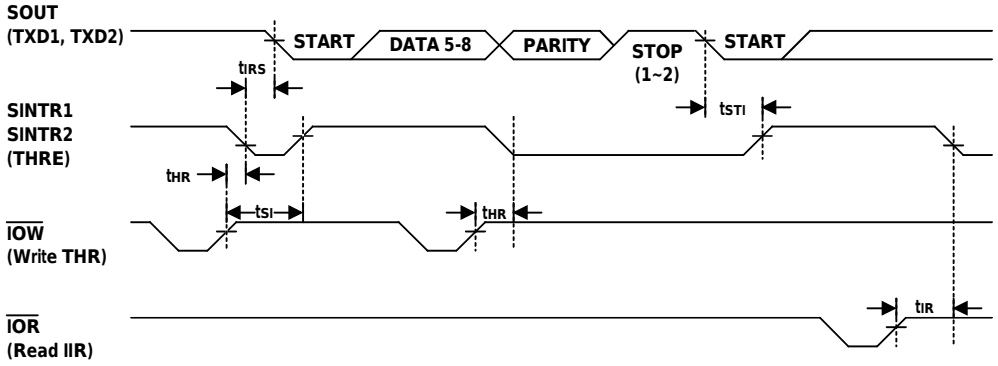
(4) Configuration register – CR# 0FH (Writer only)

Writing any value to CR# 0FH can bring the HT6550A out of the configuration mode.

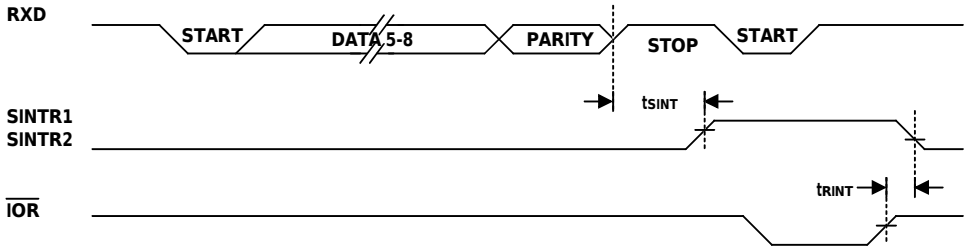
Timing Diagram

UART/Parallel port

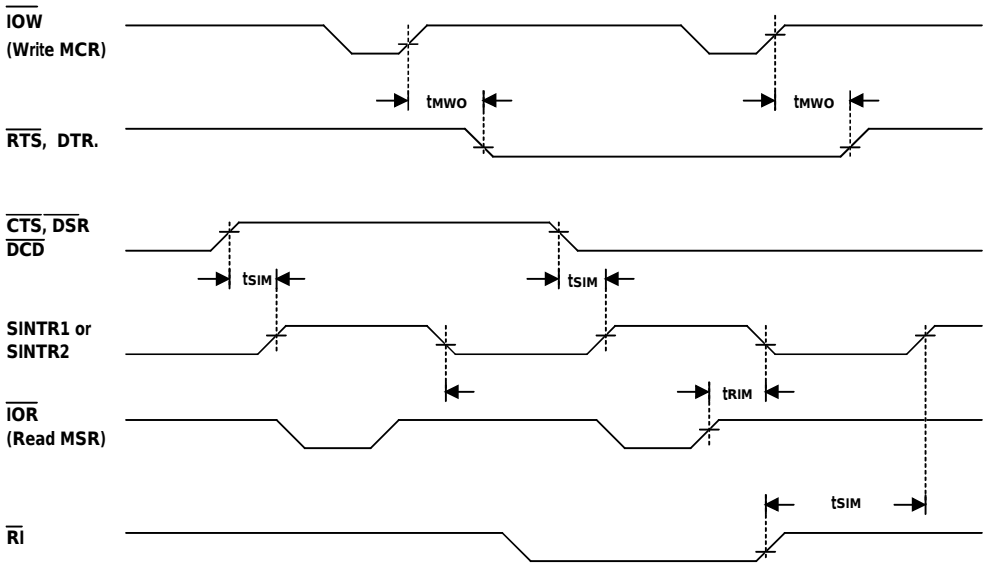
- Transmitter timming



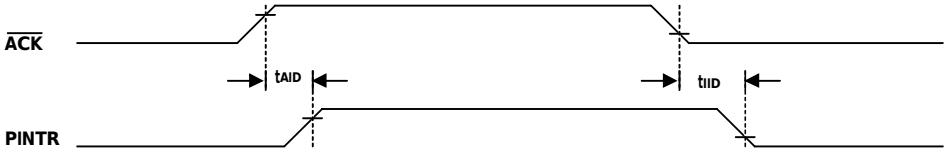
- Receiver timing



- MODEM control timing

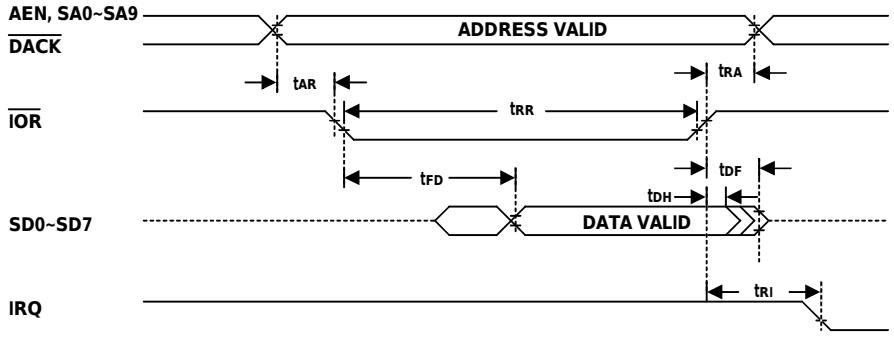


- Printer interrupt timing

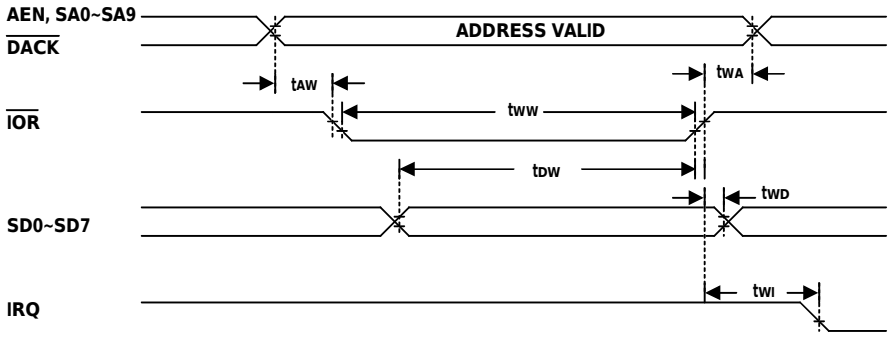


FDC

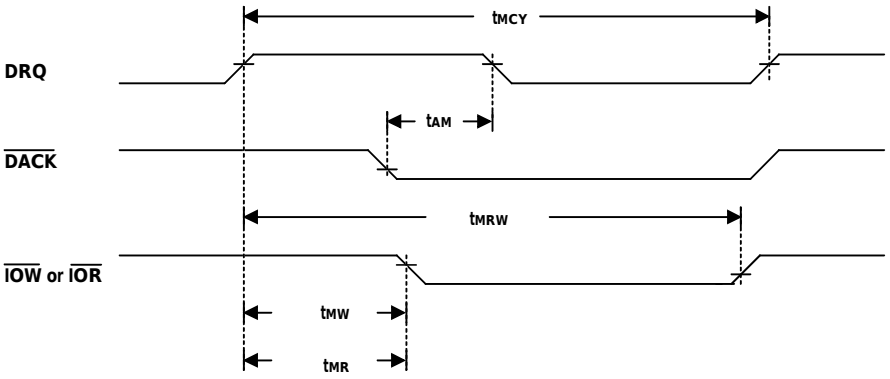
- Processor read operation



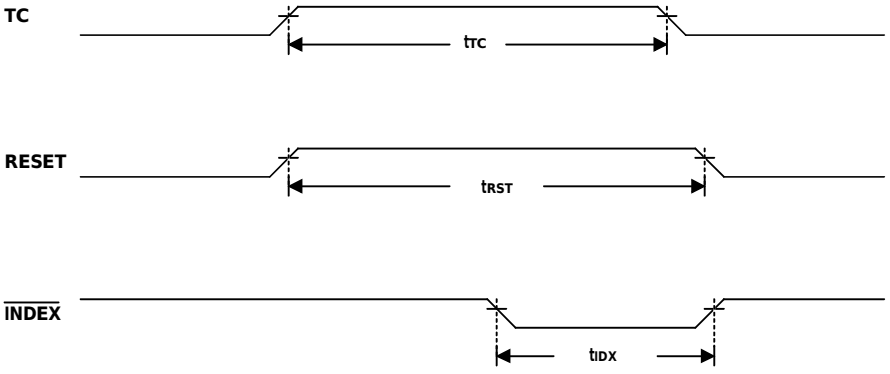
- Processor write operation



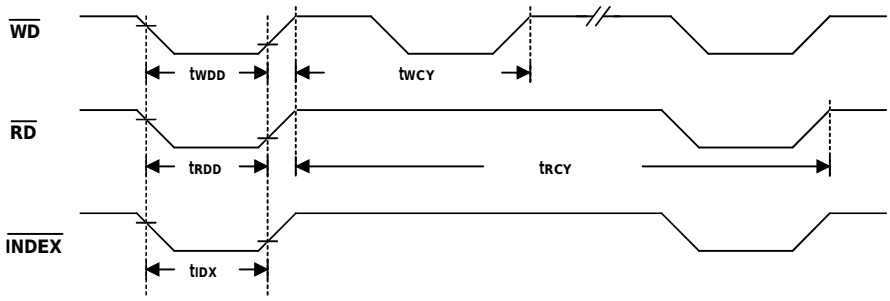
- DMA operation



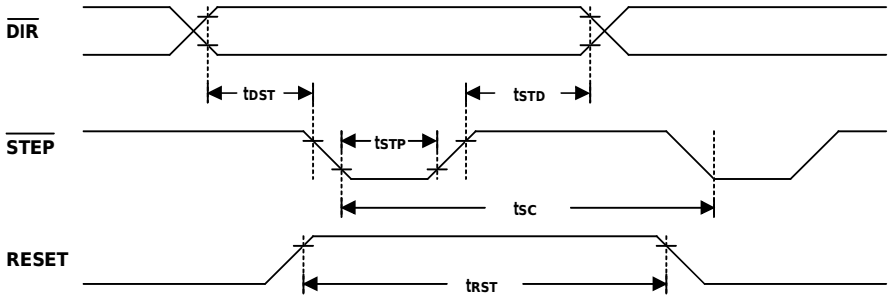
- Terminal count



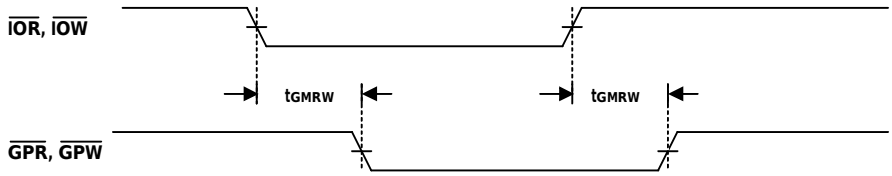
- FDD write/read operation



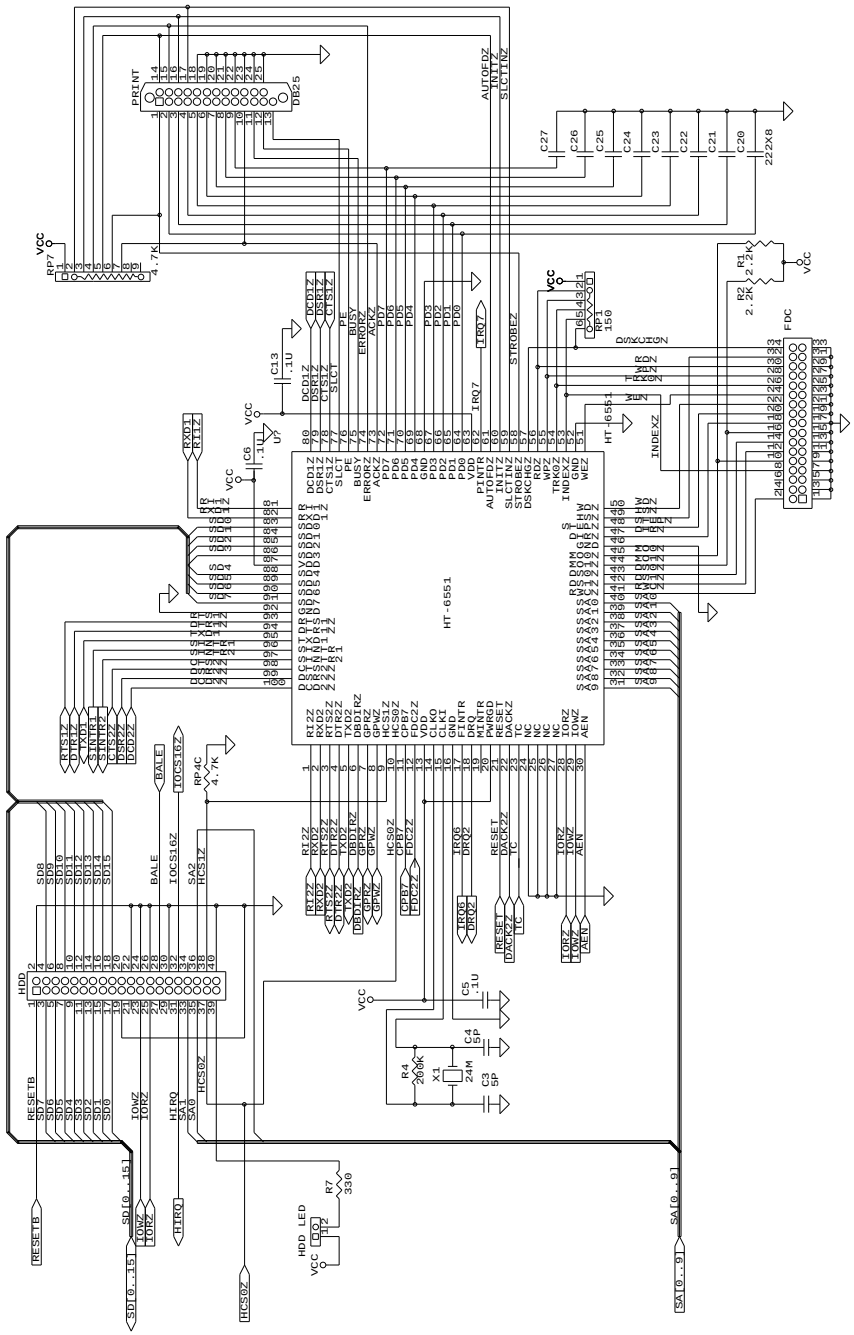
- Seek operation

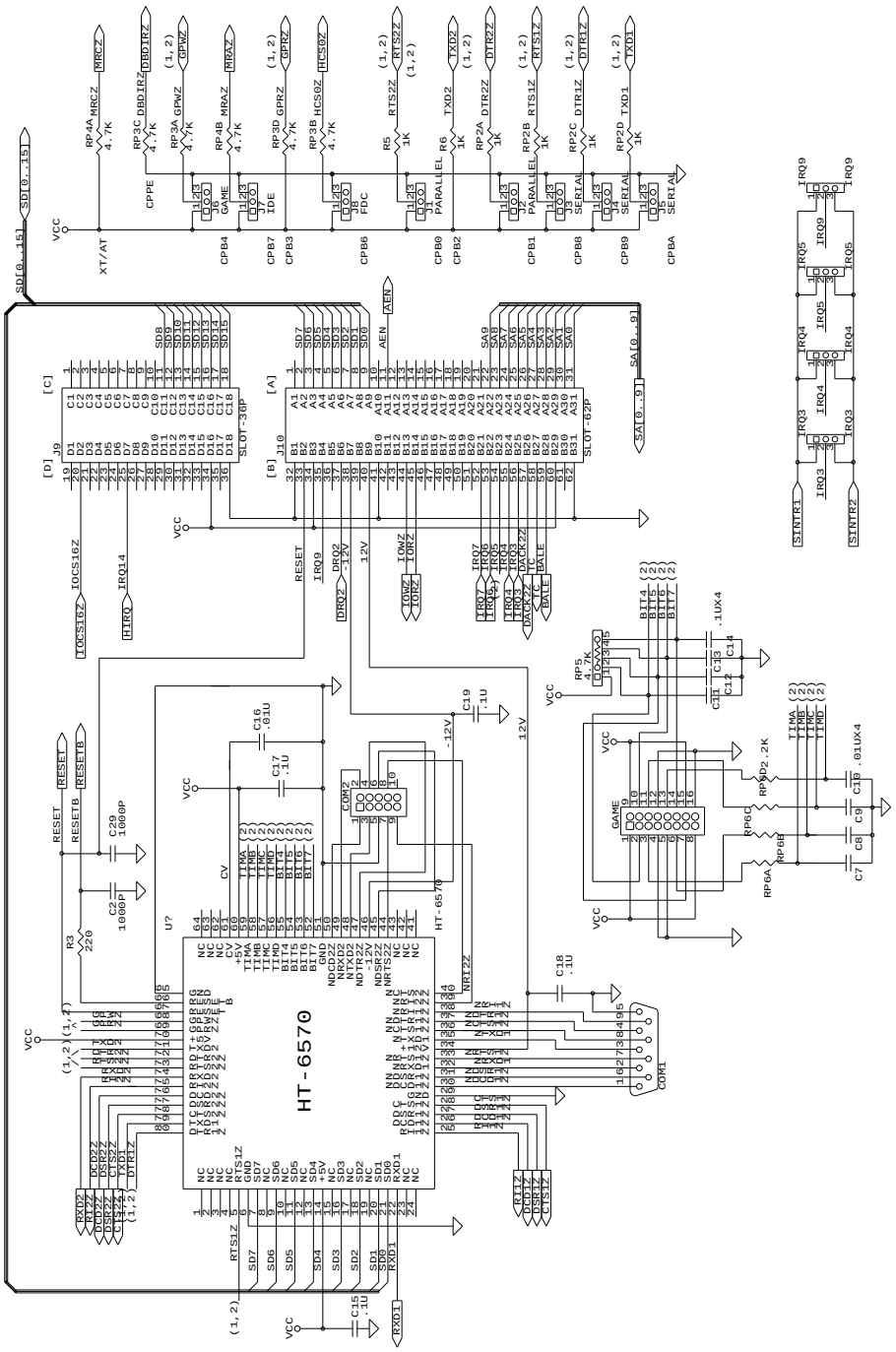


Game Port



Application Diagram




HT-6570
U?
J9
J10
SLOT-36P
SLOT-62P
SD[0..15]
SA[0..9]
VCC
RESET
RESETB
IRQ14
IRQ9
DRQ2
IOCS16Z
AEN
12V
-12V
XT/AT
CPPE
CPB4
CPB7
CPB3
CPB6
CPB0
CPB2
CPB1
CPB8
CPB9
CPBA
J6 GAME
IDE
J8 FDC
PARALLEL
J2 PARALLEL
SERIAL
J4 SERIAL
J5 SERIAL
RP4A MRCZ 4.7K
RP3C DBDIRZ 4.7K
RP3A GPWZ 4.7K
RP4B MRAZ 4.7K
RP3D GPRZ 4.7K
RP3B HCS0Z 4.7K
R5 RTS2Z 1K
R6 TXD2 1K
RP2A DTR2Z 1K
RP2B RTS1Z 1K
RP2C DTR1Z 1K
RP2D TXD1 1K
RP5 4.7K
RP6A RP6B RP6C RP6D 2.2K
C2 1000P
C16 .01U
C17 .1U
C18 .1U
C19 .1U
C29 1000P
C15 .1U
R3 220
COM1
COM2
GAME
IRQ3
IRQ4
IRQ5
IRQ9
STNTR1
STNTR2
TIMA
TIMB
TIMC
TIMD
BIT4
BIT5
BIT6
BIT7
.1UX4
.01UX4