

### Features

- Operating voltage:  
f<sub>sys</sub>=4MHz: 2.2V~5.5V  
f<sub>sys</sub>=8MHz: 3.3V~5.5V
- 19 bidirectional I/O lines (max.)
- 1 interrupt input shared with an I/O line
- 8-bit programmable timer/event counter with overflow interrupt and 7-stage prescaler
- On-chip crystal and RC oscillator
- Watchdog Timer
- 2048×14 program memory
- 64×8 data memory RAM
- Supports PFD for sound generation
- HALT function and wake-up feature reduce power consumption
- Up to 0.5μs instruction cycle with 8MHz system clock at V<sub>DD</sub>=5V
- 6-level subroutine nesting
- 8 channels 9-bit resolution A/D converter
- 1-channel 8-bit PWM output shared with one I/O line
- Bit manipulation instruction
- 14-bit table read instruction
- 63 powerful instructions
- All instructions in one or two machine cycles
- Low voltage reset function
- I<sup>2</sup>C Bus (slave mode)
- 24-pin SKDIP/SOP package

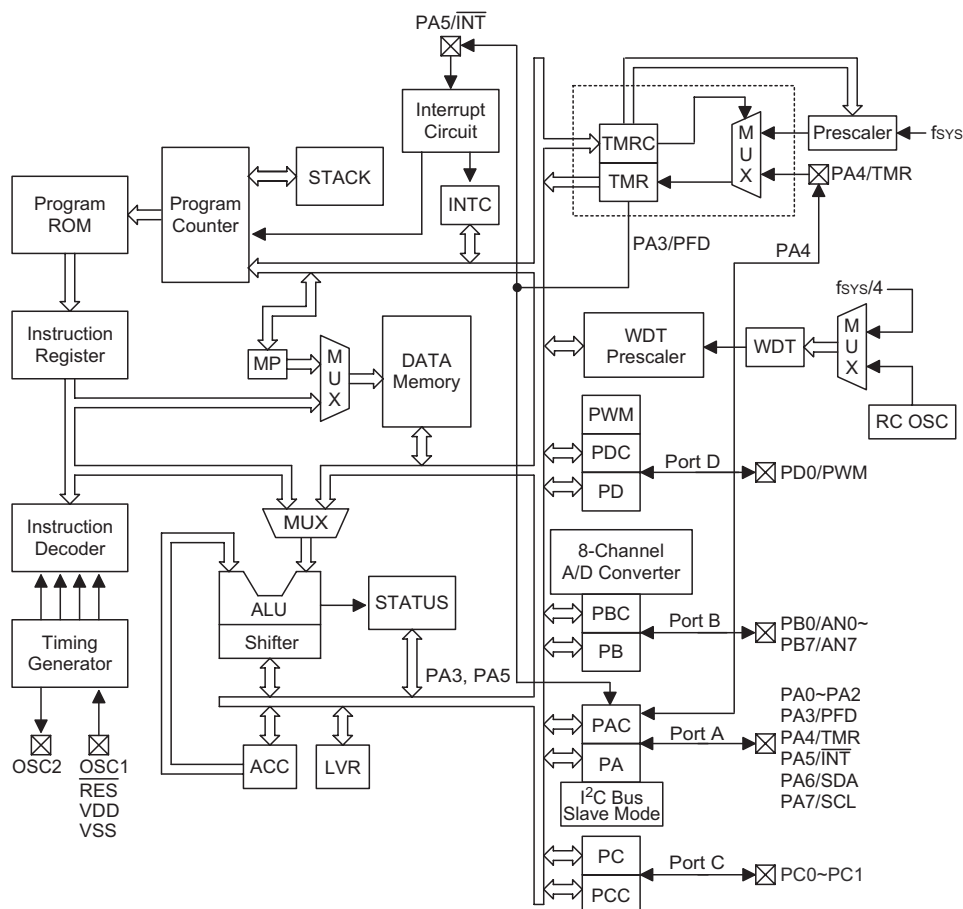
### General Description

The HT46R22/HT46C22 are 8-bit, high performance, RISC architecture microcontroller devices specifically designed for A/D applications that interface directly to analog signals, such as those from sensors. The mask version HT46C22 is fully pin and functionally compatible with the OTP version HT46R22 device.

The advantages of low power consumption, I/O flexibility, programmable frequency divider, timer functions, oscillator options, multi-channel A/D Converter, Pulse Width Modulation function, I<sup>2</sup>C interface, HALT and wake-up functions, enhance the versatility of these devices to suit a wide range of A/D application possibilities such as sensor signal processing, motor driving, industrial control, consumer products, subsystem controllers, etc.

I<sup>2</sup>C is a trademark of Philips Semiconductors

## Block Diagram



## Pin Assignment

PB5/AN5	1	24	PB6/AN6
PB4/AN4	2	23	PB7/AN7
PA3/PFD	3	22	PA4/TMR
PA2	4	21	PA5/INT
PA1	5	20	PA6/SDA
PA0	6	19	PA7/SCL
PB3/AN3	7	18	OSC2
PB2/AN2	8	17	OSC1
PB1/AN1	9	16	VDD
PB0/AN0	10	15	RES
VSS	11	14	PD0/PWM
PC0	12	13	PC1

**HT46R22/HT46C22**  
— 24 SKDIP-A/SOP-A

**Pad Description**

Pad Name	I/O	Options	Description
PA0~PA2 PA3/PFD PA4/TMR PA5/INT PA6/SDA PA7/SCL	I/O	Pull-high Wake-up PA3 or PFD I/O or Serial Bus	Bidirectional 8-bit input/output port. Each bit can be configured as wake-up input by options. Software instructions determine the CMOS output or Schmitt trigger input with or without pull-high resistor (determined by pull-high options: bit option). The PFD, TMR and INT are pin-shared with PA3, PA4 and PA5, respectively. Once the I <sup>2</sup> C Bus function is used, the internal registers related to PA6 and PA7 can not be used.
PB0/AN0 PB1/AN1 PB2/AN2 PB3/AN3 PB4/AN4 PB5/AN5 PB6/AN6 PB7/AN7	I/O	Pull-high	Bidirectional 8-bit input/output port. Software instructions determine the CMOS output, Schmitt trigger input with or without pull-high resistor (determined by pull-high option: port option) or A/D input. Once a PB line is selected as an A/D input (by using software control), the I/O function and pull-high resistor are disabled automatically.
PC0~PC1	I/O	Pull-high	Bidirectional 2-bit input/output port. Software instructions determine the CMOS output, Schmitt trigger input with or without pull-high resistor (determine by pull-high option: port option).
PD0/PWM	I/O	Pull-high I/O or PWM	Bidirectional 1-bit input/output port. Software instructions determine the CMOS output, Schmitt trigger input with or without a pull-high resistor (determined by pull-high option: port option). The PWM output function is pin-shared with PD0 (dependent on PWM options).
OSC1 OSC2	I O	Crystal or RC	OSC1, OSC2 are connected to an RC network or a Crystal (determined by options) for the internal system clock. In the case of RC operation, OSC2 is the output terminal for 1/4 system clock.
RES	I	—	Schmitt trigger reset input. Active low.
VSS	—	—	Negative power supply, ground.
VDD	—	—	Positive power supply
TEST1 TEST2 TEST3	I	—	TEST mode input pin It disconnects in normal operation

**Absolute Maximum Ratings**

Supply Voltage .....	V <sub>SS</sub> -0.3V to V <sub>SS</sub> +6.0V	Storage Temperature .....	-50°C to 125°C
Input Voltage .....	V <sub>SS</sub> -0.3V to V <sub>DD</sub> +0.3V	Operating Temperature .....	-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>DD</sub>	Operating Voltage	—	f <sub>SYS</sub> =4MHz	2.2	—	5.5	V
		—	f <sub>SYS</sub> =8MHz	3.3	—	5.5	V
I <sub>DD1</sub>	Operating Current (Crystal OSC)	3V	No load, f <sub>SYS</sub> =4MHz ADC disable	—	0.6	1.5	mA
		5V		—	2	4	mA
I <sub>DD2</sub>	Operating Current (RC OSC)	3V	No load, f <sub>SYS</sub> =4MHz ADC disable	—	0.8	1.5	mA
		5V		—	2.5	4	mA
I <sub>DD3</sub>	Operating Current (Crystal OSC, RC OSC)	5V	No load, f <sub>SYS</sub> =8MHz ADC disable	—	4	8	mA
I <sub>STB1</sub>	Standby Current (WDT Enabled)	3V	No load, system HALT	—	—	5	μA
		5V		—	—	10	μA
I <sub>STB2</sub>	Standby Current (WDT Disabled)	3V	No load, system HALT	—	—	1	μA
		5V		—	—	2	μA
V <sub>IL1</sub>	Input Low Voltage for I/O Ports, TMR and INT	—	—	0	—	0.3V <sub>DD</sub>	V
V <sub>IH1</sub>	Input High Voltage for I/O Ports, TMR and INT	—	—	0.7V <sub>DD</sub>	—	V <sub>DD</sub>	V
V <sub>IL2</sub>	Input Low Voltage ( $\overline{\text{RES}}$ )	—	—	0	—	0.4V <sub>DD</sub>	V
V <sub>IH2</sub>	Input High Voltage ( $\overline{\text{RES}}$ )	—	—	0.9V <sub>DD</sub>	—	V <sub>DD</sub>	V
V <sub>LVR</sub>	Low Voltage Reset	—	—	2.7	3	3.3	V
I <sub>OL</sub>	I/O Port Sink Current	3V	V <sub>OL</sub> =0.1V <sub>DD</sub>	4	8	—	mA
		5V	V <sub>OL</sub> =0.1V <sub>DD</sub>	10	20	—	mA
I <sub>OH</sub>	I/O Port Source Current	3V	V <sub>OH</sub> =0.9V <sub>DD</sub>	-2	-4	—	mA
		5V	V <sub>OH</sub> =0.9V <sub>DD</sub>	-5	-10	—	mA
R <sub>PH</sub>	Pull-high Resistance	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ
V <sub>AD</sub>	A/D Input Voltage	—	—	0	—	V <sub>DD</sub>	V
E <sub>AD</sub>	A/D Conversion Error	—	—	—	±0.5	±1	LSB
I <sub>ADC</sub>	Additional Power Consumption if A/D Converter is Used	3V	—	—	0.5	1	mA
		5V		—	1.5	3	mA

**A.C. Characteristics**

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
f <sub>SYS</sub>	System Clock	—	2.2V~5.5V	400	—	4000	kHz
		—	3.3V~5.5V	400	—	8000	kHz
f <sub>TIMER</sub>	Timer I/P Frequency (TMR)	—	2.2V~5.5V	0	—	4000	kHz
		—	3.3V~5.5V	0	—	8000	kHz
t <sub>WDTOSC</sub>	Watchdog Oscillator Period	3V	—	45	90	180	μs
		5V	—	32	65	130	μs
t <sub>RES</sub>	External Reset Low Pulse Width	—	—	1	—	—	μs
t <sub>SST</sub>	System Start-up Timer Period	—	Wake-up from HALT	—	1024	—	*t <sub>SYS</sub>
t <sub>INT</sub>	Interrupt Pulse Width	—	—	1	—	—	μs
t <sub>AD</sub>	A/D Clock Period	—	—	1	—	—	μs
t <sub>ADC</sub>	A/D Conversion Time	—	—	—	76	—	t <sub>AD</sub>
t <sub>ADCS</sub>	A/D Sampling Time	—	—	—	32	—	t <sub>AD</sub>
t <sub>IIC</sub>	I <sup>2</sup> C Bus Clock Period	—	Connect to external pull-high resistor 2kΩ	64	—	—	*t <sub>SYS</sub>

Note: \*t<sub>SYS</sub>=1/f<sub>SYS</sub>

## Functional Description

### Execution Flow

The system clock for the microcontroller is derived from either a crystal or an RC oscillator. The system clock is internally divided into four non-overlapping clocks. One instruction cycle consists of four system clock cycles.

Instruction fetching and execution are pipelined in such a way that a fetch takes an instruction cycle while decoding and execution takes the next instruction cycle. However, the pipelining scheme causes each instruction to effectively execute in a cycle. If an instruction changes the program counter, two cycles are required to complete the instruction.

### Program Counter – PC

The program counter (PC) controls the sequence in which the instructions stored in program ROM are executed and its contents specify full range of program memory.

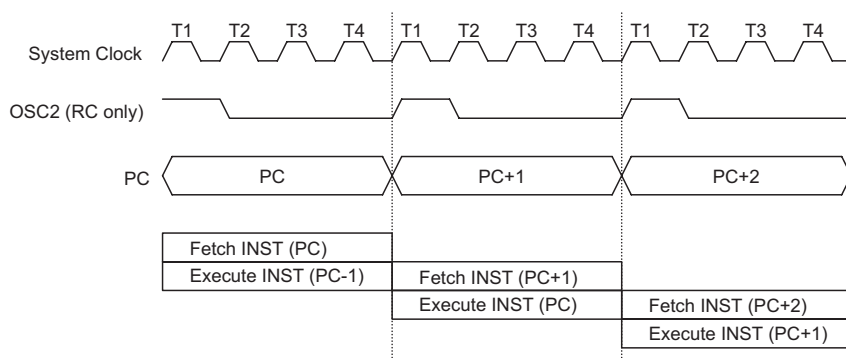
After accessing a program memory word to fetch an instruction code, the contents of the program counter are incremented by 1. The program counter then points to the memory word containing the next instruction code.

When executing a jump instruction, conditional skip execution, loading PCL register, subroutine call, initial reset, internal interrupt, external interrupt or return from subroutine, the PC manipulates the program transfer by loading the address corresponding to each instruction.

The conditional skip is activated by instructions. Once the condition is met, the next instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaces it to get the proper instruction. Otherwise proceed with the next instruction.

The lower byte of the program counter (PCL) is a readable and writeable register (06H). Moving data into the PCL performs a short jump. The destination will be within 256 locations.

When a control transfer takes place, an additional dummy cycle is required.



**Execution Flow**

Mode	Program Counter										
	*10	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
Initial Reset	0	0	0	0	0	0	0	0	0	0	0
External Interrupt	0	0	0	0	0	0	0	0	1	0	0
Timer/Event Counter Overflow	0	0	0	0	0	0	0	1	0	0	0
A/D Converter Interrupt	0	0	0	0	0	0	0	1	1	0	0
I <sup>2</sup> C Bus Interrupt	0	0	0	0	0	0	1	0	0	0	0
Skip	Program Counter + 2										
Loading PCL	*10	*9	*8	@7	@6	@5	@4	@3	@2	@1	@0
Jump, Call Branch	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0
Return from Subroutine	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

**Program Counter**

Note: \*10~\*0: Program counter bits  
#10~#0: Instruction code bits

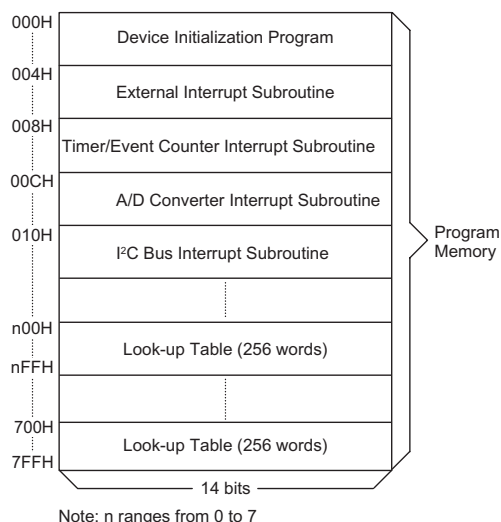
S10~S0: Stack register bits  
@7~@0: PCL bits

## Program Memory – ROM

The program memory is used to store the program instructions which are to be executed. It also contains data, table, and interrupt entries, and is organized into 2048×14 bits, addressed by the program counter and table pointer.

Certain locations in the program memory are reserved for special usage:

- Location 000H  
This area is reserved for program initialization. After chip reset, the program always begins execution at location 000H.
- Location 004H  
This area is reserved for the external interrupt service program. If the INT input pin is activated, the interrupt is enabled and the stack is not full, the program begins execution at location 004H.
- Location 008H  
This area is reserved for the timer/event counter interrupt service program. If a timer/event counter overflow, and if the interrupt is enabled and the stack is not full, the program begins execution at location 008H.



**Program Memory**

- Location 00CH  
This area is reserved for the A/D converter interrupt service program. If an A/D converter interrupt results from an end of A/D conversion, and if the interrupt is enabled and the stack is not full, the program begins execution at location 00CH.
- Location 010H  
This area is reserved for the I<sup>2</sup>C Bus interrupt service program. If the I<sup>2</sup>C Bus interrupt resulting from a slave address is match or completed 1 byte of data transfer, and if the interrupt is enable and the stack is not full, the program begins execution at location 010H.
- Table location  
Any location in the ROM space can be used as look-up tables. The instructions "TABRDC [m]" (the current page, 1 page=256 words) and "TABRDL [m]" (the last page) transfer the contents of the lower-order byte to the specified data memory, and the higher-order byte to TBLH (08H). Only the destination of the lower-order byte in the table is well-defined, the other bits of the table word are transferred to the lower portion of TBLH, and the remaining 2 bit is read as "0". The Table Higher-order byte register (TBLH) is read only. The table pointer (TBLP) is a read/write register (07H), which indicates the table location. Before accessing the table, the location must be placed in TBLP. The TBLH is read only and cannot be restored. If the main routine and the ISR (Interrupt Service Routine) both employ the table read instruction, the contents of the TBLH in the main routine are likely to be changed by the table read instruction used in the ISR. Errors can occur. In other words, using the table read instruction in the main routine and the ISR simultaneously should be avoided. However, if the table read instruction has to be applied in both the main routine and the ISR, the interrupt is supposed to be disabled prior to the table read instruction. It will not be enabled until the TBLH has been backed up. All table related instructions require two cycles to complete the operation. These areas may function as normal program memory depending upon the requirements.

Instruction	Table Location										
	*10	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
TABRDC [m]	P10	P9	P8	@7	@6	@5	@4	@3	@2	@1	@0
TABRDL [m]	1	1	1	@7	@6	@5	@4	@3	@2	@1	@0

**Table Location**

Note: \*10~\*0: Table location bits  
@7~@0: Table pointer bits

P10~P8: Current program counter bits





### Indirect Addressing Register

Location 00H is an indirect addressing register that is not physically implemented. Any read/write operation of [00H] accesses data memory pointed to by MP (01H). Reading location 00H itself indirectly will return the result 00H. Writing indirectly results in no operation.

The memory pointer register MP (01H) is a 7-bit register. The bit 7 of MP is undefined and reading will return the result "1". Any writing operation to MP will only transfer the lower 7-bit data to MP.

### Accumulator

The accumulator is closely related to ALU operations. It is also mapped to location 05H of the data memory and can carry out immediate data operations. The data movement between two data memory locations must pass through the accumulator.

### Arithmetic and Logic Unit – ALU

This circuit performs 8-bit arithmetic and logic operations. The ALU provides the following functions:

- Arithmetic operations (ADD, ADC, SUB, SBC, DAA)
- Logic operations (AND, OR, XOR, CPL)
- Rotation (RL, RR, RLC, RRC)
- Increment and Decrement (INC, DEC)
- Branch decision (SZ, SNZ, SIZ, SDZ ....)

The ALU not only saves the results of a data operation but also changes the status register.

### Status Register – STATUS

This 8-bit register (0AH) contains the 0 flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). It also records the status information and controls the operation sequence.

With the exception of the TO and PDF flags, bits in

the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition operations related to the status register may give different results from those intended. The TO flag can be affected only by system power-up, a WDT time-out or executing the "CLR WDT" or "HALT" instruction. The PDF flag can be affected only by executing the "HALT" or "CLR WDT" instruction or a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

In addition, on entering the interrupt sequence or executing the subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status are important and if the subroutine can corrupt the status register, precautions must be taken to save it properly.

### Interrupt

The device provides an external interrupt, an internal timer/event counter interrupt, the A/D converter interrupt and the I<sup>2</sup>C Bus interrupts. The interrupt control register 0 (INTC0;0BH) and interrupt control register 1 (INTC1;1EH) contains the interrupt control bits to set the enable or disable and the interrupt request flags.

Once an interrupt subroutine is serviced, all the other interrupts will be blocked (by clearing the EMI bit). This scheme may prevent any further interrupt nesting. Other interrupt requests may happen during this interval but only the interrupt request flag is recorded. If a certain interrupt requires servicing within the service routine, the EMI bit and the corresponding bit of INTC0 and INTC1 may be set to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the SP is decremented. If immediate service is desired, the stack must be prevented from becoming full.

Bit No.	Label	Function
0	C	C is set if the operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
1	AC	AC is set if the operation results in a carry out of the low nibbles in addition or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
2	Z	Z is set if the result of an arithmetic or logic operation is 0; otherwise Z is cleared.
3	OV	OV is set if the operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
4	PDF	PDF is cleared by system power-up or executing the "CLR WDT" instruction. PDF is set by executing the "HALT" instruction.
5	TO	TO is cleared by system power-up or executing the "CLR WDT" or "HALT" instruction. TO is set by a WDT time-out.
6, 7	—	Unused bit, read as "0"

**Status (0AH) Register**

All these kinds of interrupts have a wake-up capability. As an interrupt is serviced, a control transfer occurs by pushing the program counter onto the stack, followed by a branch to a subroutine at specified location in the program memory. Only the program counter is pushed onto the stack. If the contents of the register or status register (STATUS) are altered by the interrupt service program which corrupts the desired control sequence, the contents should be saved in advance.

External interrupts are triggered by a high to low transition of INT and the related interrupt request flag (EIF; bit 4 of INTC0) will be set. When the interrupt is enabled, the stack is not full and the external interrupt is active, a subroutine call to location 04H will occur. The interrupt request flag (EIF) and EMI bits will be cleared to disable other interrupts.

The internal timer/event counter interrupt is initialized by setting the timer/event counter interrupt request flag (TF; bit 5 of INTC0), caused by a timer overflow. When the interrupt is enabled, the stack is not full and the TF bit is set, a subroutine call to location 08H will occur. The related interrupt request flag (TF) will be reset and the EMI bit cleared to disable further interrupts.

The A/D converter interrupt is initialized by setting the A/D converter request flag (ADF; bit 6 of INTC0), caused by an end of A/D conversion. When the interrupt is enabled, the stack is not full and the ADF is set, a subroutine call to location 0CH will occur. The related interrupt request flag (ADF) will be reset and the EMI bit cleared to disable further interrupts.

The I<sup>2</sup>C Bus interrupt is initialized by setting the I<sup>2</sup>C Bus interrupt request flag (HIF; bit 4 of INTC1), caused by a slave address match (HAAS="1") or 1 byte of data transfer is completed. When the interrupt is enabled, the stack is not full and the HIF bit is set, a subroutine call to location 10H will occur. The related interrupt request flag (HIF) will be reset and the EMI bit cleared to disable further interrupts.

During the execution of an interrupt subroutine, other interrupt acknowledgments are held until the "RETI" instruction is executed or the EMI bit and the related interrupt control bit are set to 1 (of course, if the stack is not full). To return from the interrupt subroutine, "RET" or "RETI" may be invoked. RETI will set the EMI bit to enable an interrupt service, but RET will not.

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In the case of simultaneous requests the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

Interrupt Source	Priority	Vector
External Interrupt	1	04H
Timer/Event Counter Overflow	2	08H
A/D Converter Interrupt	3	0CH
I <sup>2</sup> C Bus Interrupt	4	10H

Bit No.	Label	Function
0	EMI	Controls the master (global) interrupt (1= enabled; 0= disabled)
1	EET	Controls the external interrupt (1= enabled; 0= disabled)
2	ETI	Controls the timer/event counter interrupt (1= enabled; 0= disabled)
3	EADI	Controls the A/D converter interrupt (1= enabled; 0= disabled)
4	EIF	External interrupt request flag (1= active; 0= inactive)
5	TF	Internal timer/event counter request flag (1= active; 0= inactive)
6	ADF	A/D converter request flag (1= active; 0= inactive)
7	—	For test mode used only. Must be written as "0"; otherwise may result in unpredictable operation.

**INTC0 (0BH) Register**

Bit No.	Label	Function
0	EHI	Controls the I <sup>2</sup> C Bus interrupt (1=enabled; 0=disabled)
1~3	—	Unused bit, read as "0"
4	HIF	I <sup>2</sup> C Bus interrupt request flag (1=active; 0=inactive)
5~7	—	Unused bit, read as "0"

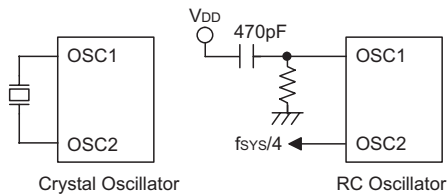
**INTC1 (1EH) Register**

The timer/event counter interrupt request flag (TF), external interrupt request flag (EIF), A/D converter request flag (ADF), the I<sup>2</sup>C Bus interrupt request flag (HIF), enable timer/event counter bit (ETI), enable external interrupt bit (EEI), enable A/D converter interrupt bit (EADI), enable I<sup>2</sup>C Bus interrupt bit (EHI) and enable master interrupt bit (EMI) constitute an interrupt control register 0 (INTC0) and an interrupt control register 1 (INTC1) which are located at 0BH and 1EH in the data memory. EMI, EEI, ETI, EADI, EHI are used to control the enabling/disabling of interrupts. These bits prevent the requested interrupt from being serviced. Once the interrupt request flags (TF, EIF, ADF, HIF) are set, they will remain in the INTC0 and INTC1 register until the interrupts are serviced or cleared by a software instruction.

It is recommended that a program does not use the "CALL subroutine" within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and enabling the interrupt is not well controlled, the original control sequence will be damaged once the "CALL" operates in the interrupt subroutine.

#### Oscillator Configuration

There are two oscillator circuits in the microcontroller.



System Oscillator

Both are designed for system clocks, namely the RC oscillator and the Crystal oscillator, which are determined by the options. No matter what oscillator type is selected, the signal provides the system clock. The HALT mode stops the system oscillator and ignores an external signal to conserve power.

If an RC oscillator is used, an external resistor between OSC1 and VSS is required and the resistance must range from 30kΩ to 750kΩ. The system clock, divided

by 4, is available on OSC2 with pull-high resistor, which can be used to synchronize external logic. The RC oscillator provides the most cost effective solution. However, the frequency of oscillation may vary with VDD, temperatures and the chip itself due to process variations. It is, therefore, not suitable for timing sensitive operations where an accurate oscillator frequency is desired.

If the Crystal oscillator is used, a crystal across OSC1 and OSC2 is needed to provide the feedback and phase shift required for the oscillator, and no other external components are required. Instead of a crystal, a resonator can also be connected between OSC1 and OSC2 to get a frequency reference, but two external capacitors in OSC1 and OSC2 are required (If the oscillating frequency is less than 1MHz).

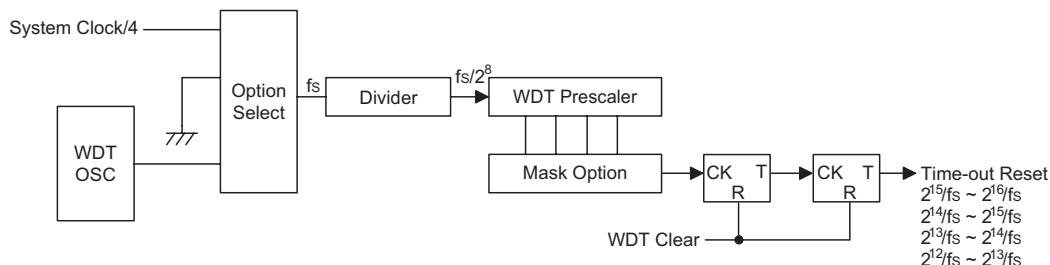
The WDT oscillator is a free running on-chip RC oscillator, and no external components are required. Even if the system enters the power down mode, the system clock is stopped, but the WDT oscillator still works with a period of approximately 65μs@5V. The WDT oscillator can be disabled by options to conserve power.

#### Watchdog Timer – WDT

The clock source of the WDT is implemented by an dedicated RC oscillator (WDT oscillator) or instruction clock (system clock divided by 4) decided by options. This timer is designed to prevent a software malfunction or sequence jumping to an unknown location with unpredictable results. The watchdog Timer can be disabled by an option. If the watchdog Timer is disabled, all the executions related to the WDT result in no operation.

Once an internal WDT oscillator (RC oscillator with period 65μs@5V normally) is selected, it is divided by  $2^{12} \sim 2^{15}$  (by option to get the WDT time-out period). The minimum period of WDT time-out period is about 300ms~600ms. This time-out period may vary with temperature, VDD and process variations. By selection the WDT options, longer time-out periods can be realized. If the WDT time-out is selected  $2^{15}$ , the maximum time-out period is divided by  $2^{15} \sim 2^{16}$  about 2.1s~4.3s.

If the WDT oscillator is disabled, the WDT clock may still come from the instruction clock and operate in the same manner except that in the halt state the WDT may stop counting and lose its protecting purpose. In this situation



Watchdog Timer

the logic can only be restarted by external logic. If the device operates in a noisy environment, using the on-chip RC oscillator (WDT OSC) is strongly recommended, since the HALT will stop the system clock.

The WDT overflow under normal operation will initialize "chip reset" and set the status bit TO. Whereas in the HALT mode, the overflow will initialize a "warm reset" only the program counter and stack pointer are reset to 0. To clear the contents of WDT, three methods are adopted; external reset (a low level to  $\overline{\text{RES}}$ ), software instructions, or a HALT instruction. The software instructions include CLR WDT and the other set – CLR WDT1 and CLR WDT2. Of these two types of instruction, only one can be active depending on the options – "CLR WDT times selection option". If the "CLR WDT" is selected (i.e. CLRWDT times equal 1), any execution of the CLR WDT instruction will clear the WDT. In case "CLR WDT1" and "CLR WDT2" are chosen (i.e. CLRWDT times equal two), these two instructions must be executed to clear the WDT; otherwise, the WDT may reset the chip because of time-out.

If the WDT time-out period is selected  $f_s/2^{12}$  (options), the WDT time-out period ranges from  $f_s/2^{12} \sim f_s/2^{13}$ , since the "CLR WDT" or "CLR WDT1" and "CLR WDT2" instructions only clear the last two stages of the WDT.

#### **Power Down Operation – HALT**

The HALT mode is initialized by the "HALT" instruction and results in the following...

- The system oscillator will be turned off but the WDT oscillator keeps running (if the WDT oscillator is selected).
- The contents of the on chip RAM and registers remain unchanged.
- WDT will be cleared and recounted again (if the WDT clock is from the WDT oscillator).
- All of the I/O ports maintain their original status.
- The PDF flag is set and the TO flag is cleared.

The system can leave the HALT mode by means of an external reset, an interrupt, an external falling edge signal on port A or a WDT overflow. An external reset causes a device initialization and the WDT overflow performs a "warm reset". After the TO and PDF flags are examined, the reason for chip reset can be determined.

The PDF flag is cleared by system power-up or executing the "CLR WDT" instruction and is set when executing the "HALT" instruction. The TO flag is set if the WDT time-out occurs, and causes a wake-up that only resets the program counter and SP; the others keep their original status.

The port A wake-up and interrupt methods can be considered as a continuation of normal execution. Each bit in port A can be independently selected to wake up the device by the options. Awakening from an I/O port stimulus, the program will resume execution of the next instruction. If it is awakening from an interrupt, two sequences may happen. If the related interrupt is disabled or the interrupt is enabled but the stack is full, the program will resume execution at the next instruction. If the interrupt is enabled and the stack is not full, the regular interrupt response takes place. If an interrupt request flag is set to "1" before entering the HALT mode, the wake-up function of the related interrupt will be disabled. Once a wake-up event occurs, it takes  $1024 t_{\text{SYS}}$  (system clock period) to resume normal operation. In other words, a dummy period will be inserted after wake-up. If the wake-up results from an interrupt acknowledgment, the actual interrupt subroutine execution will be delayed by one or more cycles. If the wake-up results in the next instruction execution, this will be executed immediately after the dummy period is finished.

To minimize power consumption, all the I/O pins should be carefully managed before entering the HALT status.

## Reset

There are three ways in which a reset can occur:

- $\overline{\text{RES}}$  reset during normal operation
- $\overline{\text{RES}}$  reset during HALT
- WDT time-out reset during normal operation

The WDT time-out during HALT is different from other chip reset conditions, since it can perform a "warm re-set" that resets only the program counter and SP, leaving the other circuits in their original state. Some registers remain unchanged during other reset conditions. Most registers are reset to the "initial condition" when the reset conditions are met. By examining the PDF and TO flags, the program can distinguish between different "chip resets".

TO	PDF	RESET Conditions
0	0	RES reset during power-up
u	u	RES reset during normal operation
0	1	RES wake-up HALT
1	u	WDT time-out during normal operation
1	1	WDT wake-up HALT

Note: "u" means unchanged

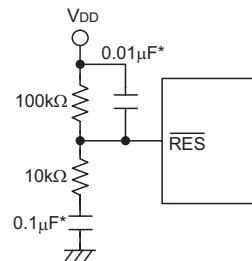
To guarantee that the system oscillator is started and stabilized, the SST (System Start-up Timer) provides an extra-delay of 1024 system clock pulses when the system reset (power-up, WDT time-out or RES reset) or the system awakes from the HALT state.

When a system reset occurs, the SST delay is added during the reset period. Any wake-up from HALT will enable the SST delay.

An extra option load time delay is added during system reset (power-up, WDT time-out at normal mode or  $\overline{\text{RES}}$  reset).

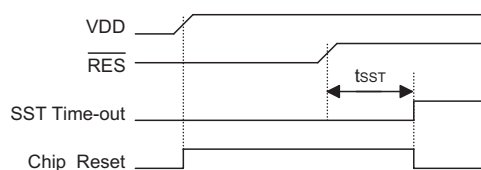
The functional unit chip reset status are shown below.

Program Counter	000H
Interrupt	Disable
WDT	Clear after master reset, WDT begins counting
Timer/Event Counter	Off
Input/Output ports	Input mode
Stack Pointer	Points to the top of the stack

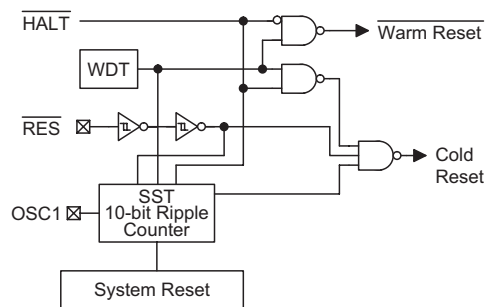


**Reset Circuit**

Note: "\*" Make the length of the wiring, which is connected to the  $\overline{\text{RES}}$  pin as short as possible, to avoid noise interference.



**Reset Timing Chart**



**Reset Configuration**

The registers states are summarized in the following table.

Register	Reset (Power On)	WDT Time-out (Normal Operation)	RES Reset (Normal Operation)	RES Reset (HALT)	WDT Time-out (HALT)*
TMR	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRC	00-0 1000	00-0 1000	00-0 1000	00-0 1000	uu-u uuuu
Program Counter	000H	000H	000H	000H	000H
MP	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu	-uuu uuuu
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	--xx xxxx	--uu uuuu	--uu uuuu	--uu uuuu	--uu uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu	--11 uuuu
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu
INTC1	---0 ---0	---0 ---0	---0 ---0	---0 ---0	---u ---u
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PB	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PBC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PC	---- --11	---- --11	---- --11	---- --11	---- --uu
PCC	---- --11	---- --11	---- --11	---- --11	---- --uu
PD	---- ---1	---- ---1	---- ---1	---- ---1	---- ---u
PDC	---- ---1	---- ---1	---- ---1	---- ---1	---- ---u
PWM	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
HADR	xxxx xxx-	xxxx xxx-	xxxx xxx-	xxxx xxx-	uuuu uu-
HCR	0--0 0---	0--0 0---	0--0 0---	0--0 0---	u--u u---
HSR	100- -0-1	100- -0-1	100- -0-1	100- -0-1	uuu- -u-u
HDR	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
ADRL	x--- ----	x--- ----	x--- ----	x--- ----	u--- ----
ADRH	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
ADCR	0100 0000	0100 0000	0100 0000	0100 0000	uuuu uuuu
ACSR	1--- --00	1--- --00	1--- --00	1--- --00	u--- --uu

Note: "\*" stands for warm reset  
 "u" stands for unchanged  
 "x" stands for unknown

### Timer/Event Counter

A timer/event counter (TMR) is implemented in the microcontroller. The timer/event counter contains an 8-bit programmable count-up counter and the clock may come from an external source or the system clock.

Using the internal system clock, there is only one reference time-base. The internal clock source comes from  $f_{SYS}$ . Using external clock input allows the user to count external events, measure time internals or pulse widths, or generate an accurate time base. While using the internal clock allows the user to generate an accurate time base.

There are two registers related to the timer/event counter; TMR ([0DH]), TMRC ([0EH]). Two physical registers are mapped to TMR location; writing TMR makes the starting value be placed in the timer/event counter preload register and reading TMR gets the contents of the timer/event counter. The TMRC is a timer/event counter control register, which defines some options.

The TM0, TM1 bits define the operating mode. The event count mode is used to count external events, which means the clock source comes from an external (TMR) pin. The timer mode functions as a normal timer with the clock source coming from the  $f_{INT}$  clock. The pulse width measurement mode can be used to count the high or low level duration of the external signal (TMR). The counting is based on the  $f_{INT}$ .

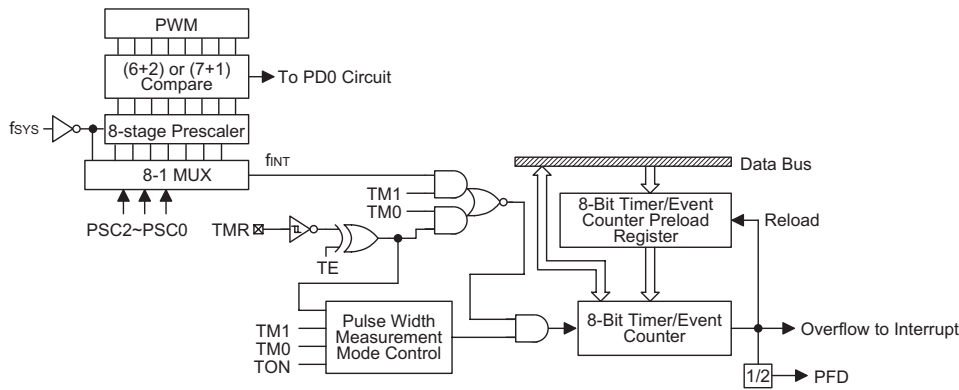
In the event count or timer mode, once the timer/event counter starts counting, it will count from the current contents in the timer/event counter to FFH. Once overflow occurs, the counter is reloaded from the timer/event counter preload register and generates the interrupt request flag (TF; bit 5 of INTC) at the same time.

In the pulse width measurement mode with the TON and TE bits equal to 1, once the TMR has received a transient from low to high (or high to low if the TE bits is "0") it will start counting until the TMR returns to the original level and resets the TON. The measured result will remain in the timer/event counter even if the activated transient occurs again. In other words, only 1 cycle measurement can be done. Until setting the TON, the cycle measurement will function again as long as it receives further transient pulse. Note that, in this operating mode, the timer/event counter starts counting not according to the logic level but according to the transient edges. In the case of counter overflows, the counter is reloaded from the timer/event counter preload register and issues the interrupt request just like the other two modes. To enable the counting operation, the timer ON bit (TON; bit 4 of TMRC) should be set to 1. In the pulse width measurement mode, the TON will be cleared automatically after the measurement cycle is completed. But in the other two modes the TON can only be reset by instructions. The overflow of the timer/event counter is one of the wake-up sources. No matter what the operation mode is, writing a 0 to ETI can disable the interrupt service.

Bit No.	Label	Function
0 1 2	PSC0 PSC1 PSC2	To define the prescaler stages, PSC2, PSC1, PSC0= 000: $f_{INT}=f_{SYS}$ 001: $f_{INT}=f_{SYS}/2$ 010: $f_{INT}=f_{SYS}/4$ 011: $f_{INT}=f_{SYS}/8$ 100: $f_{INT}=f_{SYS}/16$ 101: $f_{INT}=f_{SYS}/32$ 110: $f_{INT}=f_{SYS}/64$ 111: $f_{INT}=f_{SYS}/128$
3	TE	Defines the TMR active edge of the timer/event counter: In Event Counter Mode (TM1,TM0)=(0,1): 1:count on falling edge; 0:count on rising edge In Pulse Width measurement mode (TM1,TM0)=(1,1): 1: start counting on the rising edge, stop on the falling edge; 0: start counting on the falling edge, stop on the rising edge
4	TON	To enable or disable timer counting (0=disabled; 1=enabled)
5	—	Unused bit, read as "0"
6 7	TM0 TM1	To define the operating mode 01=Event count mode (external clock) 10=Timer mode (internal clock) 11=Pulse width measurement mode 00=Unused

**TMRC (0EH) Register**





Timer/Event Counter

In the case of timer/event counter OFF condition, writing data to the timer/event counter preload register will also reload that data to the timer/event counter. But if the timer/event counter is turned on, data written to it will only be kept in the timer/event counter preload register. The timer/event counter will still operate until overflow occurs. When the timer/event counter (reading TMR) is read, the clock will be blocked to avoid errors. As clock blocking may result in a counting error, this must be taken into consideration by the programmer.

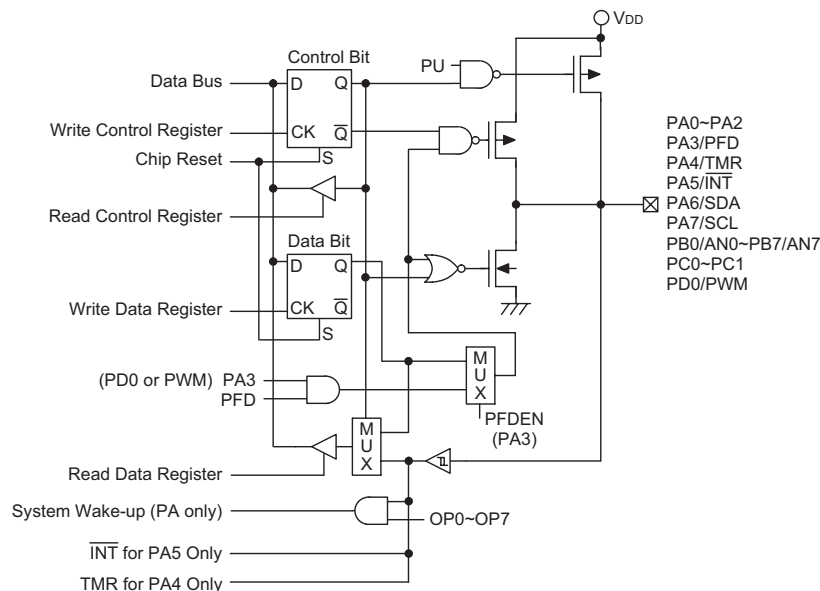
The bit0~bit2 of the TMRC can be used to define the pre-scaling stages of the internal clock sources of timer/event counter. The definitions are as shown. The overflow signal of timer/event counter can be used to generate the PFD signal.

### Input/Output Ports

There are 19 bidirectional input/output lines in the microcontroller, labeled as PA, PB, PC and PD, which are mapped to the data memory of [12H], [14H], [16H]

and [18H] respectively. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, that is, the inputs must be ready at the T2 rising edge of instruction "MOV A,[m]" (m=12H, 14H, 16H or 18H). For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Each I/O line has its own control register (PAC, PBC, PCC, PDC) to control the input/output configuration. With this control register, CMOS output or Schmitt trigger input with or without pull-high resistor structures can be reconfigured dynamically (i.e. on-the-fly) under software control. To function as an input, the corresponding latch of the control register must write "1". The input source also depends on the control register. If the control register bit is "1", the input will read the pad state. If the control register bit is "0", the contents of the latches will move to the internal bus. The latter is possible in the "read-modify-write" instruction.



Input/Output Ports



For output function, CMOS is the only configuration. These control registers are mapped to locations 13H, 15H, 17H and 19H.

After a chip reset, these input/output lines remain at high levels or floating state (dependent on pull-high options). Each bit of these input/output latches can be set or cleared by "SET [m].i" and "CLR [m].i" (m=12H, 14H, 16H or 18H) instructions.

Some instructions first input data and then follow the output operations. For example, "SET [m].i", "CLR [m].i", "CPL [m]", "CPLA [m]" read the entire port states into the CPU, execute the defined operations (bit-operation), and then write the results back to the latches or the accumulator.

Each line of port A has the capability of waking-up the device. The highest 6-bit of port C and 7-bit of port D are not physically implemented; on reading them a "0" is returned whereas writing then results in a no-operation. See Application note.

Each I/O port has a pull-high option. Once the pull-high option is selected, the I/O port has a pull-high resistor, otherwise, there's none. Take note that a non-pull-high I/O port operating in input mode will cause a floating state.

The PA3 is pin-shared with the PFD signal. If the PFD option is selected, the output signal in output mode of PA3 will be the PFD signal generated by timer/event counter overflow signal. The input mode always remaining its original functions. Once the PFD option is selected, the PFD output signal is controlled by PA3 data register only. Writing "1" to PA3 data register will enable the PFD output function and writing "0" will force the PA3 to remain at "0". The I/O functions of PA3 are shown below.

I/O Mode	I/P (Normal)	O/P (Normal)	I/P (PFD)	O/P (PFD)
PA3	Logical Input	Logical Output	Logical Input	PFD (Timer on)

Note: The PFD frequency is the timer/event counter overflow frequency divided by 2.

The PA5 and PA4 are pin-shared with INT and TMR pins respectively.

The PB can also be used as A/D converter inputs. The A/D function will be described later. There is a PWM function shared with PD0. If the PWM function is enabled, the PWM signal will appear on PD0 (if PD0 is operating in output mode). Writing "1" to PD0 data register will enable the PWM output function and writing "0" will force the PD0 to remain at "0". The I/O functions of PD0 is as shown.

I/O Mode	I/P (Normal)	O/P (Normal)	I/P (PWM)	O/P (PWM)
PD0	Logical Input	Logical Output	Logical Input	PWM

It is recommended that unused or not bonded out I/O lines should be set as output pins by software instruction to avoid consuming power under input floating state.

## PWM

The microcontroller provides 1 channels (6+2)/(7+1) (dependent on options) bits PWM output shared with PD0. The PWM channel has its data registers denoted as PWM(1AH). The frequency source of the PWM counter comes from  $f_{SYS}$ . The PWM registers is a 8-bit register. The waveforms of PWM outputs are as shown. Once the PD0 is selected as the PWM outputs and the output function of PD0 is enabled (PDC.0="0"), writing 1 to PD0 data register will enable the PWM output function and writing "0" will force the PD0 to stay at "0".

A (6+2) bits mode PWM cycle is divided into four modulation cycles (modulation cycle 0~modulation cycle 3). Each modulation cycle has 64 PWM input clock period. In a (6+2) bit PWM function, the contents of the PWM register is divided into two groups. Group 1 of the PWM register is denoted by DC which is the value of PWM.7~PWM.2. The group 2 is denoted by AC which is the value of PWM.1~PWM.0.

In a (6+2) bits mode PWM cycle, the duty cycle of each modulation cycle is shown in the table.

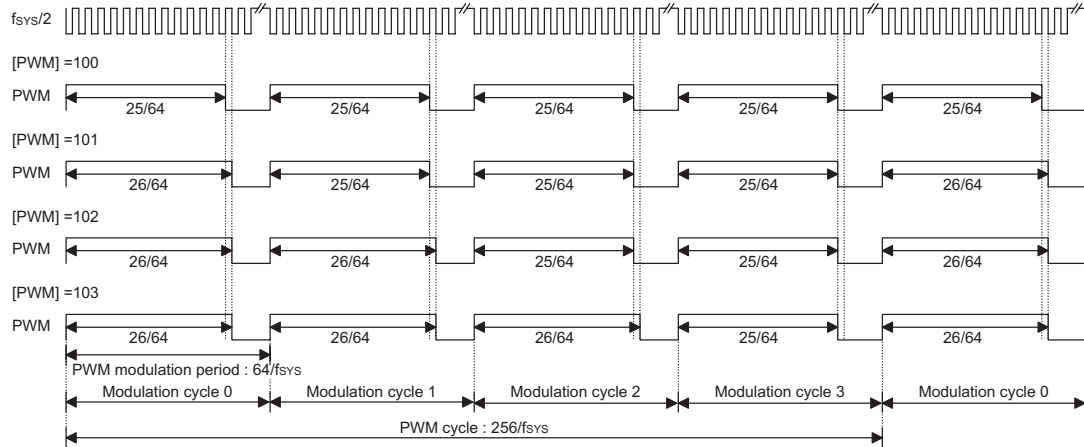
Parameter	AC (0~3)	Duty Cycle
Modulation cycle i (i=0~3)	i<AC	$\frac{DC + 1}{64}$
	i≥AC	$\frac{DC}{64}$

A (7+1) bits mode PWM cycle is divided into two modulation cycles (modulation cycle 0 ~ modulation cycle 1). Each modulation cycle has 128 PWM input clock period.

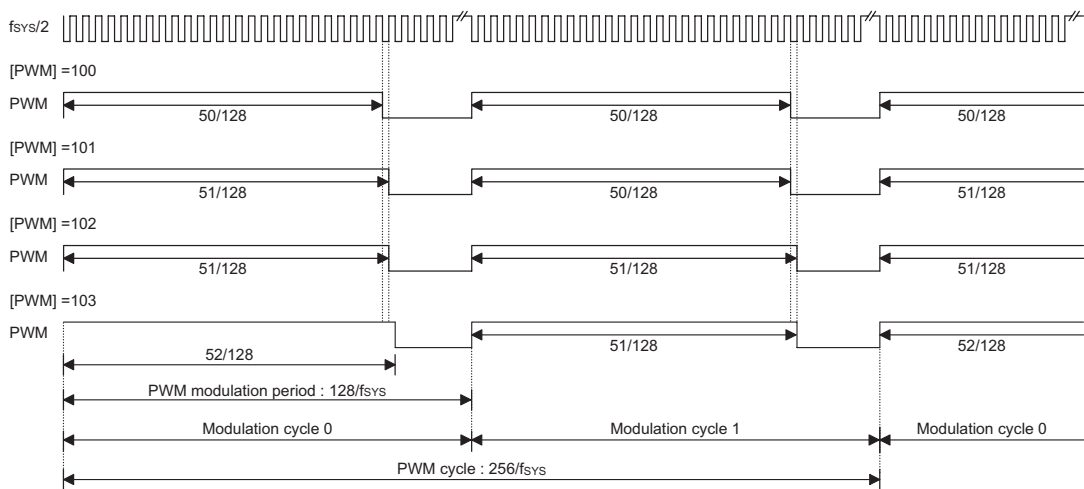
In a (7+1) bits PWM function, the contents of the PWM register is divided into two groups. Group 1 of the PWM register is denoted by DC which is the value of PWM.7~PWM.1. The group 2 is denoted by AC which is the value of PWM.0.

In a (7+1) bits mode PWM cycle, the duty cycle of each modulation cycle is shown in the table.

Parameter	AC (0~1)	Duty Cycle
Modulation cycle i (i=0~1)	i<AC	$\frac{DC + 1}{128}$
	i≥AC	$\frac{DC}{128}$



(6+2) PWM Mode



(7+1) PWM Mode

The modulation frequency, cycle frequency and cycle duty of the PWM output signal are summarized in the following table.

PWM Modulation Frequency	PWM Cycle Frequency	PWM Cycle Duty
$f_{SYS}/64$ for (6+2) bits mode $f_{SYS}/128$ for (7+1) bits mode	$f_{SYS}/256$	$[PWM]/256$

#### A/D Converter

The 8 channels and 9-bit resolution A/D converter are implemented in this microcontroller. The reference voltage is VDD. The A/D converter contains 4 special registers which are; ADRL (24H), ADRH (25H), ADCR (26H) and ACSR (27H). The ADRH and ADRL are A/D result register higher-order byte and lower-order byte and are read-only. After the A/D conversion is completed, the ADRH and ADRL should be read to get the conversion result data. The ADCR is an A/D converter control register, which defines the A/D channel number, analog

channel select, start A/D conversion control bit and the end of A/D conversion flag. If the users want to start an A/D conversion, define PB configuration, select the converted analog channel, and give START bit a raising edge and falling edge (0→1→0). At the end of A/D conversion, the EOCB bit is cleared and an A/D converter interrupt occurs (if the A/D converter interrupt is enabled). The ACSR is A/D clock setting register, which is used to select the A/D clock source.

The A/D converter control register is used to control the A/D converter. The bit2~bit0 of the ADCR are used to select an analog input channel. There are a total of eight channels to select. The bit5~bit3 of the ADCR are used to set PB configurations. PB can be an analog input or as digital I/O line decided by these 3 bits. Once a PB line is selected as an analog input, the I/O functions and pull-high resistor of this I/O line are disabled and the A/D converter circuit is power on. The EOCB bit (bit6 of the ADCR) is end of A/D conversion flag. Check this bit to know when A/D conversion is completed. The START

bit of the ADCR is used to begin the conversion of the A/D converter. Giving START bit a rising edge and falling edge means that the A/D conversion has started. In order to ensure the A/D conversion is completed, the START should remain at "0" until the EOCB is cleared to "0" (end of A/D conversion).

Bit No.	Label	Function
0 1	ADCS0 ADCS1	Selects the A/D converter clock source 00= system clock/2 01= system clock/8 10= system clock/32 11= undefined
2~6	—	Unused bit, read as "0"
7	TEST	For test mode used only

#### ACSR (27H) Register

Bit No.	Label	Function
0 1 2	ACS0 ACS1 ACS2	Defines the analog channel select.
3 4 5	PCR0 PCR1 PCR2	Defines the port B configuration select. If PCR0, PCR1 and PCR2 are all 0, the ADC circuit is power off to reduce power consumption
6	EOCB	Indicates end of A/D conversion. (0 = end of A/D conversion) Each time bits 3~5 change state the A/D should be initialized by issuing a START signal, otherwise the EOCB flag may have an undefined condition. See "Important note for A/D initialization".
7	START	Starts the A/D conversion. (0→1→0= start; 0→1= Reset A/D converter and set EOCB to "1")

#### ADCR (26H) Register

PCR2	PCR1	PCR0	7	6	5	4	3	2	1	0
0	0	0	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	1	PB7	PB6	PB5	PB4	PB3	PB2	PB1	AN0
0	1	0	PB7	PB6	PB5	PB4	PB3	PB2	AN1	AN0
0	1	1	PB7	PB6	PB5	PB4	PB3	AN2	AN1	AN0
1	0	0	PB7	PB6	PB5	PB4	AN3	AN2	AN1	AN0
1	0	1	PB7	PB6	PB5	AN4	AN3	AN2	AN1	AN0
1	1	0	PB7	PB6	AN5	AN4	AN3	AN2	AN1	AN0
1	1	1	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

#### Port B Configuration

ACS2	ACS1	ACS0	Analog Channel
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

#### Analog Input Channel Selection

Bit 7 of the ACSR register is used for test purposes only and must not be used for other purposes by the application program. Bit1 and bit0 of the ACSR register are used to select the A/D clock source.

When the A/D conversion has completed, the A/D interrupt request flag will be set. The EOCB bit is set to "1" when the START bit is set from "0" to "1".

Important Note for A/D initialization:

Special care must be taken to initialize the A/D converter each time the Port B A/D channel selection bits are modified, otherwise the EOCB flag may be in an undefined condition. An A/D initialization is implemented by setting the START bit high and then clearing it to zero within 10 instruction cycles of the Port B channel selection bits being modified. Note that if the Port B channel selection bits are all cleared to zero then an A/D initialization is not required.

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADRL	D0	—	—	—	—	—	—	—
ADRH	D8	D7	D6	D5	D4	D3	D2	D1

Note: D0~D8 is A/D conversion result data bit LSB~MSB.

#### ADRL (24H), ADRH (25H) Register

The following two programming examples illustrate how to setup and implement an A/D conversion. In the first example, the method of polling the EOCB bit in the ADCR register is used to detect when the conversion cycle is complete, whereas in the second example, the A/D interrupt is used to determine when the conversion is complete.

Example: using EOCB Polling Method to detect end of conversion

```

clr    EADI                ; disable ADC interrupt
mov    a,00000001B
mov    ACSR,a              ; setup the ACSR register to select fsys/8 as the A/D clock
mov    a,00100000B        ; setup ADCR register to configure Port PB0~PB3 as A/D inputs
mov    ADCR,a              ; and select AN0 to be connected to the A/D converter
:
:                          ; As the Port B channel bits have changed the following START
:                          ; signal (0-1-0) must be issued within 10 instruction cycles
:

```

Start\_conversion:

```

clr    START
set    START                ; reset A/D
clr    START                ; start A/D

```

Polling\_EOC:

```

sz     EOCB                ; poll the ADCR register EOCB bit to detect end of A/D conversion
jmp    polling_EOC         ; continue polling
mov    a,ADRH              ; read conversion result high byte value from the ADRH register
mov    adrh_buffer,a       ; save result to user defined memory
mov    a,ADRL              ; read conversion result low byte value from the ADRL register
mov    adrl_buffer,a       ; save result to user defined memory
:
:
jmp    start_conversion     ; start next A/D conversion

```

Example: using interrupt method to detect end of conversion

```

clr    EADI                ; disable ADC interrupt
mov    a,00000001B
mov    ACSR,a              ; setup the ACSR register to select fsys/8 as the A/D clock

mov    a,00100000B        ; setup ADCR register to configure Port PB0~PB3 as A/D inputs
mov    ADCR,a              ; and select AN0 to be connected to the A/D converter
:
:                          ; As the Port B channel bits have changed the following START

```

; signal (0-1-0) must be issued within 10 instruction cycles

Start\_conversion:

```

clr    START
set    START           ; reset A/D
clr    START           ; start A/D
clr    ADF             ; clear ADC interrupt request flag
set    EADI            ; enable ADC interrupt
set    EMI             ; enable global interrupt
:
:
:

```

; ADC interrupt service routine

ADC\_ISR:

```

mov    acc_stack,a     ; save ACC to user defined memory
mov    a,STATUS
mov    status_stack,a  ; save STATUS to user defined memory
:
:
:
mov    a,ADRH          ; read conversion result high byte value from the ADRH register
mov    adrh_buffer,a   ; save result to user defined register
mov    a,ADRL          ; read conversion result low byte value from the ADRL register
mov    adrl_buffer,a   ; save result to user defined register
clr    START
set    START           ; reset A/D
clr    START           ; start A/D
:
:
:

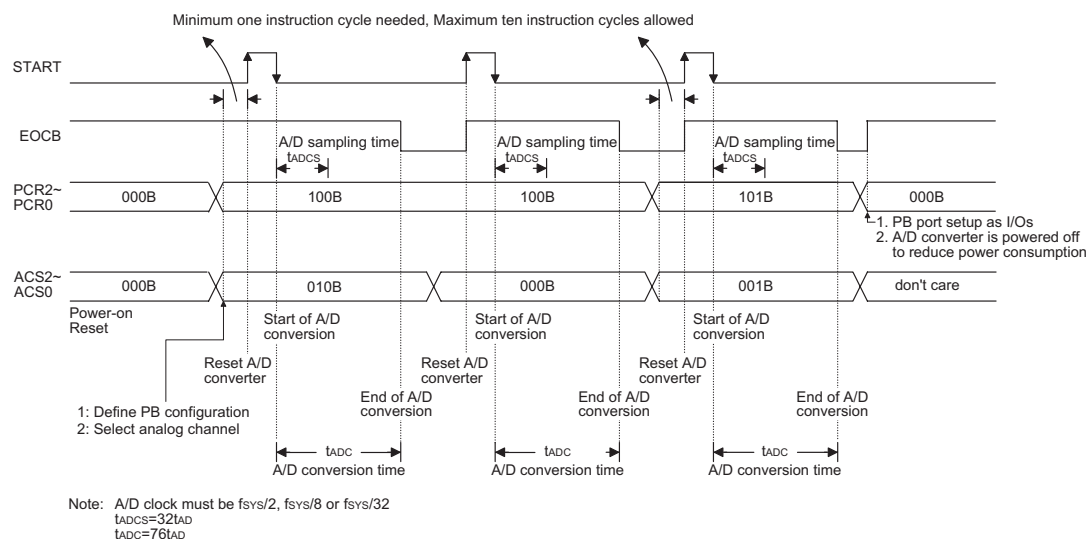
```

EXIT\_INT\_ISR:

```

mov    a,status_stack
mov    STATUS,a        ; restore STATUS from user defined memory
mov    a,acc_stack     ; restore ACC from user defined memory
reti

```



**A/D Conversion Timing**

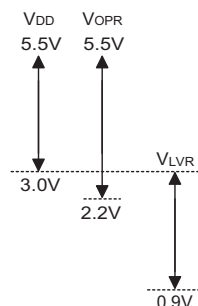
### Low Voltage Reset – LVR

The microcontroller provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V~3.3V, such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications:

- The low voltage (0.9V~ $V_{LVR}$ ) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
- The LVR uses the "OR" function with the external  $\overline{RES}$  signal to perform chip reset.

The relationship between  $V_{DD}$  and  $V_{LVR}$  is shown below.



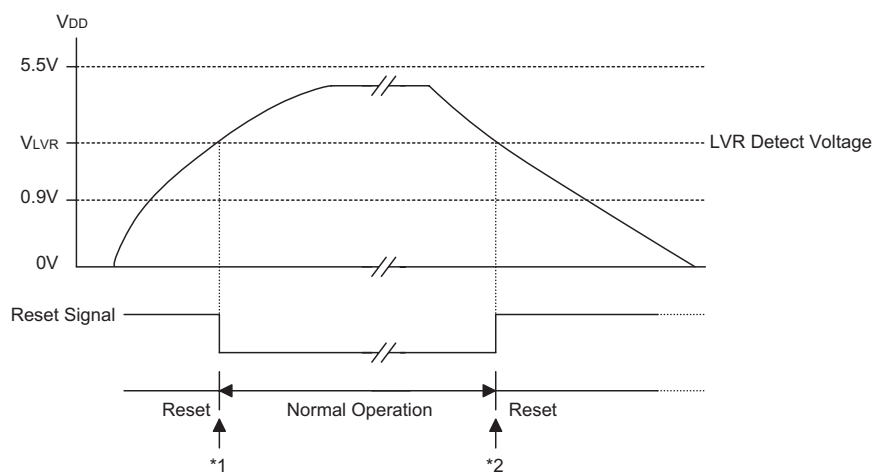
Note:  $V_{OPR}$  is the voltage range for proper chip operation at 4MHz system clock.

### I<sup>2</sup>C Bus Serial Interface

I<sup>2</sup>C Bus is implemented in the device. The I<sup>2</sup>C Bus is a bidirectional 2-wire lines. The data line and clock line are implement in SDA pin and SCL pin. The SDA and SCL are NMOS open drain output pin. They must connect a pull-high resistor respectively.

Using the I<sup>2</sup>C Bus, the device has two ways to transfer data. One is in slave transmit mode, the other is in slave receive mode. There are four registers related to I<sup>2</sup>C Bus; HADR([20H]), HCR([21H]), HSR([22H]), HDR([23H]). The HADR register is the slave address setting of the device, if the master sends the calling address which match, it means that this device is selected. The HCR is I<sup>2</sup>C Bus control register which defines the device enable or disable the I<sup>2</sup>C Bus as a transmitter or as a receiver. The HSR is I<sup>2</sup>C Bus status register, it responds with the I<sup>2</sup>C Bus status. The HDR is input/output data register, data to transmit or receive must be via the HDR register.

The I<sup>2</sup>C Bus control register contains three bits. The HEN bit define the enable or disable the I<sup>2</sup>C Bus. If the data wants transfer via I<sup>2</sup>C Bus, this bit must be set. The HTX bit defines whether the I<sup>2</sup>C Bus is in transmit or receive mode. If the device is as a transmitter, this bit must be set to "1". The TXAK defines the transmit acknowledge signal, when the device received 8-bit data, the device sends this bit to I<sup>2</sup>C Bus at the 9th clock. If the receiver wants to continue to receive the next data, this bit must be reset to "0" before receiving data.



### Low Voltage Reset

Note: \*1: To make sure that the system oscillator has stabilized, the SST provides an extra delay of 1024 system clock pulses before entering the normal operation.

\*2: Since low voltage state has to be maintained in its original state for over 1ms, therefore after 1ms delay, the device enters the reset mode.

The I<sup>2</sup>C Bus status register contains 5 bits. The HCF bit is reset to "0" when one data byte is being transferred. If one data transfer is completed, this bit is set to "1". The HAAS bit is set "1" when the address is match, and the I<sup>2</sup>C Bus interrupt request flag is set to "1". If the interrupt is enabled and the stack is not full, a subroutine call to location 10H will occur. Writing data to the I<sup>2</sup>C Bus control register clears HAAS bit. If the address is not match, this bit is reset to "0". The HBB bit is set to respond the I<sup>2</sup>C Bus is busy. It mean that a START signal is detected. This bit is reset to "0" when the I<sup>2</sup>C Bus is not busy. It means that a STOP signal is detected and the I<sup>2</sup>C Bus is free. The SRW bit defines the read/write command bit, if the calling address is match. When HAAS is set to "1", the device check SRW bit to determine whether the device is working in transmit or receive mode. When SRW bit is set "1", it means that the master wants to read data from I<sup>2</sup>C Bus, the slave device must write data to I<sup>2</sup>C Bus, so the slave device is working in transmit mode. When SRW is reset to "0", it means that the master wants to write data to I<sup>2</sup>C Bus, the slave device must read data from the bus, so the slave device is working in receive mode. The RXAK bit is reset "0" indicates an acknowledges signal has been received. In the transmit mode, the transmitter checks RXAK bit to know the receiver which wants to receive the next data byte, so the transmitter continue to write data to the I<sup>2</sup>C Bus until the RXAK bit is set to "1" and the transmitter releases the SDA line, so that the master can send the STOP signal to release the bus.

The HADR bit7~bit1 define the device slave address. At the beginning of transfer, the master must select a device by sending the address of the slave device. The bit 0 is unused and is not defined. If the I<sup>2</sup>C Bus receives a start signal, all slave device notice the continuity of the 8-bit data. The front of 7 bits is slave address and the first bit is MSB. If the address is match, the HAAS status bit is set and generate an I<sup>2</sup>C Bus interrupt. In the ISR, the slave device must check the HAAS bit to know the I<sup>2</sup>C Bus interrupt comes from the slave address that has match or completed one 8-bit data transfer. The last bit of the 8-bit data is read/write command bit, it responds in SRW bit. The slave will check the SRW bit to know if the master wants to transmit or receive data. The device check SRW bit to know it is as a transmitter or receiver.

Bit7~Bit1	Bit0
Slave Address	—

"—" means undefined

#### HADR (20H) Register

The HDR register is the I<sup>2</sup>C Bus input/output data register. Before transmitting data, the HDR must write the data which we want to transmit. Before receiving data, the device must dummy read data from HDR. Transmit or Receive data from I<sup>2</sup>C Bus must be via the HDR reg-

ister. At the beginning of the transfer of the I<sup>2</sup>C Bus, the device must initial the bus, the following are the notes for initialing the I<sup>2</sup>C Bus.

Note:

1: Write the I<sup>2</sup>C Bus address register (HADR) to define its own slave address.

2: Set HEN bit of I<sup>2</sup>C Bus control register (HCR) bit 0 to enable the I<sup>2</sup>C Bus.

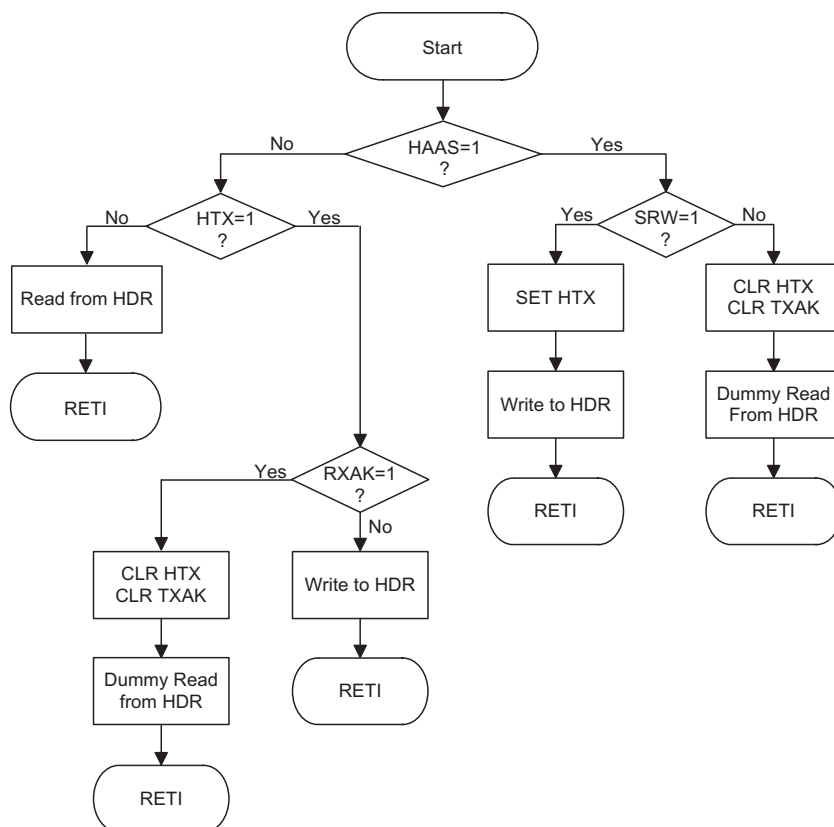
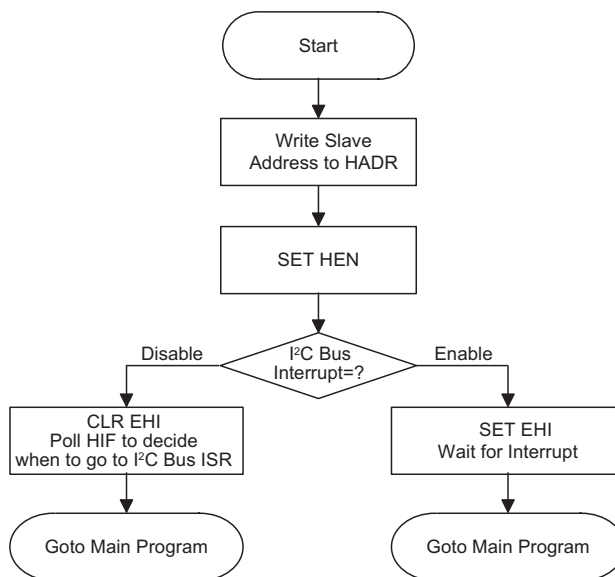
Bit No.	Label	Function
7	HEN	To enable or disable I <sup>2</sup> C Bus function (0= disable; 1= enable)
6~5	—	Unused bit, read as "0"
4	HTX	To define the transmit or receive mode (0= receive mode; 1= transmit)
3	TXAK	To enable or disable transmit acknowledge (0=acknowledge; 1=don't acknowledge)
2~0	—	Unused bit, read as "0"

#### HCR (21H) Register

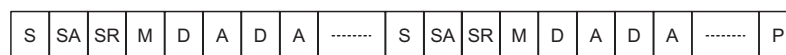
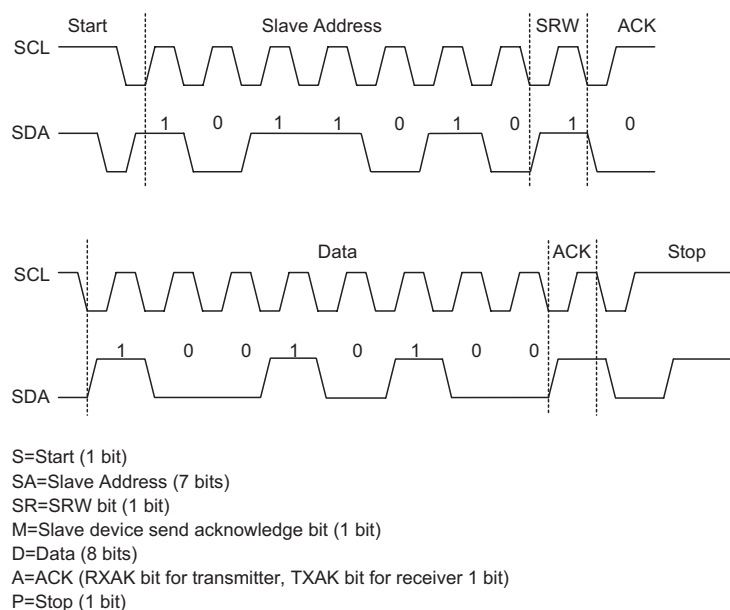
3: Set EHI bit of the interrupt control register 1 (INTC1) bit 0 to enable the I<sup>2</sup>C Bus interrupt.

Bit No.	Label	Function
7	HCF	HCF is clear to "0" when one data byte is being transferred, HCF is set to "1" indicating 8-bit data communication has been finished.
6	HAAS	HAAS is set to "1" when the calling address has matched, and I <sup>2</sup> C Bus interrupt will occur and HIF is set.
5	HBB	HBB is set to "1" when I <sup>2</sup> C Bus is busy and HBB is cleared to "0" means that the I <sup>2</sup> C Bus is not busy.
4~3	—	Unused bit, read as "0"
2	SRW	SRW is set to "1" when the master wants to read data from the I <sup>2</sup> C Bus, so the slave must transmit data to the master. SRW is cleared to "0" when the master wants to write data to the I <sup>2</sup> C Bus, so the slave must receive data from the master.
1	—	Unused bit, read as "0"
0	RXAK	RXAK is cleared to "0" when the master receives an 8-bit data and acknowledgment at the 9th clock, RXAK is set to "1" means not acknowledged.

#### HSR (22H) Register



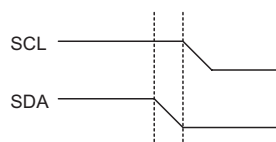




I<sup>2</sup>C Communication Timing Diagram

### Start Signal

The START signal is generated only by the master device. The other device in the bus must detect the START signal to set the I<sup>2</sup>C Bus busy bit (HBB). The START signal is SDA line from high to low, when SCL is high.



Start Bit

### Slave Address

The master must select a device for transferring the data by sending the slave device address after the START signal. All device in the I<sup>2</sup>C Bus will receive the I<sup>2</sup>C Bus slave address (7 bits) to compare with its own slave address (7 bits). If the slave address is matched, the slave device will generate an interrupt and save the following bit (8th bit) to SRW bit and sends an acknowledge bit (low level) to the 9th bit. The slave device also sets the status flag (HAAS), when the slave address is matched.

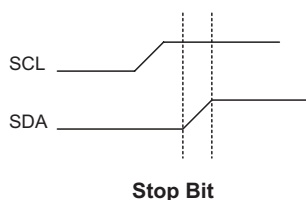
In interrupt subroutine, check HAAS bit to know whether the I<sup>2</sup>C Bus interrupt comes from a slave address that is matched or a data byte transfer is completed. When the slave address is matched, the device must be in transmit mode or receive mode and write data to HDR or dummy read from HDR to release the SCL line.

### SRW Bit

The SRW bit means that the master device wants to read from or write to the I<sup>2</sup>C Bus. The slave device check this bit to understand itself if it is a transmitter or a receiver. The SRW bit is set to "1" means that the master wants to read data from the I<sup>2</sup>C Bus, so the slave device must write data to a bus as a transmitter. The SRW is cleared to "0" means that the master wants to write data to the I<sup>2</sup>C Bus, so the slave device must read data from the I<sup>2</sup>C Bus as a receiver.

### Acknowledge Bit

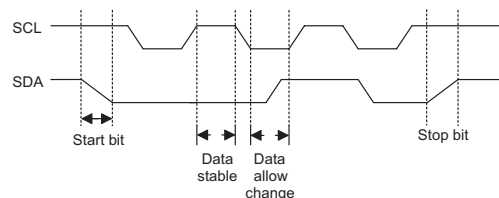
One of the slave device generates an acknowledge signal, when the slave address is matched. The master device can check this acknowledge bit to know if the slave device accepts the calling address. If no acknowledge bit, the master must send a STOP bit and end the communication. When the I<sup>2</sup>C Bus status register bit 6 HAAS is high, it means the address is matched, so the slave must check SRW as a transmitter (set HTX) to "1" or as a receiver (clear HTX) to "0".



### Data Byte

The data is 8 bits and is sent after the slave device has acknowledges the slave address. The first bit is MSB and the 8th bit is LSB. The receiver sends the acknowledge signal ("0") and continues to receive the next 1 byte data. If the transmitter checks and there's no acknowledge signal, then it release the SDA line, and the

master sends a STOP signal to release the I<sup>2</sup>C Bus. The data is stored in the HDR register. The transmitter must write data to the HDR before transmit data and the receiver must read data from the HDR after receiving data.



**Data Timing Diagram**

### Receive Acknowledge Bit

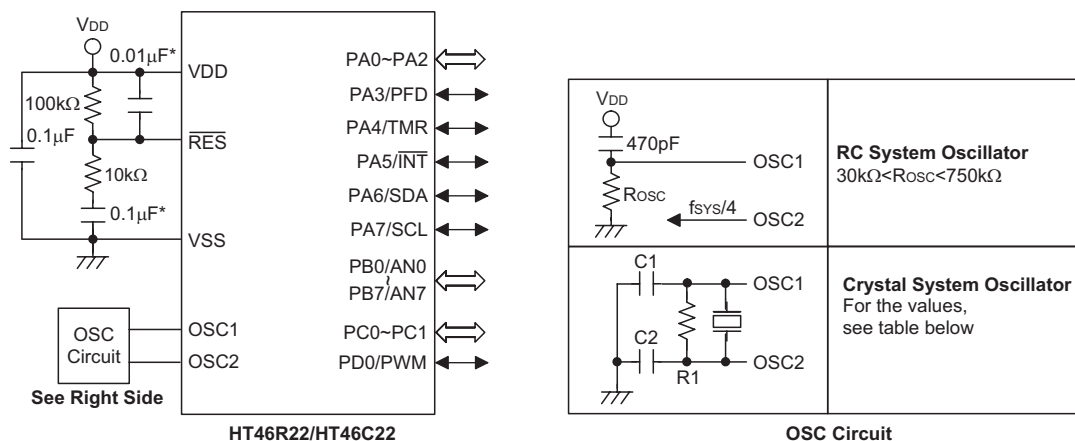
When the receiver wants to continue to receive the next data byte, it generates an acknowledge bit (TXAK) at the 9th clock. The transmitter checks the acknowledge bit (RXAK) to continue to write data to the I<sup>2</sup>C Bus or change to receive mode and dummy read the HDR register to release the SDA line and the master sends the STOP signal.

### Options

The following shows ten kinds of options in the microcontroller. ALL the options must be defined to ensure proper system function.

No.	Options
1	OSC type selection. This option is to decide if an RC or crystal oscillator is chosen as system clock.
2	WDT source selection. There are three types of selection: On-chip RC oscillator, instruction clock or disable the WDT.
3	CLRWDT times selection. This option defines how to clear the WDT by instruction. "One time" means that the CLR WDT instruction can clear the WDT. "Two times" means only if both of the CLR WDT1 and CLR WDT2 instructions have been executed, then WDT can be cleared.
4	Wake-up selection. This option defines the wake-up function activity. External I/O pins (PA only) all have the capability to wake-up the chip from a HALT.
5	Pull-high selection. This option is to decide whether a pull-high resistance is visible or not in the input mode of the I/O ports. PA0~PA7, can be independently selected.
6	PFD selection. PA3: Level output or PFD output
7	PWM selection: (7+1) or (6+2) mode PD0: Level output or PWM output
8	WDT time-out period selection. $2^{12}/f_S \sim 2^{13}/f_S$ , $2^{13}/f_S \sim 2^{14}/f_S$ , $2^{14}/f_S \sim 2^{15}/f_S$ , $2^{15}/f_S \sim 2^{16}/f_S$ .
9	Low voltage reset selection: Enable or disable LVR function.
10	I <sup>2</sup> C Bus function: Enable or disable

## Application Circuits



The following table shows the C1, C2 and R1 values corresponding to the different crystal values. (For reference only)

Crystal or Resonator	C1, C2	R1
4MHz Crystal	0pF	10kΩ
4MHz Resonator	10pF	12kΩ
3.58MHz Crystal	0pF	10kΩ
3.58MHz Resonator	25pF	10kΩ
2MHz Crystal & Resonator	25pF	10kΩ
1MHz Crystal	35pF	27kΩ
480kHz Resonator	300pF	9.1kΩ
455kHz Resonator	300pF	10kΩ
429kHz Resonator	300pF	10kΩ

The function of the resistor R1 is to ensure that the oscillator will switch off should low voltage conditions occur. Such a low voltage, as mentioned here, is one which is less than the lowest value of the MCU operating voltage. Note however that if the LVR is enabled then R1 can be removed.

**Note:** The resistance and capacitance for reset circuit should be designed in such a way as to ensure that the VDD is stable and remains within a valid operating voltage range before bringing RES to high.

\*\*\* Make the length of the wiring, which is connected to the RES pin as short as possible, to avoid noise interference.

## Instruction Set

### Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontrollers, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

### Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5µs and branch or call instructions would be implemented within 1µs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be "CLR PCL" or "MOV PCL, A". For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

### Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

### Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and

subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

### Logical and Rotate Operations

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application where rotate data operations are used is to implement multiplication and division calculations.

### Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction RET in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

### Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

### Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

### Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

### Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

Table conventions:

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
<b>Arithmetic</b>			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV
ADDM A,[m]	Add ACC to Data Memory	<sup>1</sup> Note	Z, C, AC, OV
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV
ADCM A,[m]	Add ACC to Data memory with Carry	<sup>1</sup> Note	Z, C, AC, OV
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	<sup>1</sup> Note	Z, C, AC, OV
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	<sup>1</sup> Note	Z, C, AC, OV
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	<sup>1</sup> Note	C
<b>Logic Operation</b>			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	<sup>1</sup> Note	Z
ORM A,[m]	Logical OR ACC to Data Memory	<sup>1</sup> Note	Z
XORM A,[m]	Logical XOR ACC to Data Memory	<sup>1</sup> Note	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	<sup>1</sup> Note	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
<b>Increment &amp; Decrement</b>			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	<sup>1</sup> Note	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	<sup>1</sup> Note	Z

Mnemonic	Description	Cycles	Flag Affected
<b>Rotate</b>			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	<sup>1</sup> Note	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	<sup>1</sup> Note	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	<sup>1</sup> Note	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	<sup>1</sup> Note	C
<b>Data Move</b>			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	<sup>1</sup> Note	None
MOV A,x	Move immediate data to ACC	1	None
<b>Bit Operation</b>			
CLR [m].i	Clear bit of Data Memory	<sup>1</sup> Note	None
SET [m].i	Set bit of Data Memory	<sup>1</sup> Note	None
<b>Branch</b>			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	<sup>1</sup> Note	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	<sup>1</sup> note	None
SZ [m].i	Skip if bit i of Data Memory is zero	<sup>1</sup> Note	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	<sup>1</sup> Note	None
SIZ [m]	Skip if increment Data Memory is zero	<sup>1</sup> Note	None
SDZ [m]	Skip if decrement Data Memory is zero	<sup>1</sup> Note	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	<sup>1</sup> Note	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	<sup>1</sup> Note	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
<b>Table Read</b>			
TABRDC [m]	Read table (current page) to TBLH and Data Memory	2 <sup>Note</sup>	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2 <sup>Note</sup>	None
<b>Miscellaneous</b>			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	<sup>1</sup> Note	None
SET [m]	Set Data Memory	<sup>1</sup> Note	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer	1	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	<sup>1</sup> Note	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.

2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.

3. For the "CLR WDT1" and "CLR WDT2" instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both "CLR WDT1" and "CLR WDT2" instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

## Instruction Definition

<b>ADC A,[m]</b>	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C
<b>ADCM A,[m]</b>	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C
<b>ADD A,[m]</b>	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C
<b>ADD A,x</b>	Add immediate data to ACC
Description	The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + x$
Affected flag(s)	OV, Z, AC, C
<b>ADDM A,[m]</b>	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C
<b>AND A,[m]</b>	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z
<b>AND A,x</b>	Logical AND immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } x$
Affected flag(s)	Z
<b>ANDM A,[m]</b>	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z

<b>CALL addr</b>	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack $\leftarrow$ Program Counter + 1 Program Counter $\leftarrow$ addr
Affected flag(s)	None
<b>CLR [m]</b>	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] $\leftarrow$ 00H
Affected flag(s)	None
<b>CLR [m].i</b>	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i $\leftarrow$ 0
Affected flag(s)	None
<b>CLR WDT</b>	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO $\leftarrow$ 0 PDF $\leftarrow$ 0
Affected flag(s)	TO, PDF
<b>CLR WDT1</b>	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repetitively executing this instruction without alternately executing CLR WDT2 will have no effect.
Operation	WDT cleared TO $\leftarrow$ 0 PDF $\leftarrow$ 0
Affected flag(s)	TO, PDF
<b>CLR WDT2</b>	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repetitively executing this instruction without alternately executing CLR WDT1 will have no effect.
Operation	WDT cleared TO $\leftarrow$ 0 PDF $\leftarrow$ 0
Affected flag(s)	TO, PDF



<b>CPL [m]</b>	Complement Data Memory
Description	Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	$[m] \leftarrow \overline{[m]}$
Affected flag(s)	Z
<b>CPLA [m]</b>	Complement Data Memory with result in ACC
Description	Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow \overline{[m]}$
Affected flag(s)	Z
<b>DAA [m]</b>	Decimal-Adjust ACC for addition with result in Data Memory
Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	$[m] \leftarrow ACC + 00H$ or $[m] \leftarrow ACC + 06H$ or $[m] \leftarrow ACC + 60H$ or $[m] \leftarrow ACC + 66H$
Affected flag(s)	C
<b>DEC [m]</b>	Decrement Data Memory
Description	Data in the specified Data Memory is decremented by 1.
Operation	$[m] \leftarrow [m] - 1$
Affected flag(s)	Z
<b>DECA [m]</b>	Decrement Data Memory with result in ACC
Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] - 1$
Affected flag(s)	Z
<b>HALT</b>	Enter power down mode
Description	This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.
Operation	$TO \leftarrow 0$ $PDF \leftarrow 1$
Affected flag(s)	TO, PDF

<b>INC [m]</b>	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	$[m] \leftarrow [m] + 1$
Affected flag(s)	Z
<b>INCA [m]</b>	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] + 1$
Affected flag(s)	Z
<b>JMP addr</b>	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	$Program\ Counter \leftarrow addr$
Affected flag(s)	None
<b>MOV A,[m]</b>	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	$ACC \leftarrow [m]$
Affected flag(s)	None
<b>MOV A,x</b>	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	$ACC \leftarrow x$
Affected flag(s)	None
<b>MOV [m],A</b>	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	$[m] \leftarrow ACC$
Affected flag(s)	None
<b>NOP</b>	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None
<b>OR A,[m]</b>	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "OR" } [m]$
Affected flag(s)	Z

<b>OR A,x</b>	Logical OR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "OR" } x$
Affected flag(s)	Z
<b>ORM A,[m]</b>	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \text{ "OR" } [m]$
Affected flag(s)	Z
<b>RET</b>	Return from subroutine
Description	The Program Counter is restored from the stack. Program execution continues at the restored address.
Operation	$\text{Program Counter} \leftarrow \text{Stack}$
Affected flag(s)	None
<b>RET A,x</b>	Return from subroutine and load immediate data to ACC
Description	The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.
Operation	$\text{Program Counter} \leftarrow \text{Stack}$ $ACC \leftarrow x$
Affected flag(s)	None
<b>RETI</b>	Return from interrupt
Description	The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.
Operation	$\text{Program Counter} \leftarrow \text{Stack}$ $EMI \leftarrow 1$
Affected flag(s)	None
<b>RL [m]</b>	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	$[m].(i+1) \leftarrow [m].i; (i = 0 \sim 6)$ $[m].0 \leftarrow [m].7$
Affected flag(s)	None
<b>RLA [m]</b>	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.(i+1) \leftarrow [m].i; (i = 0 \sim 6)$ $ACC.0 \leftarrow [m].7$
Affected flag(s)	None

<b>RLC [m]</b>	Rotate Data Memory left through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.
Operation	$[m].(i+1) \leftarrow [m].i; (i = 0 \sim 6)$ $[m].0 \leftarrow C$ $C \leftarrow [m].7$
Affected flag(s)	C
<b>RLCA [m]</b>	Rotate Data Memory left through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.(i+1) \leftarrow [m].i; (i = 0 \sim 6)$ $ACC.0 \leftarrow C$ $C \leftarrow [m].7$
Affected flag(s)	C
<b>RR [m]</b>	Rotate Data Memory right
Description	The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1); (i = 0 \sim 6)$ $[m].7 \leftarrow [m].0$
Affected flag(s)	None
<b>RRA [m]</b>	Rotate Data Memory right with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1); (i = 0 \sim 6)$ $ACC.7 \leftarrow [m].0$
Affected flag(s)	None
<b>RRC [m]</b>	Rotate Data Memory right through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1); (i = 0 \sim 6)$ $[m].7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C
<b>RRCA [m]</b>	Rotate Data Memory right through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1); (i = 0 \sim 6)$ $ACC.7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C

<b>SBC A,[m]</b>	Subtract Data Memory from ACC with Carry
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m] - \overline{C}$
Affected flag(s)	OV, Z, AC, C
<b>SBCM A,[m]</b>	Subtract Data Memory from ACC with Carry and result in Data Memory
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m] - \overline{C}$
Affected flag(s)	OV, Z, AC, C
<b>SDZ [m]</b>	Skip if decrement Data Memory is 0
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] - 1$ Skip if $[m] = 0$
Affected flag(s)	None
<b>SDZA [m]</b>	Skip if decrement Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] - 1$ Skip if $ACC = 0$
Affected flag(s)	None
<b>SET [m]</b>	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	$[m] \leftarrow FFH$
Affected flag(s)	None
<b>SET [m].i</b>	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	$[m].i \leftarrow 1$
Affected flag(s)	None

<b>SIZ [m]</b>	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] + 1$ Skip if $[m] = 0$
Affected flag(s)	None
<b>SIZA [m]</b>	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] + 1$ Skip if $ACC = 0$
Affected flag(s)	None
<b>SNZ [m].i</b>	Skip if bit i of Data Memory is not 0
Description	If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m].i \neq 0$
Affected flag(s)	None
<b>SUB A,[m]</b>	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C
<b>SUBM A,[m]</b>	Subtract Data Memory from ACC with result in Data Memory
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C
<b>SUB A,x</b>	Subtract immediate data from ACC
Description	The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - x$
Affected flag(s)	OV, Z, AC, C

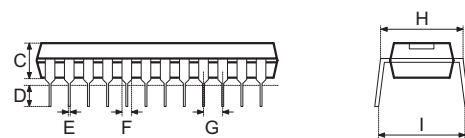
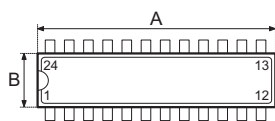
<b>SWAP [m]</b>	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	$[m].3 \sim [m].0 \leftrightarrow [m].7 \sim [m].4$
Affected flag(s)	None
<b>SWAPA [m]</b>	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC.3 \sim ACC.0 \leftarrow [m].7 \sim [m].4$ $ACC.7 \sim ACC.4 \leftarrow [m].3 \sim [m].0$
Affected flag(s)	None
<b>SZ [m]</b>	Skip if Data Memory is 0
Description	If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if $[m] = 0$
Affected flag(s)	None
<b>SZA [m]</b>	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m]$ Skip if $[m] = 0$
Affected flag(s)	None
<b>SZ [m].i</b>	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if $[m].i = 0$
Affected flag(s)	None
<b>TABRDC [m]</b>	Read table (current page) to TBLH and Data Memory
Description	The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	$[m] \leftarrow \text{program code (low byte)}$ $TBLH \leftarrow \text{program code (high byte)}$
Affected flag(s)	None
<b>TABRDL [m]</b>	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	$[m] \leftarrow \text{program code (low byte)}$ $TBLH \leftarrow \text{program code (high byte)}$
Affected flag(s)	None

<b>XOR A,[m]</b>	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "XOR" } [m]$
Affected flag(s)	Z
<b>XORM A,[m]</b>	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \text{ "XOR" } [m]$
Affected flag(s)	Z
<b>XOR A,x</b>	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "XOR" } x$
Affected flag(s)	Z

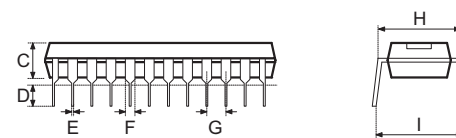
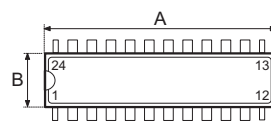


## Package Information

### 24-pin SKDIP (300mil) Outline Dimensions



**Fig1. Full Lead Packages**



**Fig2. 1/2 Lead Packages**

- MS-001d (see fig1)

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1230	—	1280
B	240	—	280
C	115	—	195
D	115	—	150
E	14	—	22
F	45	—	70
G	—	100	—
H	300	—	325
I	—	—	430

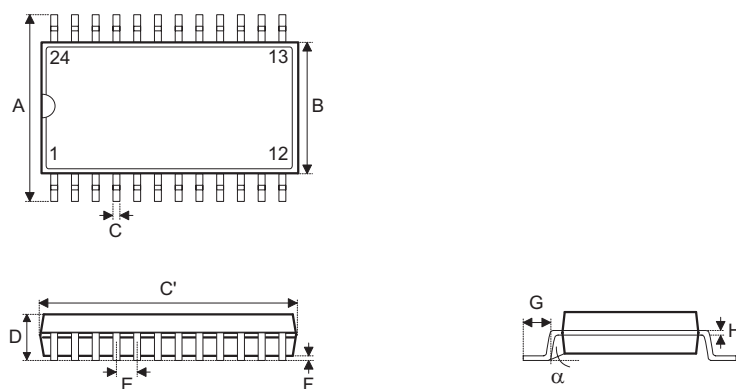
- MS-001d (see fig2)

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1160	—	1195
B	240	—	280
C	115	—	195
D	115	—	150
E	14	—	22
F	45	—	70
G	—	100	—
H	300	—	325
I	—	—	430

- MO-095a (see fig2)

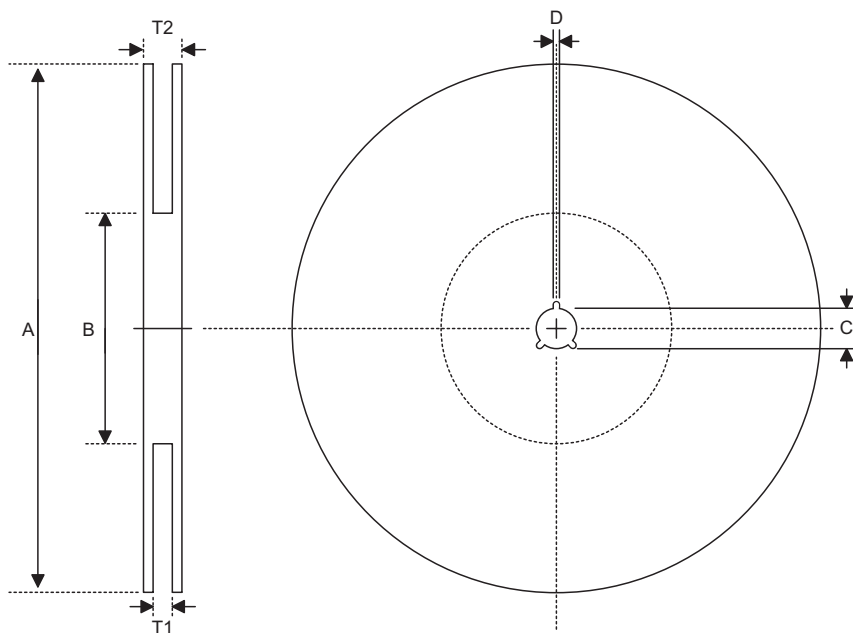
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1145	—	1185
B	275	—	295
C	120	—	150
D	110	—	150
E	14	—	22
F	45	—	60
G	—	100	—
H	300	—	325
I	—	—	430

**24-pin SOP (300mil) Outline Dimensions**

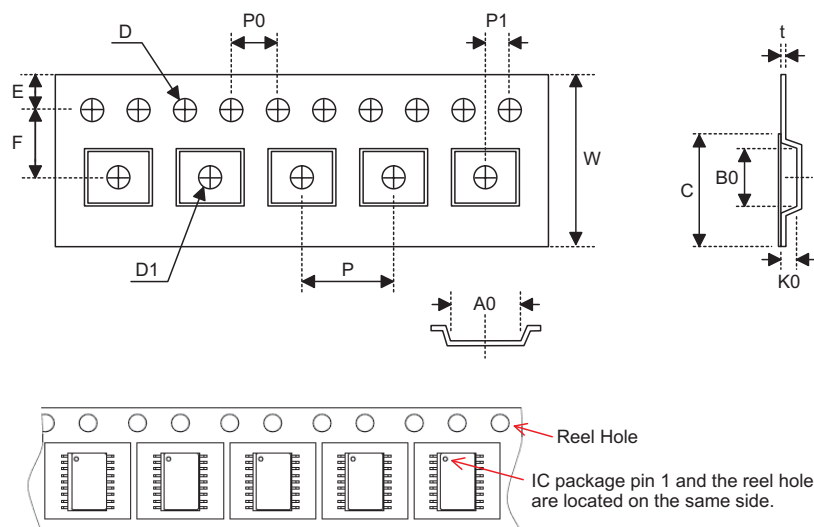


• MS-013

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	393	—	419
B	256	—	300
C	12	—	20
C'	598	—	613
D	—	—	104
E	—	50	—
F	4	—	12
G	16	—	50
H	8	—	13
$\alpha$	0°	—	8°

**Product Tape and Reel Specifications**
**Reel Dimensions**

**SOP 24W**

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 <sup>+0.5/-0.2</sup>
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8 <sup>+0.3/-0.2</sup>
T2	Reel Thickness	30.2±0.2

**Carrier Tape Dimensions**

**SOP 24W**

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.55 <sup>+0.10/-0.00</sup>
D1	Cavity Hole Diameter	1.50 <sup>+0.25/-0.00</sup>
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.9±0.1
B0	Cavity Width	15.9±0.1
K0	Cavity Depth	3.1±0.1
t	Carrier Tape Thickness	0.35±0.05
C	Cover Tape Width	21.3±0.1

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