**Ultrasonic Atomizer Flash MCU**

# HT45F3820

Revision: V1.11    Date: April 11, 2017

# Table of Contents

# Features

## CPU Features

- Operating Voltage:
    - $f_{SYS}$=12MHz: 2.7V ~ 5.5V
    - $f_{SYS}$=32kHz: 2.2V ~ 5.5V
- Up to 0.33μs instruction cycle with 12MHz system clock at $V_{DD}$=5V
- Power down and wake-up functions to reduce power consumption
- Oscillators:
    - Internal High Speed RC – HIRC
    - Internal Low Speed 32kHz RC – LIRC
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- All instructions executed in one or two instruction cycles
- Table read instructions
- 63 powerful instructions
- 4-level subroutine nesting
- Bit manipulation instruction

## Peripheral Features

- Flash Program Memory: 1K×16
- RAM Data Memory: 64×8
- True EEPROM Memory: 32×8
- Watchdog Timer function
- 8 bidirectional I/O lines
- Two pin-shared external interrupts
- Multiple Timer Modules for time measure, input capture, compare match output, PWM output function or single pulse output function
    - 10-bit PTM × 1
    - 10-bit STM × 1
- Over Current/Voltage Protection (OCVP) Function with interrupt
- Dual Time-Base functions for generation of fixed time interrupt signals
- Low voltage reset function
- Low voltage detect function
- Flash program memory can be re-programmed up to 100,000 times
- Flash program memory data retention > 10 years
- True EEPROM data memory can be re-programmed up to 1,000,000 times
- True EEPROM data memory data retention > 10 years
- Package Types: 8-pin SOP/10-pin SOP

## General Description

The HT45F3820 is a device dedicated for use in ultrasonic nebuliser applications. The application principle for ultrasonic nebulisers is to use electronic high-frequency oscillation and ceramic nebulising chip high-frequency resonance to break up the liquid water molecules thus generating a fine mist without requiring heating or any chemical substances. Compared with the heating nebulisation method, the ultrasonic method can result in 90% energy savings. Additionally, during the nebulisation process, it can release a large number of negative ions which can precipitate smoke and dust particles in air by electrostatic reaction and also can effectively remove formaldehyde, carbon monoxide, bacteria and other harmful substances thus generating cleaner air and reducing the possibility of disease transmission.

The device is a Flash Memory type 8-bit high performance RISC architecture microcontroller containing special internal circuitry for ultrasonic nebuliser applications. Offering users the convenience of Flash Memory multi-programming features, this device also includes a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of true EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc. Analog feature includes an over current/voltage protection function. Multiple and extremely flexible Timer Modules provide timing, pulse generation and PWM generation functions. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

The device also includes fully integrated low and high speed oscillators which can be flexibly used for different applications. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimise power consumption.

While the inclusion of flexible I/O programming features, Time-Base functions along with an adjustable ultrasonic nebuliser resonant frequency generator and many other features ensure that the device will find excellent use in different ultrasonic nebuliser applications.

This device can use the nebuliser resonance detector to detect the nebuliser resonant frequency, and use the nebuliser resonant frequency selection to output PFM resonant frequency for nebuliser control, it can also use the water shortage protection and OCVP functions for water shortage detection.

## Block Diagram



## Pin Assignment



**HT45F3820**
**8 SOP-A**



**HT45F3820**
**10 SOP-A**



**HT45V3820**
**16 SOP-A**
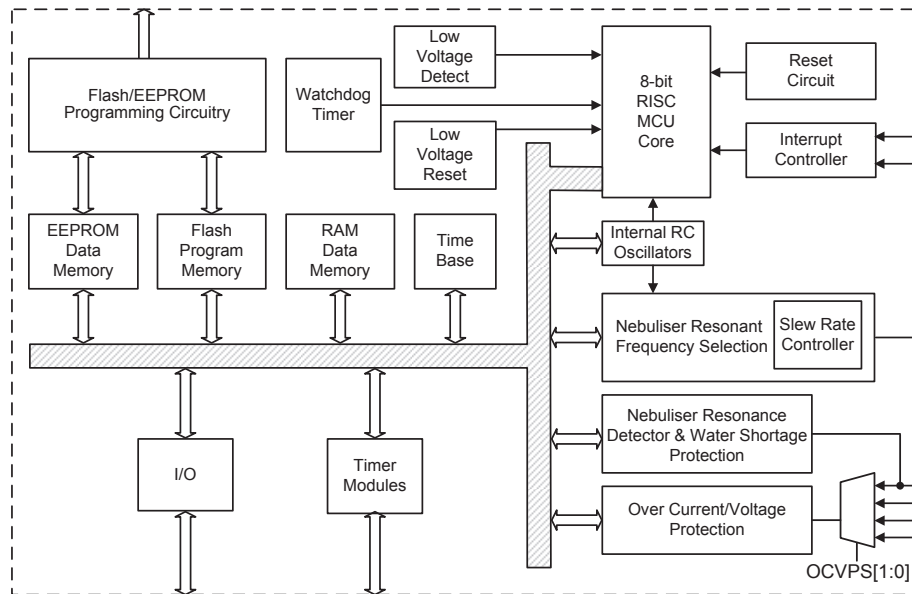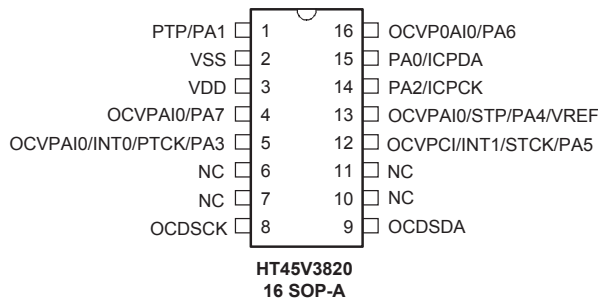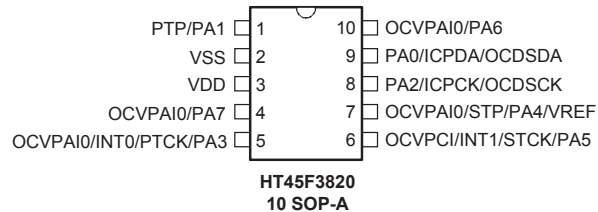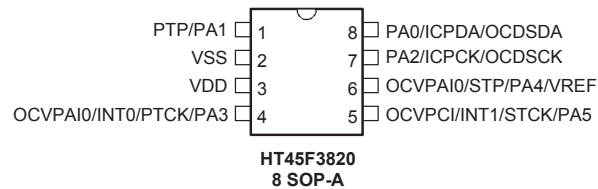
Note: 1. If the pin-shared pin functions have multiple output functions, the desired pin-shared function is determined using corresponding software control bits.

2. The actual device and its equivalent OCDS EV device share the same package type, however the OCDS EV device part number is HT45V3820. Pins OCDSCK and OCDSDA which are pin-shared with PA2 and PA0 are only used for the OCDS EV device.

## Pin Descriptions

With the exception of the power pins, all pins on this device can be referenced to by their Port name, e.g. PA0, PA1 etc, which refer to the digital I/O function of the pins. However these Port pins are also shared with other function such as Timer Module pins etc. The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

| Pin Name | Function | OPT | I/T | O/T | Description |
|---|---|---|---|---|---|
| PA0/ ICPDA/ OCDSDA | PA0 | PAPU PAWU | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | ICPDA | — | ST | CMOS | In-circuit programming data/address pin |
| | OCDSDA | — | ST | CMOS | On-chip debug support data/address pin, for EV chip only |
| PTP/PA1 | PA1 | PAPU PAWU CTRL3 | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | PTP | CTRL3 | ST | CMOS | PTM output |
| PA2/ ICPCK/ OCDSCK | PA2 | PAPU PAWU | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | ICPCK | — | ST | — | In-circuit programming clock pin |
| | OCDSCK | — | ST | — | On-chip debug support clock pin, for EV chip only |
| OCVPAI0/INT0/ PTCK/PA3 | PA3 | PAPU PAWU CTRL3 | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | OCVPAI0 | CTRL2 CTRL3 | ST | — | OCVPAI0 input path 0 |
| | INT0 | CTRL3 INTEG | ST | — | External interrupt 0 |
| | PTCK | CTRL3 PTMC0 | ST | — | PTM clock input |
| OCVPAI0/STP/ VREF/PA4 | PA4 | PAPU PAWU CTRL3 | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | STP | CTRL3 | ST | CMOS | STM output or capture input |
| | VREF | CTRL3 | AN | — | DAC Voltage reference |
| | OCVPAI0 | CTRL2 CTRL3 | ST | — | OCVPAI0 input path 0, nebuliser resonance detector & water shortage protection |
| OCVPCI/INT1/ STCK/PA5 | PA5 | PAPU PAWU CTRL3 | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | OCVPCI | CTRL3 | AN | — | Comparator non-inverted signal input |
| | INT1 | CTRL3 INTEG | ST | — | External interrupt 1 |
| | STCK | CTRL3 STMC0 | ST | — | STM clock input |
| OCVPAI0/PA6 | PA6 | PAPU PAWU | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | OCVPAI0 | CTRL2 CTRL3 | ST | — | OCVPAI0 input path 0 |
| OCVPAI0/PA7 | PA7 | PAPU PAWU | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | OCVPAI0 | CTRL2 CTRL3 | ST | — | OCVPAI0 input path 0 |

| Pin Name | Function | OPT | I/T | O/T | Description |
|----------|----------|-----|-----|-----|-------------|
| VDD | VDD | — | PWR | — | Positive power supply |
| VSS | VSS | — | PWR | — | Negative Power Supply |

Legend: I/T: Input type
O/T: Output type
OPT: Optional by register option
PWR: Power
ST: Schmitt Trigger input
CMOS: CMOS output

## Absolute Maximum Ratings

Supply Voltage ............................................................................ $V_{SS}$−0.3V to $V_{SS}$+6.0V

Input Voltage ............................................................................ $V_{SS}$−0.3V to $V_{DD}$+0.3V

Storage Temperature ........................................................................ -50°C to 125°C

Operating Temperature ...................................................................... -40°C to 85°C

$I_{OL}$ Total ............................................................................ 80mA

$I_{OH}$ Total ............................................................................ -80mA

Total Power Dissipation ...................................................................... 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect devices reliability.

## D.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|--------|-----------|-----|-----|------|------|------|------|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{DD}$ | Operating Voltage (HIRC) | — | $f_{SYS}=f_{HIRC}$=12MHz | 2.7 | — | 5.5 | V |
| | Operating Voltage (LIRC) | — | $f_{SYS}=f_{LIRC}$=32kHz | 2.2 | — | 5.5 | V |
| $I_{DD}$ | Operating Current (HIRC) | 3V | No load, all peripherals off, $f_{SYS}=f_{HIRC}$=12MHz | — | 2.2 | 3.3 | mA |
| | | 5V | | — | 5 | 7.5 | mA |
| | Operating Current (LIRC) | 3V | No load, all peripherals off, $f_{SYS}=f_{LIRC}$=32kHz | — | 10 | 20 | µA |
| | | 5V | | — | 30 | 50 | µA |
| $I_{STB}$ | Standby Current (SLEEP0 Mode) | 3V | No load, all peripherals off, WDT off | — | 0.2 | 0.8 | µA |
| | | 5V | | — | 0.5 | 1 | µA |
| | Standby Current (SLEEP1 Mode) | 3V | No load, all peripherals off, WDT on | — | 1.3 | 5 | µA |
| | | 5V | | — | 2.2 | 10 | µA |
| | Standby Current (IDLE0 Mode) | 3V | No load, all peripherals off, $f_{SUB}$ on | — | 1.3 | 3 | µA |
| | | 5V | | — | 2.2 | 5 | µA |
| | Standby Current (IDLE1 Mode, HIRC) | 3V | No load, all peripherals off, $f_{SUB}$ on, $f_{SYS}=f_{HIRC}$=12MHz | — | 0.6 | 1.2 | mA |
| | | 5V | | — | 1.2 | 2.4 | mA |
| $V_{IL}$ | Input Low Voltage for I/O Ports | 5V | — | 0 | — | 1.5 | V |
| | | — | — | 0 | — | 0.2 $V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage for I/O Ports | 5V | — | 3.5 | — | 5 | V |
| | | — | — | 0.8 $V_{DD}$ | — | $V_{DD}$ | V |

| Symbol | Parameter | Test Conditions VDD | Test Conditions Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{OL}$ | Sink Current for I/O Ports (PA7~PA2, PA0) | 3V | $V_{OL}$=0.1$V_{DD}$ | 16 | 32 | — | mA |
| | | 5V | $V_{OL}$=0.1$V_{DD}$ | 32 | 65 | — | mA |
| | Sink current for PA1 With Slew Rate Control | 3V | $V_{OL}$=0.2$V_{DD}$ | 24 | 60 | — | mA |
| | | 5V | $V_{OL}$=0.2$V_{DD}$ | 60 | 150 | — | mA |
| $I_{OH}$ | Source Current for I/O Ports (PA7~PA2, PA0) | 3V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=00B (m=0 or 2 or 4 or 6) | -0.7 | -1.5 | — | mA |
| | | 5V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=00B (m=0 or 2 or 4 or 6) | -1.5 | -2.9 | — | mA |
| | | 3V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=01B (m=0 or 2 or 4 or 6) | -1.3 | -2.5 | — | mA |
| | | 5V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=01B (m=0 or 2 or 4 or 6) | -2.5 | -5.1 | — | mA |
| | | 3V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=10B (m=0 or 2 or 4 or 6) | -1.8 | -3.6 | — | mA |
| | | 5V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=10B (m=0 or 2 or 4 or 6) | -3.6 | -7.3 | — | mA |
| | | 3V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=11B (m=0 or 2 or 4 or 6) | -4 | -8 | — | mA |
| | | 5V | $V_{OH}$=0.9$V_{DD}$, SLEDC[m+1, m]=11B (m=0 or 2 or 4 or 6) | -8 | -16 | — | mA |
| | Source current for PA1 With Slew Rate Control | 3V | $V_{OH}$=0.8$V_{DD}$ | -24 | -60 | — | mA |
| | | 5V | $V_{OH}$=0.8$V_{DD}$ | -60 | -150 | — | mA |
| $SR_{RISE}$ | Output Rising Edge Slew Rate for PA1 | 5V | SLEWC[m+1, m]=00B (m=0 or 2 or 4 or 6), 0.5V ~ 4.5V, $C_{LOAD}$=1000pF | 200 | — | — | V/μs |
| | | 5V | SLEWC[m+1, m]=01B (m=0 or 2 or 4 or 6), 0.5V ~ 4.5V, $C_{LOAD}$=1000pF | — | 60 | — | V/μs |
| | | 5V | SLEWC[m+1, m]=10B (m=0 or 2 or 4 or 6), 0.5V ~ 4.5V, $C_{LOAD}$=1000pF | — | 30 | — | V/μs |
| | | 5V | SLEWC[m+1, m]=11B (m=0 or 2 or 4 or 6), 0.5V ~ 4.5V, $C_{LOAD}$=1000pF | — | 15 | — | V/μs |
| $SR_{FALL}$ | Output Falling Edge Slew Rate for PA1 | 5V | SLEWC[m+1, m]=00B (m=0 or 2 or 4 or 6), 4.5V ~ 0.5V, $C_{LOAD}$=1000pF | 200 | — | — | V/μs |
| | | 5V | SLEWC[m+1, m]=01B (m=0 or 2 or 4 or 6), 4.5V ~ 0.5V, $C_{LOAD}$=1000pF | — | 60 | — | V/μs |
| | | 5V | SLEWC[m+1, m]=10B (m=0 or 2 or 4 or 6), 4.5V ~ 0.5V, $C_{LOAD}$=1000pF | — | 30 | — | V/μs |
| | | 5V | SLEWC[m+1, m]=11B (m=0 or 2 or 4 or 6), 4.5V ~ 0.5V, $C_{LOAD}$=1000pF | — | 15 | — | V/μs |
| $R_{PH}$ | Pull-high Resistance for I/O Ports | 3V | — | 20 | 60 | 100 | kΩ |
| | | 5V | — | 10 | 30 | 50 | kΩ |

## A.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | V$_{DD}$ | Conditions | | | | |
| f$_{SYS}$ | System Clock (HIRC) | 2.7V ~ 5.5V | f$_{SYS}$=f$_{HIRC}$=12MHz | — | 12 | — | MHz |
| | System Clock (LIRC) | 2.2V ~ 5.5V | f$_{SYS}$=f$_{LIRC}$=32kHz | — | 32 | — | kHz |
| f$_{HIRC}$ | High Speed Internal RC Oscillator (HIRC) | 3V | Ta=25°C | -2% | 12 | +2% | MHz |
| | | 5V | Ta=25°C | -2% | 12 | +2% | MHz |
| | | 2.7V ~ 5.5V | Ta=25°C | -5% | 12 | +5% | MHz |
| | | 3V | Ta=0°C ~ 70°C | - 7% | 12 | +7% | MHz |
| | | 5V | Ta=0°C ~ 70°C | - 7% | 12 | +7% | MHz |
| | | 3V | Ta= -40°C ~ 85°C | -10% | 12 | +10% | MHz |
| | | 5V | Ta= -40°C ~ 85°C | -7% | 12 | +7% | MHz |
| | | 2.7V ~ 5.5V | Ta=0°C ~ 70°C | -7% | 12 | +7% | MHz |
| | | 2.7V ~ 5.5V | Ta= -40°C ~ 85°C | -10% | 12 | +10% | MHz |
| f$_{LIRC}$ | Low Speed Internal RC Oscillator (LIRC) | 3V | Ta=25°C | -10% | 32 | +10% | kHz |
| | | 3V ± 0.3V | Ta= -40°C ~ 85°C | -40% | 32 | +40% | kHz |
| | | 2.2V ~ 5.5V | Ta= -40°C ~ 85°C | -50% | 32 | +60% | kHz |
| | | 5V | Ta=25°C | -10% | 32 | +10% | kHz |
| | | 5V ± 0.5V | Ta= -40°C ~ 85°C | -40% | 32 | +40% | kHz |
| | | 2.2V ~ 5.5V | Ta= -40°C ~ 85°C | -50% | 32 | +50% | kHz |
| t$_{INT}$ | External Interrupt Minimum Pulse Width | — | — | 1 | 3.3 | 5 | µs |
| t$_{EERD}$ | EEPROM Read Time | — | — | — | 2 | 4 | t$_{SYS}$ |
| t$_{EEWR}$ | EEPROM Write Time | — | — | — | 2 | 4 | ms |
| t$_{RSTD}$ | System Reset Delay Time (Power-on Reset, LVR Hardware Reset, LVR Software Reset, WDT Software Reset) | — | — | 25 | 50 | 100 | ms |
| | System reset delay time (WDT Time-out Hardware Cold Reset) | — | — | 8.3 | 16.7 | 33.3 | ms |
| t$_{SST}$ | System Start-up Timer Period (Wake-up from Power Down Mode and f$_{SYS}$ off) | — | f$_{SYS}$=f$_H$ ~ f$_H$ / 64, f$_H$=f$_{HIRC}$ | 16 | — | — | t$_{HIRC}$ |
| | | — | f$_{SYS}$=f$_{SUB}$=f$_{LIRC}$ | 2 | — | — | t$_{LIRC}$ |
| | System Start-up Timer Period (Slow Mode ↔ Normal Mode) | — | f$_{HIRC}$ off → on (HTO=1) | 16 | — | — | t$_{HIRC}$ |
| | System Start-up Timer Period (Wake-up from Power Down Mode and f$_{SYS}$ on) | — | f$_{SYS}$=f$_{HIRC}$ ~ f$_{HIRC}$ /64 | 2 | — | — | t$_H$ |
| | | — | f$_{SYS}$=f$_{LIRC}$ | 2 | — | — | t$_{SUB}$ |
| | System Start-up Timer Period (WDT Time-out Hardware Cold Reset) | — | — | 0 | — | — | t$_H$ |

Note: 1. t$_{SYS}$=1/f$_{SYS}$; t$_{SUB}$=1/f$_{SUB}$; t$_{HIRC}$=1/f$_{HIRC}$

2. To maintain the accuracy of the internal HIRC oscillator frequency, a 0.1µF decoupling capacitor should be connected between VDD and VSS and located as close to the device as possible.

3. Frequency accuracy (trim at V$_{DD}$=3V/5V, FADJH=01H, FADJL=00H).

## LVD & LVR Electrical Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{LVR}$ | Low Voltage Reset Voltage | — | LVR enable, 2.1V | -5% | 2.1 | +5% | V |
| | | | LVR enable, 2.55V | | 2.55 | | V |
| | | | LVR enable, 3.15V | | 3.15 | | V |
| | | | LVR enable, 3.8V | | 3.8 | | V |
| $V_{LVD}$ | Low Voltage Detector Voltage | — | LVDEN=1, $V_{LVD}$=2.0V | -5% | 2.0 | +5% | V |
| | | — | LVDEN=1, $V_{LVD}$=2.2V | | 2.2 | | V |
| | | — | LVDEN=1, $V_{LVD}$=2.4V | | 2.4 | | V |
| | | — | LVDEN=1, $V_{LVD}$=2.7V | | 2.7 | | V |
| | | — | LVDEN=1, $V_{LVD}$=3.0V | | 3.0 | | V |
| | | — | LVDEN=1, $V_{LVD}$=3.3V | | 3.3 | | V |
| | | — | LVDEN=1, $V_{LVD}$=3.6V | | 3.6 | | V |
| | | — | LVDEN=1, $V_{LVD}$=4.0V | | 4.0 | | V |
| $I_{LVR}$ | Additional PowerConsumption if LVR is used | 5V±3% | LVR disable → LVR enable | — | 60 | 90 | µA |
| $I_{LVD}$ | Additional PowerConsumption if LVD is used | 5V±3% | LVD disable → LVD enable (LVR disable) | — | 75 | 115 | µA |
| | | | LVD disable → LVD enable (LVR enable) | — | 60 | 90 | µA |
| $t_{LVR}$ | LVR Minimum Low Voltage Width to Reset | — | — | 120 | 240 | 480 | µs |
| $t_{LVD}$ | LVD Minimum Low Voltage Width to Interrupt | — | — | 60 | 120 | 240 | µs |
| $t_{LVDS}$ | LVDO Stable Time | — | For LVR enable, LVD off → on | — | — | 15 | µs |
| | | — | For LVR disable, LVD off → on | — | — | 150 | µs |
| $t_{SRESET}$ | Software Reset Width to Reset | — | — | 45 | 90 | 120 | µs |

Note: $V_{LVR}$ or $V_{LVD}$ is the MCU operating voltage level under which a LVR reset or LVD interrupt occurs.

## Over Current / Voltage Protection Electrical Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $I_{OCVP}$ | Operating Current | 3V | DAC $V_{REF}$=2.5V | — | — | 1250 | µA |
| | | 5V | | — | 730 | 1250 | µA |
| $V_{OS\_CMP}$ | Comparator Input Offset Voltage | 3V | Without calibration (OCVPCOF[4:0]=10000B) | -15 | — | 15 | mV |
| | | 5V | Without calibration (OCVPCOF[4:0]=10000B) | -15 | — | 15 | mV |
| | | 3V | With calibration | -4 | — | 4 | mV |
| | | 5V | With calibration | -4 | — | 4 | mV |
| $V_{HYS}$ | Hysteresis | 3V | — | 20 | 40 | 60 | mV |
| | | 5V | — | 20 | 40 | 60 | mV |
| $V_{CM\_CMP}$ | Comparator Common Mode Voltage Range | 3V | — | $V_{SS}$ | — | $V_{DD}$ - 1.4 | V |
| | | 5V | — | $V_{SS}$ | — | $V_{DD}$ - 1.4 | V |
| $V_{OS\_OPA}$ | OPA Input Offset Voltage | 3V | Without calibration (OCVPOOF[5:0]=100000B) | -15 | — | 15 | mV |
| | | 5V | Without calibration (OCVPOOF[5:0]=100000B) | -15 | — | 15 | mV |
| | | 3V | With calibration | -4 | — | 4 | mV |
| | | 5V | With calibration | -4 | — | 4 | mV |
| $V_{CM\_OPA}$ | OPA Common Mode Voltage Range | 3V | — | $V_{SS}$ | — | $V_{DD}$ - 1.4 | V |
| | | 5V | — | $V_{SS}$ | — | $V_{DD}$ - 1.4 | V |
| $V_{OR}$ | OPA Maximum Output Voltage Range | 3V | — | $V_{SS}$ + 0.1 | — | $V_{DD}$ - 0.1 | V |
| | | 5V | — | $V_{SS}$ + 0.1 | — | $V_{DD}$ - 0.1 | V |
| Ga | PGA Gain Accuracy | 3V/ 5V | In non-inverting mode, R2/R1≤50, using internal resistor, and input voltage > 80mV | -5 | — | 5 | % |
| | | | In non-inverting mode, R2/R1=65 or 80 , using internal resistor, and input voltage > 50mV | -8 | — | 8 | % |
| | | | In non-inverting mode, R2/R1=130, using internal resistor, and input voltage > 35mV | -10 | — | 10 | % |
| | | | In inverting mode, R2/R1≤50, using internal resistor, and input voltage < -80mV | -5 | — | 5 | % |
| | | | In inverting mode, R2/R1=65 or 80, using internal resistor, and input voltage < -50mV | -8 | — | 8 | % |
| | | | In inverting mode, R2/R1=130, using internal resistor, and input voltage < -35mV | -10 | — | 10 | % |
| DNL | Differential Non-linearity | 3V | DAC $V_{REF}=V_{DD}$ | — | — | ±2 | LSB |
| | | 5V | DAC $V_{REF}=V_{DD}$ | — | — | ±1 | LSB |
| INL | Integral Non-linearity | 3V | DAC $V_{REF}=V_{DD}$ | — | — | ±2 | LSB |
| | | 5V | DAC $V_{REF}=V_{DD}$ | — | — | ±1.5 | LSB |

## Power on Reset Electrical Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{POR}$ | $V_{DD}$ Start Voltage to Ensure Power-on Reset | — | — | — | — | 100 | mV |
| $RR_{POR}$ | $V_{DD}$ Rising Rate to Ensure Power-on Reset | — | — | 0.035 | — | — | V/ms |
| $t_{POR}$ | Minimum Time for $V_{DD}$ Stays at $V_{POR}$ to Ensure Power-on Reset | — | — | 1 | — | — | ms |
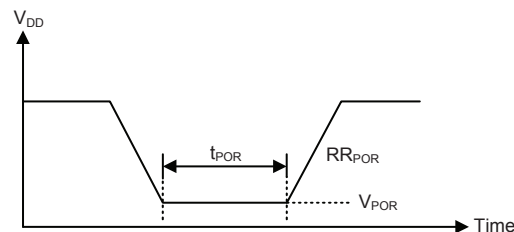


## System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The device takes advantage of the usual features found within RISC microcontrollers providing increased speed of operation and Periodic performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O control system with maximum reliability and flexibility. This makes the device suitable for low-cost, high-volume production for controller applications.

### Clocking and Pipelining

The main system clock, derived from either an HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.
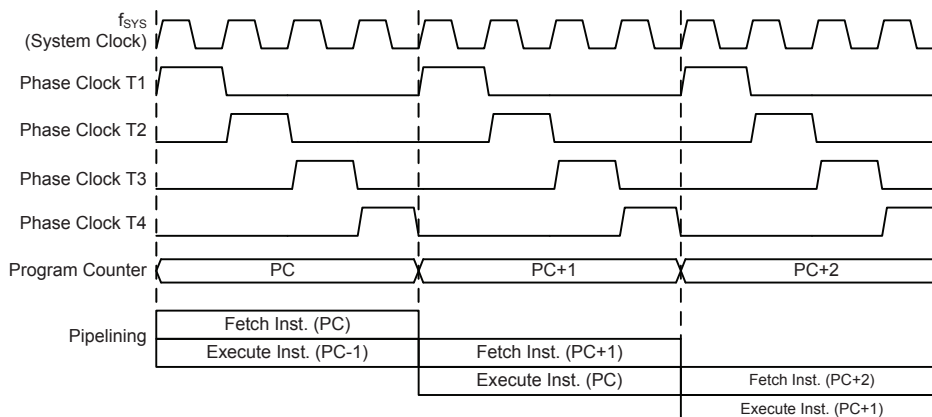
**System Clock and Pipelining**

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.
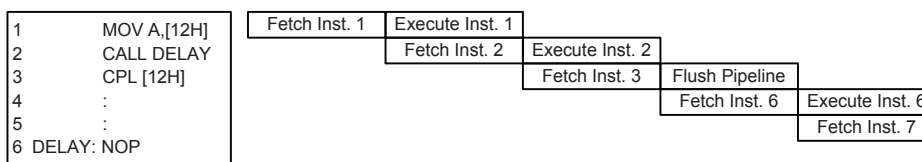


**Instruction Fetching**

## Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demand a jump to a non-consecutive Program Memory address. Only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by the application program.

When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

| Program Counter | |
|---|---|
| **Program Counter High byte** | **PCL Register** |
| PC9~PC8 | PCL7~PCL0 |

The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly, however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted. Manipulating the PCL register may cause program branching, so an extra cycle is needed to pre-fetch.

**Stack**

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack is neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.

If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching. If the stack is overflow, the first Program Counter save in the stack will be lost.
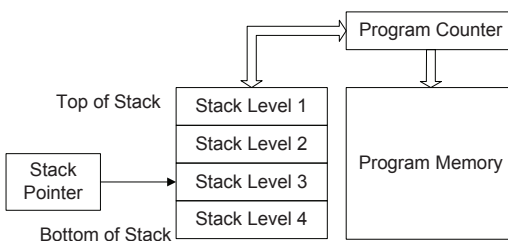


**Arithmetic and Logic Unit – ALU**

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

• Arithmetic operations: ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA

• Logic operations: AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA

• Rotation: RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC

• Increment and Decrement: INCA, INC, DECA, DEC

• Branch decision: JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI

# Flash Program Memory

The Program Memory is the location where the user code or program is stored. For this device the Program Memory is Flash type, which means it can be programmed and re-programmed a large number of times, allowing the user the convenience of code modification on the same device. By using the appropriate programming tools, this Flash device offers users the flexibility to conveniently debug and develop their applications while also offering a means of field programming and updating.

## Structure

The Program Memory has a capacity of 1K×16 bits. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by a separate table pointer register.

## Special Vectors

Within the Program Memory, certain locations are reserved for the reset and interrupts. The location 000H is reserved for use by the device reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.

| 000H | Reset |
|------|-------|
| 004H | Interrupt Vector |
| 024H | |
| 3FFH | 16 bits |
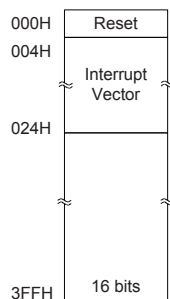
**Program Memory Structure**

## Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the address of the look up data to be retrieved in the table pointer register, TBLP and TBHP. These registers define the total address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the Program Memory using the "TABRD[m]" or "TABRDL[m]" instructions, respectively. When the instruction is executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register. Any unused bits in this transferred higher order byte will be read as "0".

The accompanying diagram illustrates the addressing data flow of the look-up table.

### Table Program Example

The following example shows how the table pointer and table data is defined and retrieved from the microcontroller. This example uses raw table data located in the Program Memory which is stored there using th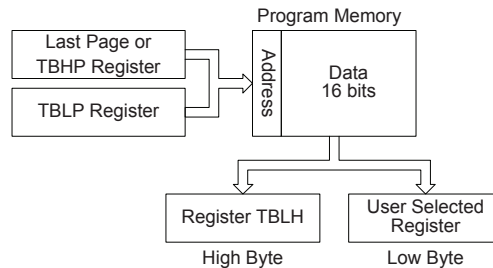e ORG statement. The value at this ORG statement is "300H" which refers to the start address of the last page within the 1K words Program Memory of the device. The table pointer is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "306H" or 6 locations after the start of the TBHP specified page. Note that the value for the table pointer is referenced to the first address specified by the TBHP and TBLP registers if the "TABRD [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRD [m]" instruction is executed.

Because the TBLH register is a read-only register and cannot be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of the TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

#### Table Read Program Example

```
tempreg1 db ?      ; temporary register #1
tempreg2 db ?      ; temporary register #2
:
mov a,06h          ; initialise low table pointer-note that this address is referenced
mov tblp,a         ; to the last page or specific page
mov a,03h          ; initialise high table pointer
mov tbhp,a
:
tabrd tempreg1     ; transfers value in table referenced by table pointer
                   ; data at program memory address "306H" transferred to tempreg1 and TBLH
dec tblp           ; reduce value of table pointer by one
tabrd tempreg2     ; transfers value in table referenced by table pointer
                   ; data at program memory address "305H" transferred to tempreg2 and TBLH
                   ; in this example the data "1AH" is transferred to tempreg1 and data "0FH" to
                   ; register tempreg2, the value 00H will be transferred to the high byte
                   ; register TBLH
:
org 300h           ; sets initial address of program memory
dc 00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
:
```

### In Circuit Programming

The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device. As an additional convenience, Holtek has provided a means of programming the microcontroller in-circuit using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the device.

The Holtek Flash MCU to Writer Programming Pin correspondence table is as follows:

| Holtek Write Pins | MCU Programming Pins | Function |
|---|---|---|
| ICPDA | PA0 | Programming Serial Data/Address |
| ICPCK | PA2 | Programming Clock |
| VDD | VDD | Power Supply |
| VSS | VSS | Ground |

The Program Memory and EEPROM data memory can both be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply. The technical details regarding the in-circuit programming of the device are beyond the scope of this document and will be supplied in supplementary literature.

During the programming process, the user must take care of the ICPDA and ICPCK pins for data and clock programming purpose to ensure that no other outputs are connected to these two pins.
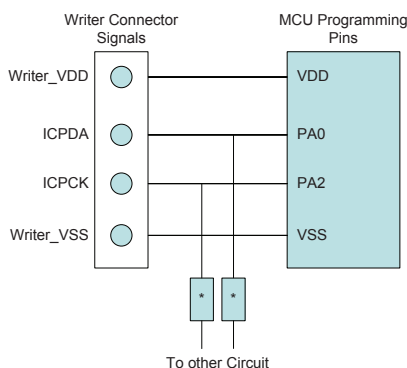


Note: * may be resistor or capacitor. The resistance of * must be greater than 1kΩ or the capacitance of * must be less than 1nF.

### On-Chip Debug Support – OCDS

The device has an EV chip named HT45V3820 which is used to emulate the HT45F3820 device. This EV chip device also provides an "On-Chip Debug" function to debug the real MCU device during the development process. The EV chip and the real MCU device are almost functionally compatible except for the "On-Chip Debug" function. Users can use the EV chip device to emulate the real chip device behavior by connecting the OCDSDA and OCDSCK pins to the Holtek HT-IDE development tools. The OCDSDA pin is the OCDS Data/Address input/output pin while the OCDSCK pin is the OCDS clock input pin. When users use the EV chip for debugging, other functions which are shared with the OCDSDA and OCDSCK pins in the device will have no effect in the EV chip. However, the two OCDS pins which are pin-shared with the ICP programming pins are still used as the Flash Memory programming pins for ICP. For more detailed OCDS information, refer to the corresponding document named "Holtek e-Link for 8-bit MCU OCDS User's Guide".

| Holtek e-Link Pins | EV Chip Pins | Pin Description |
|---|---|---|
| OCDSDA | OCDSDA | On-chip Debug Support Data/Address input/output |
| OCDSCK | OCDSCK | On-chip Debug Support Clock input |
| VDD | VDD | Power Supply |
| GND | VSS | Ground |

## RAM Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored.

### Structure

Divided into two sections, the first of these is an area of RAM, known as the Special Purpose Data Memory. Here are located registers which are necessary for correct operation of the device. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of Data Memory is known as the General Purpose Data Memory, which is reserved for general purpose use. All locations within this area are read and write accessible under program control.

The overall Data Memory is subdivided into two banks. The Special Purpose Data Memory registers are accessible in all banks, with the exception of the EEC register at address 40H, which is only accessible in Bank 1. Switching between the different Data Memory banks is achieved by setting the Bank Pointer to the correct value. The start address of the Data Memory for the device is the address 00H.

| Special Purpose Data Memory | General Purpose Data Memory | |
|---|---|---|
| Address | Capacity | Address |
| Bank 0: 00H~7FH<br>Bank 1: 00H~7FH | 64×8 | Bank 0: 80H~BFH |



**Data Memory Structure**
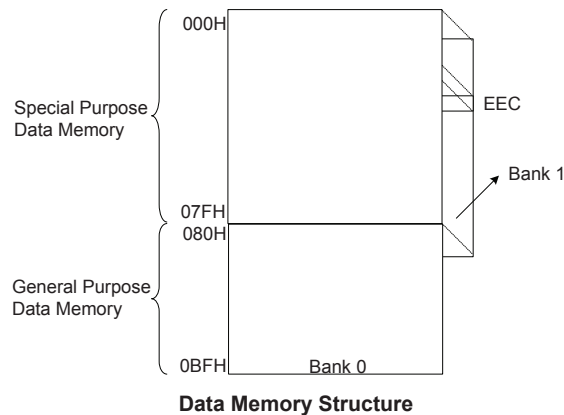
### General Purpose Data Memory

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user programing for both reading and writing operations. By using the bit operation instructions individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory.

## Special Purpose Data Memory

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writeable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value "00H".

| Bank 0, 1 | | | Bank 0 | Bank 1 |
|---|---|---|---|---|
| 00H | IAR0 | 35H | Unused | |
| 01H | MP0 | 36H | Unused | |
| 02H | IAR1 | 37H | Unused | |
| 03H | MP1 | 38H | Unused | |
| 04H | BP | 39H | CTRL2 | |
| 05H | ACC | 3AH | CTRL3 | |
| 06H | PCL | 3BH | | |
| 07H | TBLP | 3CH | | |
| 08H | TBLH | 3DH | Unused | |
| 09H | TBHP | 3EH | | |
| 0AH | STATUS | 3FH | | |
| 0BH | SMOD | 40H | Unused | EEC |
| 0CH | LVDC | 41H | Unused | |
| 0DH | INTEG | 42H | Unused | |
| 0EH | INTC0 | 43H | SLEWC | |
| 0FH | INTC1 | 44H | SLEDC | |
| 10H | INTC2 | 45H | Unused | |
| 11H | Unused | 46H | PTMC0 | |
| 12H | MFI0 | 47H | PTMC1 | |
| 13H | MFI1 | 48H | PTMDL | |
| 14H | PA | 49H | PTMDH | |
| 15H | PAC | 4AH | PTMAL | |
| 16H | PAPU | 4BH | PTMAH | |
| 17H | PAWU | 4CH | PTMRPL | |
| 18H | MFI2 | 4DH | PTMRPH | |
| 19H | Unused | 4EH | | |
| 1AH | WDTC | 4FH | | |
| 1BH | TBC | 50H | | |
| 1CH | Unused | 51H | | |
| 1DH | Unused | 52H | | |
| 1EH | EEA | 53H | | |
| 1FH | EED | 54H | Unused | |
| 20H | Unused | 55H | | |
| 21H | Unused | 56H | | |
| 22H | Unused | 57H | | |
| 23H | Unused | 58H | | |
| 24H | FADJL | 59H | | |
| 25H | FADJH | 5AH | | |
| 26H | CTRL | 5BH | OCVPC0 | |
| 27H | LVRC | 5CH | OCVPC1 | |
| 28H | Unused | 5DH | OCVPC2 | |
| 29H | Unused | 5EH | OCVPDA | |
| 2AH | Unused | 5FH | OCVPOCAL | |
| 2BH | Unused | 60H | OCVPCCAL | |
| 2CH | Unused | 61H | | |
| 2DH | Unused | | | |
| 2EH | Unused | | | |
| 2FH | STMC0 | | Unused | |
| 30H | STMC1 | | | |
| 31H | STMDL | | | |
| 32H | STMDH | | | |
| 33H | STMAL | | | |
| 34H | STMAH | 7FH | | |

☐ : Unused, read as 00H

**Special Purpose Data Memory Structure**

## Special Function Register Description

Most of the Special Function Register details will be described in the relevant functional section. However, several registers require a separate description in this section.

### Indirect Addressing Registers – IAR0, IAR1

The Indirect Addressing Registers, IAR0 and IAR1, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0 and IAR1 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointers, MP0 or MP1. Acting as a pair, IAR0 and MP0 can together access data from Bank 0 while the IAR1 and MP1 register pair can access data from any bank. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers indirectly will return a result of "00H" and writing to the registers indirectly will result in no operation.

### Memory Pointers – MP0, MP1

Two Memory Pointers, known as MP0 and MP1 are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to is the address specified by the related Memory Pointer. MP0, together with Indirect Addressing Register, IAR0, are used to access data from Bank 0, while MP1 and IAR1 are used to access data from all banks according to BP register. Direct Addressing can only be used within Bank 0, all other Banks must be addressed indirectly using MP1 and IAR1.

The following example shows how to clear a section of four Data Memory locations already defined as locations adres1 to adres4.

#### Indirect Addressing Program Example

```
data .section ´data´
adres1   db ?
adres2   db ?
adres3   db ?
adres4   db ?
block    db ?
code .section at 0 ´code´
org 00h
start:
     mov a,04h             ; setup size of block
     mov block,a
     mov a,offset adres1   ; Accumulator loaded with first RAM address
     mov mp0,a             ; setup memory pointer with first RAM address
loop:
     clr IAR0              ; clear the data at address defined by mp0
     inc mp0              ; increment memory pointer
     sdz block            ; check if last memory location has been cleared
     jmp loop
continue:
```

The important point to note here is that in the example shown above, no reference is made to specific Data Memory addresses.

**Bank Pointer – BP**

For this device, the Data Memory is divided into two banks, Bank0 and Bank1. Selecting the required Data Memory area is achieved using the Bank Pointer. Bit 0 of the Bank Pointer is used to select Data Memory Bank 0 or 1.

The Data Memory is initialised to Bank 0 after a reset, except for a WDT time-out reset in the Power down Mode, in which case, the Data Memory bank remains unaffected. It should be noted that the Special Purpose Data Memory is not affected by the bank selection, which means that the Special Function Registers can be accessed from within any bank. Directly addressing the Data Memory will always result in Bank 0 being accessed irrespective of the value of the Bank Pointer. Accessing data from Bank1 must be implemented using Indirect Addressing.

**BP Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | DMBP0 |
| R/W | — | — | — | — | — | — | — | R/W |
| POR | — | — | — | — | — | — | — | 0 |

Bit 7 ~ 1    Unimplemented, read as "0"

Bit 0    **DMBP0**: Select Data Memory Banks
    0: Bank 0
    1: Bank 1

**Accumulator – ACC**

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user-defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

**Program Counter Low Register – PCL**

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

### Look-up Table Registers – TBLP, TBHP, TBLH

These three special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP and TBHP are the table pointers and indicate the location where the table data is located. Their value must be setup before any table read commands are executed. Their value can be changed, for example using the "INC" or "DEC" instruction, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

### Status Register – STATUS

This 8-bit register contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the "CLR WDT" or "HALT" instruction. The PDF flag is affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

• C is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.

• AC is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.

• Z is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.

• OV is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.

• PDF is cleared by a system power-up or executing the "CLR WDT" instruction. PDF is set by executing the "HALT" instruction.

• TO is cleared by a system power-up or executing the "CLR WDT" or "HALT" instruction. TO is set by a WDT time-out.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the subroutine can corrupt the status register, precautions must be taken to correctly save it.

**STATUS Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | TO | PDF | OV | Z | AC | C |
| R/W | — | — | R | R | R/W | R/W | R/W | R/W |
| POR | — | — | 0 | 0 | x | x | x | x |

"x" unknown

Bit 7~6    Unimplemented, read as "0"

Bit 5    **TO**: Watchdog Time-out flag
　　　　0: After power up or executing the "CLR WDT" or "HALT" instruction
　　　　1: A watchdog time-out occurred.

Bit 4    **PDF**: Power down flag
　　　　0: After power up or executing the "CLR WDT" instruction
　　　　1: By executing the "HALT" instruction

Bit 3    **OV**: Overflow flag
　　　　0: No overflow
　　　　1: An operation results in a carry into the highest-order bit but not a carry out of the highest-order bit or vice versa.

Bit 2    **Z**: Zero flag
　　　　0: The result of an arithmetic or logical operation is not zero
　　　　1: The result of an arithmetic or logical operation is zero

Bit 1    **AC**: Auxiliary flag
　　　　0: No auxiliary carry
　　　　1: An operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction

Bit 0    **C**: Carry flag
　　　　0: No carry-out
　　　　1: An operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation
　　　C is also affected by a rotate through carry instruction.

## EEPROM Data Memory

One of the special features in the device is its internal EEPROM Data Memory. EEPROM, which stands for Electrically Erasable Programmable Read Only Memory, is by its nature a non-volatile form of memory, with data retention even when its power supply is removed. By incorporating this kind of data memory, a whole new host of application possibilities are made available to the designer. The availability of EEPROM storage allows information such as product identification numbers, calibration values, specific user data, system setup data or other product information to be stored directly within the product microcontroller. The process of reading and writing data to the EEPROM memory has been reduced to a very trivial affair.

### EEPROM Data Memory Structure

The EEPROM Data Memory capacity is up to 32×8 bits. Unlike the Program Memory and RAM Data Memory, the EEPROM Data Memory is not directly mapped and is therefore not directly accessible in the same way as the other types of memory. Read and Write operations to the EEPROM are carried out in single byte operations using an address and data register in Bank 0 and a single control register in Bank 1.

### EEPROM Registers

Three registers control the overall operation of the internal EEPROM Data Memory. These are the address register, EEA, the data register, EED and a single control register, EEC. As both the EEA and EED registers are located in Bank 0, they can be directly accessed in the same way as any other Special Function Register. The EEC register however, being located in Bank 1, cannot be directly addressed directly and can only be read from or written to indirectly using the MP1 Memory Pointer and Indirect Addressing Register, IAR1. Because the EEC control register is located at address 40H in Bank 1, the MP1 Memory Pointer must first be set to the value 40H and the Bank Pointer register, BP, set to the value, 01H, before any operations on the EEC register are executed.

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EEA | — | — | — | D4 | D3 | D2 | D1 | D0 |
| EED | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| EEC | — | — | — | — | WREN | WR | RDEN | RD |

EEPROM Control Register List

### EEA Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | D4 | D3 | D2 | D1 | D0 |
| R/W | — | — | — | R/W | R/W | R/W | R/W | R/W |
| POR | — | — | — | 0 | 0 | 0 | 0 | 0 |

Bit 7 ~ 5    Unimplemented, read as "0"

Bit 4 ~ 0    Data EEPROM address
Data EEPROM address bit 4 ~ bit 0

**EED Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 ~ 0    Data EEPROM data
                Data EEPROM data bit 7 ~ bit 0

**EEC Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|-----|-----|------|-----|------|-----|
| Name | — | — | — | — | WREN | WR | RDEN | RD |
| R/W | — | — | — | — | R/W | R/W | R/W | R/W |
| POR | — | — | — | — | 0 | 0 | 0 | 0 |

Bit 7 ~ 4    Unimplemented, read as "0"

Bit 3        **WREN**: Data EEPROM Write Enable
                0: Disable
                1: Enable
                This is the Data EEPROM Write Enable Bit which must be set high before Data EEPROM write operations are carried out. Clearing this bit to zero will inhibit Data EEPROM write operations.

Bit 2        **WR**: EEPROM Write Control
                0: Write cycle has finished
                1: Activate a write cycle
                This is the Data EEPROM Write Control Bit and when set high by the application program will activate a write cycle. This bit will be automatically reset to zero by the hardware after the write cycle has finished. Setting this bit high will have no effect if the WREN has not first been set high.

Bit 1        **RDEN**: Data EEPROM Read Enable
                0: Disable
                1: Enable
                This is the Data EEPROM Read Enable Bit which must be set high before Data EEPROM read operations are carried out. Clearing this bit to zero will inhibit Data EEPROM read operations.

Bit 0        **RD**: EEPROM Read Control
                0: Read cycle has finished
                1: Activate a read cycle
                This is the Data EEPROM Read Control Bit and when set high by the application program will activate a read cycle. This bit will be automatically reset to zero by the hardware after the read cycle has finished. Setting this bit high will have no effect if the RDEN has not first been set high.

Note:  The WREN, WR, RDEN and RD cannot be set to "1" at the same time in one instruction. The WR and RD cannot be set to "1" at the same time.

### Reading Data from the EEPROM

To read data from the EEPROM, the read enable bit, RDEN, in the EEC register must first be set high to enable the read function. The EEPROM address of the data to be read must then be placed in the EEA register. If the RD bit in the EEC register is now set high, a read cycle will be initiated. Setting the RD bit high will not initiate a read operation if the RDEN bit has not been set. When the read cycle terminates, the RD bit will be automatically cleared to zero, after which the data can be read from the EED register. The data will remain in the EED register until another read or write operation is executed. The application program can poll the RD bit to determine when the data is valid for reading.

### Writing Data to the EEPROM

The EEPROM address of the data to be written must first be placed in the EEA register and the data placed in the EED register. To write data to the EEPROM, the write enable bit, WREN, in the EEC register must first be set high to enable the write function. After this, the WR bit in the EEC register must be immediately set high to initiate a write cycle. These two instructions must be executed consecutively. The global interrupt bit EMI should also first be cleared before implementing any write operations, and then set again after the write cycle has started. Note that setting the WR bit high will not initiate a write cycle if the WREN bit has not been set. As the EEPROM write cycle is controlled using an internal timer whose operation is asynchronous to microcontroller system clock, a certain time will elapse before the data will have been written into the EEPROM. Detecting when the write cycle has finished can be implemented either by polling the WR bit in the EEC register or by using the EEPROM interrupt. When the write cycle terminates, the WR bit will be automatically cleared to zero by the microcontroller, informing the user that the data has been written to the EEPROM. The application program can therefore poll the WR bit to determine when the write cycle has ended.

### Write Protection

Protection against inadvertent write operation is provided in several ways. After the device is powered on, the Write enable bit in the control register will be cleared preventing any write operations. Also at power-on the Bank Pointer, BP, will be reset to zero, which means that Data Memory Bank 0 will be selected. As the EEPROM control register is located in Bank 1, this adds a further measure of protection against spurious write operations. During normal program operation, ensuring that the Write Enable bit in the control register is cleared will safeguard against incorrect write operations.

### EEPROM Interrupt

The EEPROM write interrupt is generated when an EEPROM write cycle has ended. The EEPROM interrupt must first be enabled by setting the DEE bit in the relevant interrupt register. However as the EEPROM is contained within a Multi-function Interrupt, the associated multi-function interrupt enable bit must also be set. When an EEPROM write cycle ends, the DEF request flag and its associated multi-function interrupt request flag will both be set. If the global, EEPROM and Multi-function interrupts are enabled and the stack is not full, a jump to the associated Multi-function Interrupt vector will take place. When the interrupt is serviced only the Multi-function interrupt flag will be automatically reset, the EEPROM interrupt flag must be manually reset by the application program. More details can be obtained in the Interrupt section.

## Programming Considerations

Care must be taken that data is not inadvertently written to the EEPROM. Protection can be Periodic by ensuring that the Write Enable bit is normally cleared to zero when not writing. Also the Bank Pointer could be normally cleared to zero as this would inhibit access to Bank 1 where the EEPROM control register exist. Although certainly not necessary, consideration might be given in the application program to the checking of the validity of new write data by a simple read back process. When writing data the WR bit must be set high immediately after the WREN bit has been set high, to ensure the write cycle executes correctly. The global interrupt bit EMI should also be cleared before a write cycle is executed and then re-enabled after the write cycle starts. Note that the device should not enter the IDLE or SLEEP mode until the EEPROM read or write operation is totally completed, otherwise, the EEPROM read or write operation will fail.

## Programming Examples

- **Reading data from the EEPROM – polling method**

```
MOV A, EEPROM_ADRES           ; user defined address
MOV EEA, A
MOV A, 040H                   ; setup memory pointer MP1
MOV MP1, A                    ; MP1 points to EEC register
MOV A, 01H                    ; setup Bank Pointer
MOV BP, A
SET IAR1.1                    ; set RDEN bit, enable read operations
SET IAR1.0                    ; start Read Cycle-set RD bit
BACK:
SZ  IAR1.0                    ; check for read cycle end
JMP BACK
CLR IAR1                      ; disable EEPROM write
CLR BP
MOV A, EED                    ; move read data to register
MOV READ_DATA, A
```

- **Writing Data to the EEPROM – polling method**

```
MOV A, EEPROM_ADRES           ; user defined address
MOV EEA, A
MOV A, EEPROM_DATA            ; user defined data
MOV EED, A
MOV A, 040H                   ; setup memory pointer MP1
MOV MP1, A                    ; MP1 points to EEC register
MOV A, 01H                    ; setup Bank Pointer
MOV BP, A                     ; BP points to data memory bank 1
CLR EMI
SET IAR1.3                    ; set WREN bit, enable write operations
SET IAR1.2                    ; start Write Cycle-set WR bit - executed immediately after
                             ; set WREN bit
SET EMI
BACK:
SZ  IAR1.2                    ; check for write cycle end
JMP BACK
CLR IAR1                      ; disable EEPROM write
CLR BP
```

# Oscillators

Various oscillator options offer the user a wide range of functions according to their various application requirements. The flexible features of the oscillator functions ensure that the best optimisation can be achieved in terms of speed and power saving. Oscillator selections and operation are selected through registers.

## Oscillator Overview

In addition to being the source of the main system clock the oscillators also provide clock sources for the Watchdog Timer and Time Base Interrupts. Fully integrated internal oscillators, requiring no external components, are provided to form a range of both fast and slow system oscillators. The higher frequency oscillators provide higher performance but carry with it the disadvantage of higher power requirements, while the opposite is of course true for the lower frequency oscillators. With the capability of dynamically switching between fast and slow system clock, the device has the flexibility to optimize the performance/power ratio, a feature especially important in power sensitive portable applications.

| Type | Name | Freq. |
|---|---|---|
| Internal High Speed RC | HIRC | 12MHz (adjustable) |
| Internal Low Speed RC | LIRC | 32kHz |

**Oscillator Types**

## System Clock Configurations

There are two methods of generating the system clock, a high speed internal RC oscillator and a low speed internal RC oscillator. Selecting whether the low or high speed oscillator is used as the system oscillator is implemented using the HLCLK bit and CKS2 ~ CKS0 bits in the SMOD register and as the system clock can be dynamically selected.

The actual source clock used for the high speed and the low speed oscillators is chosen via registers. The frequency of the slow speed or high speed system clock is also determined using the HLCLK bit and CKS2 ~ CKS0 bits in the SMOD register. Note that two oscillator selections must be made namely one high speed and one low speed system oscillators. It is not possible to choose a no-oscillator selection for either the high or low speed oscillator.
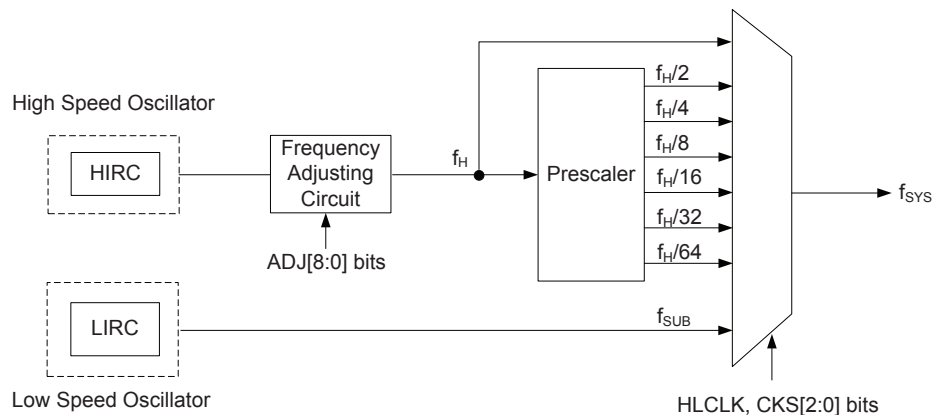


**System Clock Configurations**

### Internal RC Oscillator – HIRC

The internal high speed RC oscillator is a fully integrated system oscillator requiring no external components. The internal RC oscillator has a frequency of 12MHz which can be adjusted by changing the ADJ[8:0] bits field value. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. Note that if this internal system clock option is selected, it requires no external pins for its operation.

The ADJ[8:0] bit field in the FADJH and FADJL registers is used to adjust the HIRC oscillation frequency. The HIRC oscillator is supposed to have a frequency of 12MHz with the default ADJ[8:0] field value, 100000000B. The greater value the ADJ[8:0] field is written, the lower frequency the HIRC oscillator has. The HIRC oscillator will have a maximum adjusted frequency when the ADJ[8:0] field is set to 000000000B. Note that a certain time delay for the HIRC oscillator stabilization should be allowed when the HIRC oscillation frequency is changed by configuring the ADJ[8:0] field. The new HIRC frequency cannot be used until the updated frequency is stable.

#### FADJL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|------|
| Name | ADJ7 | ADJ6 | ADJ5 | ADJ4 | ADJ3 | ADJ2 | ADJ1 | ADJ0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0    **ADJ7~ADJ0**: HIRC frequency adjustment control bit 7 ~ bit 0

#### FADJH Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|------|
| Name | — | — | — | — | — | — | — | ADJ8 |
| R/W | — | — | — | — | — | — | — | R/W |
| POR | — | — | — | — | — | — | — | 1 |

Bit 7~1    Unimplemented, read as "0"

Bit 0    **ADJ8**: HIRC frequency adjustment control bit 8

### Internal 32kHz Oscillator – LIRC

The Internal 32kHz system oscillator is the low frequency oscillator. It is a fully integrated RC oscillator with a typical frequency of 32kHz at 5V, requiring no external components for its implementation. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised.

# Operating Modes and System Clocks

Present day applications require that their microcontrollers have high performance but often still demand that they consume as little power as possible, conflicting requirements that are especially true in battery powered portable applications. The fast clocks required for high performance will by their nature increase current consumption and of course vice-versa, lower speed clocks reduce current consumption. As Holtek has provided this device with both high and low speed clock sources and the means to switch between them dynamically, the user can optimise the operation of their microcontroller to achieve the best performance/power ratio.

## System Clocks

The device has many different clock sources for both the CPU and peripheral function operation. By providing the user with a wide range of clock options using register programming, a clock system can be configured to obtain maximum application performance.

The main system clock, can come from either a high frequency $f_H$ or low frequency $f_{SUB}$ source, and is selected using the HLCLK bit and CKS2~CKS0 bits in the SMOD register. The high speed system clock can be sourced from the HIRC oscillator. The low speed system clock source can be sourced from the LIRC oscillator. The other choice, which is a divided version of the high speed system oscillator has a range of $f_H/2$~$f_H/64$.
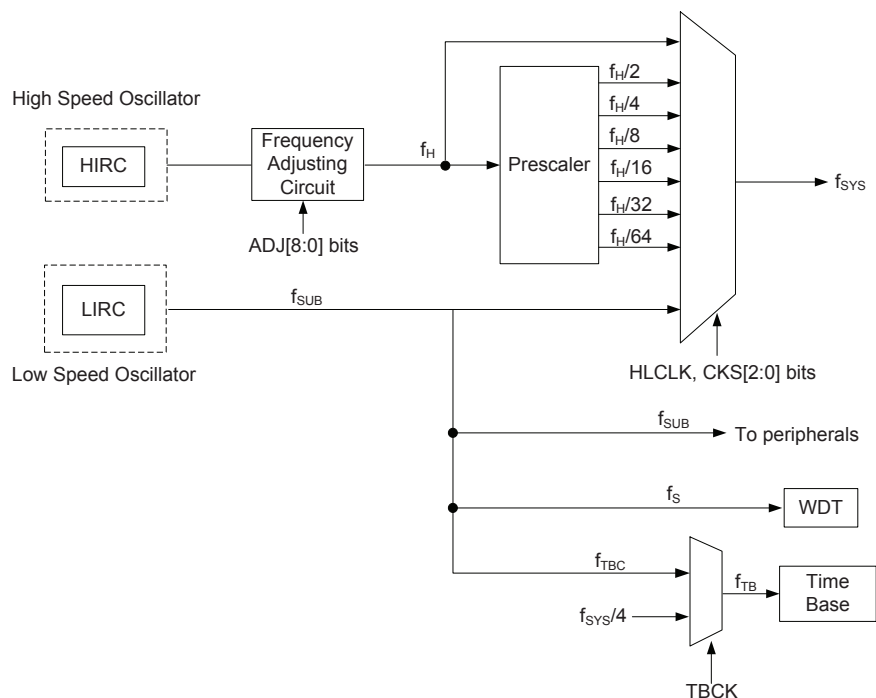


**Device Clock Configurations**

Note: When the system clock source $f_{SYS}$ is switched to $f_{SUB}$ from $f_H$, the high speed oscillator will stop to conserve the power. Thus there is no $f_H$~$f_H/64$ for peripheral circuit to use.

### System Operating Modes

There are six different modes of operation for the microcontroller, each one with its own special characteristics and which can be chosen according to the specific performance and power requirements of the application. There are two modes allowing normal operation of the microcontroller, the NORMAL Mode and SLOW Mode. The remaining four modes, the SLEEP0, SLEEP1, IDLE0 and IDLE1 Mode are used when the microcontroller CPU is switched off to conserve power.

| Operating Mode | Description | | | |
|---|---|---|---|---|
| | **CPU** | $f_{SYS}$ | $f_H$ | $f_{SUB}$ |
| NORMAL Mode | On | $f_H \sim f_H/64$ | On | On |
| SLOW Mode | On | $f_{SUB}$ | Off | On |
| ILDE0 Mode | Off | Off | Off | On |
| IDLE1 Mode | Off | On | On/Off | On |
| SLEEP0 Mode [(Note)] | Off | Off | Off | Off |
| SLEEP1 Mode | Off | Off | Off | On |

Note: If the Watchdog Timer configuration option is "Always enabled" which means the $f_{SUB}$ clock must always be on, there is not SLEEP0 mode.

#### NORMAL Mode

As the name suggests this is one of the main operating modes where the microcontroller has all of its functions operational and where the system clock is provided by the high speed oscillator. This mode operates allowing the microcontroller to operate normally with a clock source will come from the high speed oscillator, HIRC. The high speed oscillator will however first be divided by a ratio ranging from 1 to 64, the actual ratio being selected by the CKS2~CKS0 and HLCLK bits in the SMOD register. Although a high speed oscillator is used, running the microcontroller at a divided clock ratio reduces the operating current.

#### SLOW Mode

This is also a mode where the microcontroller operates normally although now with a slower speed clock source. The clock source used will be from $f_{SUB}$. Running the microcontroller in this mode allows it to run with much lower operating currents. In the SLOW Mode, the $f_H$ is off.

#### SLEEP0 Mode

If the WDT configuration option is "Always enabled", there is not SLEEP0 mode. If the WDT configuration option is "controlled by WDTC register" the MCU can enter the SLEEP0 mode. The SLEEP Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is low. In the SLEEP0 mode the CPU will be stopped, and the $f_{SUB}$ and $f_S$ clocks will be stopped too, and the Watchdog Timer function is disabled. In this mode, the LVDEN is must cleared to zero. If the LVDEN is set high, it won't enter the SLEEP0 Mode.

#### SLEEP1 Mode

The SLEEP Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is low. In the SLEEP1 mode the CPU will be stopped. However the $f_{SUB}$ and $f_S$ clocks will continue to operate if the LVDEN is "1" or the Watchdog Timer function is enabled.

#### IDLE0 Mode

The IDLE0 Mode is entered when a HALT instruction is executed and when the IDLEN bit in the SMOD register is high and the FSYSON bit in the CTRL register is low. In the IDLE0 Mode the system oscillator will be inhibited from driving the CPU, the system oscillator will be stopped, the low frequency clock $f_{SUB}$ will be on to drive some peripheral functions.

### IDLE1 Mode

The IDLE1 Mode is entered when a HALT instruction is executed and when the IDLEN bit in the SMOD register is high and the FSYSON bit in the CTRL register is high. In the IDLE1 Mode the system oscillator will be inhibited from driving the CPU, the system oscillator will continue to run, and this system oscillator may be high speed or low speed system oscillator. In the IDLE1 Mode the low frequency clock $f_{SUB}$ will be on to drive some peripheral functions.

Note: If LVDEN=1 and the SLEEP or IDLE mode is entered, the LVD and bandgap functions will not be disabled, and the $f_{SUB}$ clock will be forced to be enabled.

## Control Registers

The SMOD and CTRL registers are used to control the internal clocks within the device.

### SMOD Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CKS2 | CKS1 | CKS0 | — | LTO | HTO | IDLEN | HLCLK |
| R/W | R/W | R/W | R/W | — | R | R | R/W | R/W |
| POR | 1 | 1 | 0 | — | 0 | 0 | 1 | 0 |

Bit 7 ~ 5     **CKS2 ~ CKS0**: The system clock selection when HLCLK is "0"
000: $f_{SUB}$
001: $f_{SUB}$
010: $f_H/64$
011: $f_H/32$
100: $f_H/16$
101: $f_H/8$
110: $f_H/4$
111: $f_H/2$

These three bits are used to select which clock is used as the system clock source. In addition to the system clock source, which can be LIRC, a divided version of the high speed system oscillator can also be chosen as the system clock source.

Bit 4     Unimplemented, read as "0"

Bit 3     **LTO**: LIRC System OSC SST ready flag
0: Not ready
1: Ready

This is the low speed system oscillator SST ready flag which indicates when the low speed system oscillator is stable after power on reset or a wake-up has occurred. The flag will change to a high level after 1~2 cycles.

Bit 2     **HTO**: HIRC System OSC SST ready flag
0: Not ready
1: Ready

This is the high speed system oscillator SST ready flag which indicates when the high speed system oscillator is stable after a wake-up has occurred. This flag is cleared to "0" by hardware when the device is powered on and then changes to a high level after the high speed system oscillator is stable. Therefore this flag will always be read as "1" by the application program after device power-on. The flag will be low when in the SLEEP or IDLE0 Mode but after power on reset or a wake-up has occurred, the flag will change to a high level after 15~16 clock cycles if the HIRC oscillator is used.

Bit 1     **IDLEN**: IDLE Mode Control

    0: Disable

    1: Enable

This is the IDLE Mode Control bit and determines what happens when the HALT instruction is executed. If this bit is high, when a HALT instruction is executed the device will enter the IDLE Mode. In the IDLE1 Mode the CPU will stop running but the system clock will continue to keep the peripheral functions operational, if FSYSON bit is high. If FSYSON bit is low, the CPU and the system clock will all stop in IDLE0 mode. If the bit is low the device will enter the SLEEP Mode when a HALT instruction is executed.

Bit 0     **HLCLK**: System Clock Selection

    0: $f_H/2 \sim f_H/64$ or $f_{SUB}$

    1: $f_H$

This bit is used to select if the $f_H$ clock or the $f_H/2 \sim f_H/64$ or $f_{SUB}$ clock is used as the system clock. When the bit is high the $f_H$ clock will be selected and if low the $f_H/2 \sim f_H/64$ or $f_{SUB}$ clock will be selected. When system clock switches from the $f_H$ clock to the $f_{SUB}$ clock and the $f_H$ clock will be automatically switched off to conserve power.

**CTRL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FSYSON | — | — | — | — | LVRF | LRF | WRF |
| R/W | R/W | — | — | — | — | R/W | R/W | R/W |
| POR | 0 | — | — | — | — | x | 0 | 0 |

"x" unknown

Bit 7     **FSYSON**: $f_{SYS}$ Control in IDLE Mode

    0: Disable

    1: Enable

Bit 6 ~ 3   Unimplemented, read as "0"

Bit 2     **LVRF**: LVR function reset flag

Described elsewhere

Bit 1     **LRF**: LVRC control register software reset flag

Described elsewhere

Bit 0     **WRF**: WDTC control register software reset flag

Described elsewhere

## Operating Mode Switching

The device can switch between operating modes dynamically allowing the user to select the best performance/power ratio for the present task in hand. In this way microcontroller operations that do not require high performance can be executed using slower clocks thus requiring less operating current and prolonging battery life in portable applications.

In simple terms, Mode Switching between the NORMAL Mode and SLOW Mode is executed using the HLCLK bit and CKS2~CKS0 bits in the SMOD register while Mode Switching from the NORMAL/SLOW Modes to the SLEEP/IDLE Modes is executed via the HALT instruction. When a HALT instruction is executed, whether the device enters the IDLE Mode or the SLEEP Mode is determined by the condition of the IDLEN bit in the SMOD register and FSYSON in the CTRL register.

When the HLCLK bit switches to a low level, which implies that clock source is switched from the high speed clock source, $f_H$, to the clock source, $f_H/2 \sim f_H/64$ or $f_{SUB}$. If the clock is from the $f_{SUB}$, the high speed clock source will stop running to conserve power. When this happens it must be noted that the $f_H/16$ and $f_H/64$ internal clock sources will also stop running, which may affect the operation of other internal functions such as the TMs. The accompanying flowchart shows what happens when the device moves between the various operating modes.
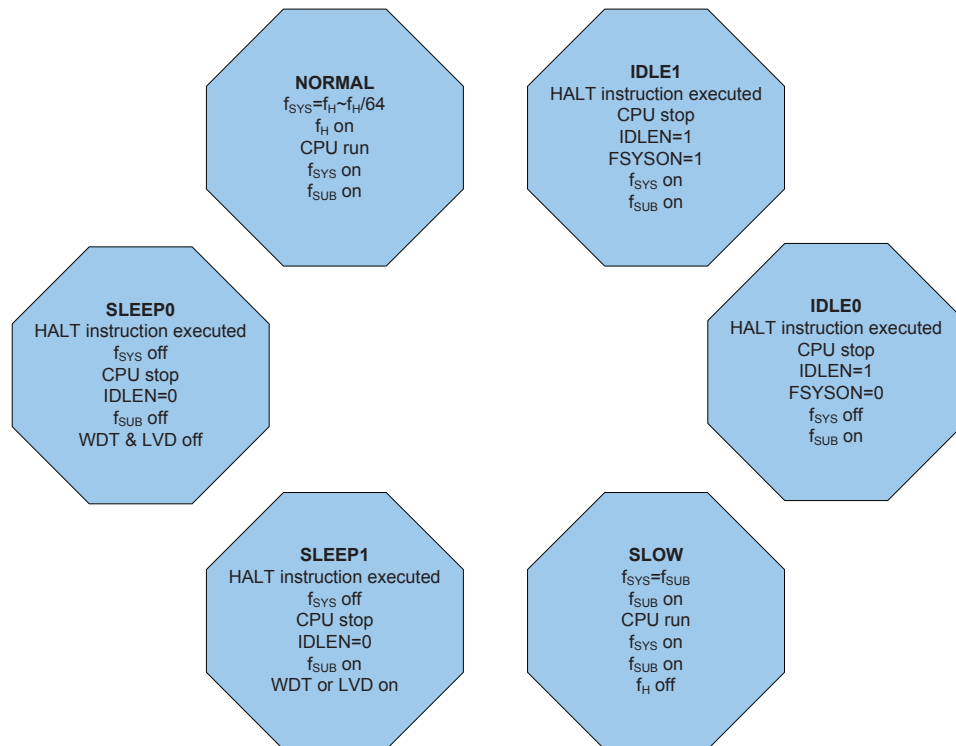


Note: If the Watchdog Timer configuration option is "Always enabled" which means the $f_{SUB}$ clock must always be on, there is not SLEEP0 mode.

**NORMAL Mode to SLOW Mode Switching**

When running in the NORMAL Mode, which uses the high speed system oscillator, and therefore consumes more power, the system clock can switch to run in the SLOW Mode by setting the HLCLK bit to "0" and setting the CKS2~CKS0 bits to "000" or "001" in the SMOD register. This will then use the low speed system oscillator which will consume less power. Users may decide to do this for certain operations which do not require high performance and can subsequently reduce power consumption.

The SLOW Mode is sourced from the LIRC oscillator and therefore requires this oscillator to be stable before full mode switching occurs. This is monitored using the LTO bit in the SMOD register.
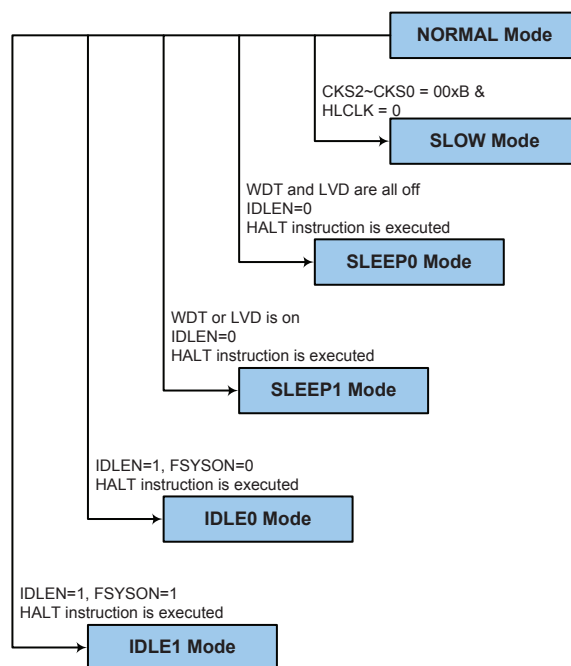
**SLOW Mode to NORMAL Mode Switching**

In SLOW Mode the system uses LIRC low speed system oscillator. To switch back to the NORMAL Mode, where the high speed system oscillator is used, the HLCLK bit should be set to "1" or HLCLK bit is "0", but CKS2~CKS0 is set to "010", "011", "100", "101", "110" or "111". As a certain amount of time will be required for the high frequency clock to stabilise, the status of the HTO bit is checked. The amount of time required for high speed system oscillator stabilization depends upon which high speed system oscillator type is used.
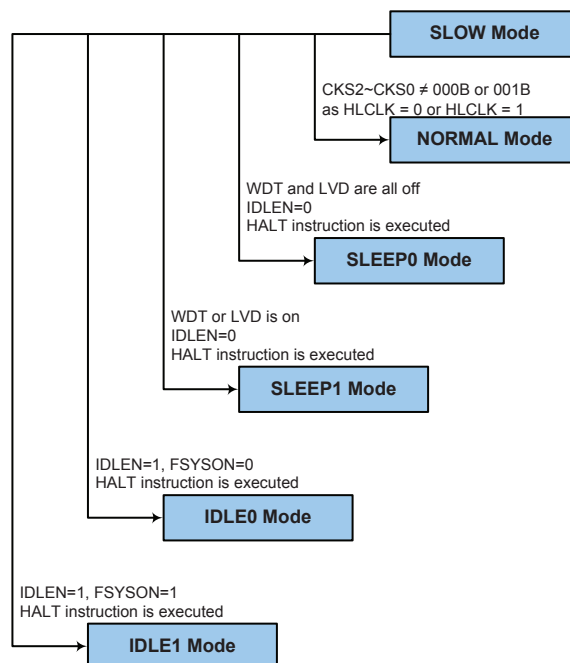


**Entering the SLEEP0 Mode**

There is only one way for the device to enter the SLEEP0 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "0" and the WDT and LVD are both off. When this instruction is executed under the conditions described above, the following will occur:

- The system clock and the $f_{SUB}$ clock will be stopped and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and stopped.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Entering the SLEEP1 Mode

There is only one way for the device to enter the SLEEP1 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "0" and the WDT or LVD is on. When this instruction is executed under the conditions described above, the following will occur:

- The system clock will be stopped and the application program will stop at the "HALT" instruction but the WDT or LVD will remain with the clock source coming with the $f_{SUB}$ clock.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting as the WDT is enabled.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Entering the IDLE0 Mode

There is only one way for the device to enter the IDLE0 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "1" and the FSYSON bit in CTRL register equal to "0". When this instruction is executed under the conditions described above, the following will occur:

- The system clock will be stopped and the application program will stop at the "HALT" instruction, but the low frequency $f_{SUB}$ clock will be on.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting.
- The I/O ports will maintain their present conditions as it is enabled.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Entering the IDLE1 Mode

There is only one way for the device to enter the IDLE1 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "1" and the FSYSON bit in CTRL register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

- The system clock and the low frequency $f_{SUB}$ will be on and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting as it is enabled.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Standby Current Considerations

As the main reason for entering the SLEEP or IDLE Mode is to keep the current consumption of the device to as low a value as possible, perhaps only in the order of several micro-amps except in the IDLE1 Mode, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised. Special attention must be made to the I/O pins on the device. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. This also applies to devices which have different package types, as there may be unbonded pins. These must either be setup as outputs or if setup as inputs must have pull-high resistors connected.

Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs. In the IDLE1 Mode the system oscillator is on, if the system oscillator is from the high speed system oscillator, the additional standby current will also be perhaps in the order of several hundred micro-amps.

### Wake-up

After the system enters the SLEEP or IDLE Mode, it can be woken up from one of various sources listed as follows:

- An external falling edge on Port A
- A system interrupt
- A WDT overflow

If the device is woken up by a WDT overflow, a Watchdog Timer reset will be initiated. The actual source of the wake-up can be determined by examining the TO and PDF flags. The PDF flag is cleared by a system power-up or executing the clear Watchdog Timer instructions and is set when executing the "HALT" instruction. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the Program Counter and Stack Pointer, the other flags remain in their original status.

Each pin on Port A can be setup using the PAWU register to permit a negative transition on the pin to wake-up the system. When a Port A pin wake-up occurs, the program will resume execution at the instruction following the "HALT" instruction. If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the "HALT" instruction. In this situation, the interrupt which woke-up the device will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set high before entering the SLEEP or IDLE Mode, the wake-up function of the related interrupt will be disabled.

# Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise.

## Watchdog Timer Clock Source

The Watchdog Timer clock source is provided by the internal $f_S$ clock which is in turn supplied by the LIRC oscillator. The Watchdog Timer source clock is then subdivided by a ratio of $2^8$ to $2^{18}$ to give longer timeouts, the actual value being chosen using the WS2~WS0 bits in the WDTC register. The LIRC internal oscillator has an approximate period of 32kHz at a supply voltage of 5V. However, it should be noted that this specified internal clock period can vary with $V_{DD}$, temperature and process variations.

## Watchdog Timer Control Register

A single register, WDTC, controls the required timeout period as well as the enable/disable operation. This register together with the configuration option control the overall operation of the Watchdog Timer.

### WDTC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|------|
| Name | WE4 | WE3 | WE2 | WE1 | WE0 | WS2 | WS1 | WS0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

Bit 7~3     **WE4~WE0**: WDT function enable/disable control

If the WDT configuration option is "Always enabled":
   10101 or 01010: Enable
   Others: Reset MCU

If the WDT configuration option is "Controlled by WDTC register":
   10101: Disable
   01010: Enable
   Others: Reset MCU

When these bits are changed by the environmental noise or software setting to reset the microcontroller, the reset operation will be activated after a delay time, $t_{SRESET}$ and the WRF bit in the CTRL register will be set high.

Bit 2~0     **WS2~WS0**: WDT time-out period selection
   000: $2^8/f_S$
   001: $2^{10}/f_S$
   010: $2^{12}/f_S$
   011: $2^{14}/f_S$
   100: $2^{15}/f_S$
   101: $2^{16}/f_S$
   110: $2^{17}/f_S$
   111: $2^{18}/f_S$

These three bits determine the division ratio of the Watchdog Timer source clock, which in turn determines the timeout period.

**CTRL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | FSYSON | — | — | — | — | LVRF | LRF | WRF |
| R/W | R/W | — | — | — | — | R/W | R/W | R/W |
| POR | 0 | — | — | — | — | x | 0 | 0 |

"x" unknown

Bit 7      **FSYSON**: $f_{SYS}$ Control in IDLE Mode
           Described elsewhere.

Bit 6~3    Unimplemented, read as "0"

Bit 2      **LVRF**: LVR function reset flag
           Described elsewhere.

Bit 1      **LRF**: LVRC Control register software reset flag
           Described elsewhere.

Bit 0      **WRF**: WDTC Control register software reset flag
             0: Not occur
             1: Occurred
           This bit is set high by the WDT Control register software reset and cleared by the
           application program. Note that this bit can only be cleared to zero by the application
           program.

## Watchdog Timer Operation

The Watchdog Timer operates by providing a device reset when its timer overflows. This means
that in the application program and during normal operation the user has to strategically clear the
Watchdog Timer before it overflows to prevent the Watchdog Timer from executing a reset. This is
done using the clear watchdog instructions. If the program malfunctions for whatever reason, jumps
to an unknown location, or enters an endless loop, these clear instructions will not be executed in the
correct manner, in which case the Watchdog Timer will overflow and reset the device. With regard
to the Watchdog Timer enable/disable function, there are also five bits, WE4~WE0, in the WDTC
register to offer additional enable/disable and reset control of the Watchdog Timer. If the WDT
configuration option is that the WDT function is always enabled, the WE4~WE0 bits still have
effects on the WDT function. When the WE4~WE0 bits value is equal to 01010B or 10101B, the
WDT function is enabled. However, if the WE4~WE0 bits are changed to any other values except
01010B and 10101B, which is caused by the environmental noise or software setting, it will reset
the microcontroller after 2~3 $f_{SUB}$ clock cycles. If the WDT configuration option is that the WDT
function is controlled by the WDTC register, the WE4~WE0 values can determine which mode the
WDT operates in. The WDT function will be disabled when the WE4~WE0 bits are set to a value of
10101B. The WDT function will be enabled if the WE4~WE0 bits value is equal to 01010B. If the
WE4~WE0 bits are set to any other values except 01010B and 10101B by the environmental noise
or software setting, it will reset the device after 2~3 $f_{SUB}$ clock cycles. After power on these bits will
have the value of 01010B.

| WDT Configuration Option | WE4 ~ WE0 Bits | WDT Function |
|--------------------------|----------------|--------------|
| Always Enabled | 01010B or 10101B | Enable |
| | Any other values | Reset MCU |
| Controlled by WDTC Register | 10101B | Disable |
| | 01010B | Enable |
| | Any other values | Reset MCU |

**Watchdog Timer Enable/Disable Control**

Under normal program operation, a Watchdog Timer time-out will initialise a device reset and set the status bit TO. However, if the system is in the SLEEP or IDLE Mode, when a Watchdog Timer time-out occurs, the TO bit in the status register will be set and only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the Watchdog Timer. The first is a WDT reset, which means a certain value except 01010B and 10101B written into the WE4~WE0 bit filed, the second is using the Watchdog Timer software clear instructions and the third is via a HALT instruction.

There is only one method of using software instruction to clear the Watchdog Timer. That is to use the single "CLR WDT" instruction to clear the WDT.

The maximum time out period is when the $2^{18}$ division ratio is selected. As an example, with a 32kHz LIRC oscillator as its source clock, this will give a maximum watchdog period of around 8 second for the $2^{18}$ division ratio, and a minimum timeout of 7.8ms for the $2^{8}$ division ration.



**Watchdog Timer**
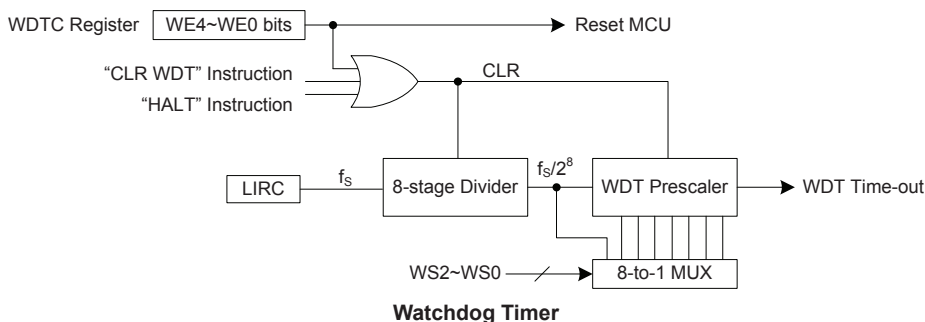
# Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup. Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset is implemented in situations where the power supply voltage falls below a certain threshold.

## Reset Functions

There are several ways in which a microcontroller reset can occur, through events occurring internally:

### Power-on Reset

The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.
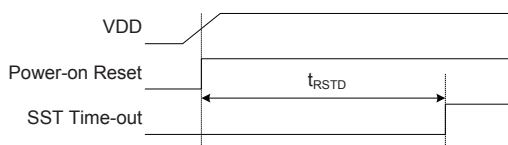


**Power-On Reset Timing Chart**

### Low Voltage Reset – LVR

The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device. The LVR function is always enabled with a specific LVR voltage, $V_{LVR}$. If the supply voltage of the device drops to within a range of $0.9V \sim V_{LVR}$ such as might occur when changing the battery, the LVR will automatically reset the device internally and the LVRF bit in the CTRL register will also be set high. For a valid LVR signal, a low voltage, i.e., a voltage in the range between $0.9V \sim V_{LVR}$ must exist for greater than the value $t_{LVR}$ specified in the LVD&LVR characteristics table. If the low voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function.

The actual $V_{LVR}$ is defined by the LVS7~LVS0 bits in the LVRC register. If the LVS7~LVS0 bits are changed to any other value except some certain values defined in the LVRC register by the environmental noise, the LVR will reset the device after 2~3 LIRC clock cycles. When this happens, the LRF bit in the CTRL register will be set high. After power on the register will have the value of 01010101B. Note that the LVR function will be automatically disabled when the device enters the power down mode.
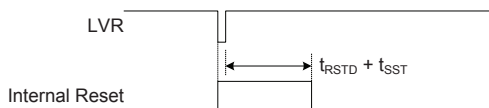
Note: $t_{RSTD}$ is power-on delay, typical time=50ms

**Low Voltage Reset Timing Chart**

- **LVRC Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LVS7 | LVS6 | LVS5 | LVS4 | LVS3 | LVS2 | LVS1 | LVS0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

Bit 7 ~ 0     **LVS7 ~ LVS0**: LVR Voltage Select control
01010101: 2.1V
00110011: 2.55V
10011001: 3.15V
10101010: 3.8V
Other values: MCU reset – register is reset to POR value

When an actual low voltage condition occurs, an MCU reset will be generated. The reset operation will be activated after the low voltage condition keeps more than a $t_{LVR}$ time. In this situation this register contents will remain the same after such a reset occurs.

Any register value, other than the defined values above, will also result in the generation of an MCU reset. The reset operation will be activated after a delay time, $t_{SRESET}$. However in this situation this register contents will be reset to the POR value.

- **CTRL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FSYSON | — | — | — | — | LVRF | LRF | WRF |
| R/W | R/W | — | — | — | — | R/W | R/W | R/W |
| POR | 0 | — | — | — | — | x | 0 | 0 |

"x" unknown

Bit 7          **FSYSON**: $f_{SYS}$ Control in IDLE Mode
Described elsewhere

Bit 6 ~ 3     Unimplemented, read as "0"

Bit 2          **LVRF**: LVR function reset flag
0: Not occurred
1: Occurred
This bit is set high when a specific low voltage reset situation condition occurs. This bit can only be cleared to zero by application program.

Bit 1          **LRF**: LVRC control register software reset flag
0: Not occurred
1: Occurred
This bit is set high when the LVRC register contains any undefined LVR voltage register value. This in effect acts like a software reset function. This bit can only be cleared to zero by application program.

Bit 0          **WRF**: WDTC control register software reset flag
Described elsewhere

### Watchdog Time-out Reset during Normal Operation

The Watchdog time-out Reset during normal operation is the same as a LVR reset except that the Watchdog time-out flag TO will be set high.
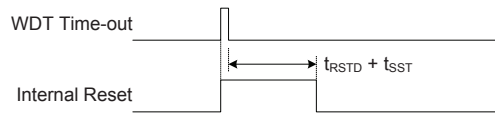


**WDT Time-out Reset during Normal Operation Timing Chart**

### Watchdog Time-out Reset during SLEEP or IDLE Mode

The Watchdog time-out Reset during SLEEP or IDLE Mode is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to zero and the TO flag will be set high. Refer to the A.C. Characteristics for $t_{SST}$ details.
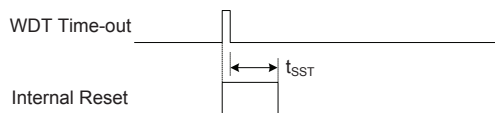


**WDT Time-out Reset during SLEEP or IDLE Timing Chart**

## Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the SLEEP or IDLE Mode function or Watchdog Timer. The reset flags are shown in the table:

| TO | PDF | RESET Conditions |
|----|-----|------------------|
| 0 | 0 | Power-on reset |
| u | u | LVR reset during NORMAL or SLOW Mode operation |
| 1 | u | WDT time-out reset during NORMAL or SLOW Mode operation |
| 1 | 1 | WDT time-out reset during IDLE or SLEEP Mode operation |

Note: "u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

| Item | Condition After RESET |
|------|----------------------|
| Program Counter | Reset to zero |
| Interrupts | All interrupts will be disabled |
| WDT | Clear after reset, WDT begins counting |
| Timer Modules | Timer Modules will be turned off |
| Input/Output Ports | I/O ports will be setup as inputs |
| Stack Pointer | Stack Pointer will point to the top of the stack |

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers.

| Register | Reset (Power On) | WDT Time-out (Normal Operation) | WDT Time-out (SLEEP/IDLE) |
|---|---|---|---|
| MP0 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| MP1 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| BP | ---- ---0 | ---- ---0 | ---- ---u |
| ACC | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 0000 0000 | 0000 0000 | 0000 0000 |
| TBLP | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TBLH | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TBHP | ---- -xxx | ---- -uuu | ---- -uuu |
| STATUS | --00 xxxx | --1u uuuu | --11 uuuu |
| SMOD | 110- 0010 | 110- 0010 | uuu- uuuu |
| LVDC | --00 -000 | --00 -000 | --uu -uuu |
| INTEG | ---- 0000 | ---- 0000 | ---- uuuu |
| INTC0 | --00 -000 | --00 -000 | --uu -uuu |
| INTC1 | 0000 0000 | 0000 0000 | uuuu uuuu |
| INTC2 | --00 --00 | --00 --00 | --uu --uu |
| MFI0 | --00 --00 | --00 --00 | --uu --uu |
| MFI1 | --00 --00 | --00 --00 | --uu --uu |
| PA | 1111 1111 | 1111 1111 | uuuu uuuu |
| PAC | 1111 1111 | 1111 1111 | uuuu uuuu |
| PAPU | 0000 0000 | 0000 0000 | uuuu uuuu |
| PAWU | 0000 0000 | 0000 0000 | uuuu uuuu |
| MFI2 | --00 --00 | --00 --00 | --uu --uu |
| WDTC | 0101 0011 | 0101 0011 | uuuu uuuu |
| TBC | 0011 -111 | 0011 -111 | uuuu -uuu |
| EEA | --00 0000 | --00 0000 | --uu uuuu |
| EED | 0000 0000 | 0000 0000 | uuuu uuuu |
| EEC | ---- 0000 | ---- 0000 | ---- uuuu |
| FADJL | 0000 0000 | 0000 0000 | uuuu uuuu |
| FADJH | ---- ---1 | ---- ---1 | ---- ---u |
| CTRL | 0--- -x00 | 0--- -000 | u--- -uuu |
| LVRC | 0101 0101 | 0101 0101 | uuuu uuuu |
| STMC0 | 0000 0000 | 0000 0000 | uuuu uuuu |
| STMC1 | 0000 0000 | 0000 0000 | uuuu uuuu |
| STMDL | 0000 0000 | 0000 0000 | uuuu uuuu |
| STMDH | ---- --00 | ---- --00 | ---- --uu |
| STMAL | 0000 0000 | 0000 0000 | uuuu uuuu |
| STMAH | ---- --00 | ---- --00 | ---- --uu |
| CTRL2 | ---- --00 | ---- --00 | ---- --uu |
| CTRL3 | -000 0000 | -000 0000 | -uuu uuuu |
| SLEWC | ---- --00 | ---- --00 | ---- --uu |
| SLEDC | ---- 0000 | ---- 0000 | ---- uuuu |
| PTMC0 | 0000 0--- | 0000 0--- | uuuu u--- |
| PTMC1 | 0000 0000 | 0000 0000 | uuuu uuuu |

| Register | Reset (Power On) | WDT Time-out (Normal Operation) | WDT Time-out (SLEEP/IDLE) |
|---|---|---|---|
| PTMDL | 0000 0000 | 0000 0000 | uuuu uuuu |
| PTMDH | - - - - - - 0 0 | - - - - - - 0 0 | - - - - - - u u |
| PTMAL | 0000 0000 | 0000 0000 | uuuu uuuu |
| PTMAH | - - - - - - 0 0 | - - - - - - 0 0 | - - - - - - u u |
| PTMRPL | 0000 0000 | 0000 0000 | uuuu uuuu |
| PTMRPH | - - - - - - 0 0 | - - - - - - 0 0 | - - - - - - u u |
| OCVPC0 | 1100 1000 | 1100 1000 | uuuu uuuu |
| OCVPC1 | 0000 - - 0 0 | 0000 - - 0 0 | uuuu - - u u |
| OCVPC2 | - 000 0000 | - 000 0000 | - uuu uuuu |
| OCVPDA | 0000 0000 | 0000 0000 | uuuu uuuu |
| OCVPOCAL | 0010 0000 | 0010 0000 | uuuu uuuu |
| OCVPCCAL | 0001 0000 | 0001 0000 | uuuu uuuu |

Note: "-" stands for unimplemented

"u" stands for unchanged

"x" stands for unknown

## Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high selections for all ports and wake-up selections on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

The device provides bidirectional input/output lines labeled with port name PA. These I/O ports are mapped to the RAM Data Memory with specific addresses as shown in the Special Purpose Data Memory table. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A, [m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PA | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| PAC | PAC7 | PAC6 | PAC5 | PAC4 | PAC3 | PAC2 | PAC1 | PAC0 |
| PAPU | PAPU7 | PAPU6 | PAPU5 | PAPU4 | PAPU3 | PAPU2 | PAPU1 | PAPU0 |
| PAWU | PAWU7 | PAWU6 | PAWU5 | PAWU4 | PAWU3 | PAWU2 | PAWU1 | PAWU0 |

**I/O Logic Function Registers List**

## Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selected using registers PAPU, and are implemented using weak PMOS transistors.

Note that only when the I/O ports are configured as digital input or NMOS output, the internal pull-high functions can be enabled using the PAPU registers. In other conditions, internal pull-high functions are disabled.

### PAPU Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | PAPU7 | PAPU6 | PAPU5 | PAPU4 | PAPU3 | PAPU2 | PAPU1 | PAPU0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 ~ 0     **PAPU7~PAPU0**: Port A Pin Pull-high Control
         0: Disable
         1: Enable

## Port A Wake-up

The HALT instruction forces the microcontroller into the SLEEP or IDLE Mode which preserves power, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the Port A pins from high to low. This function is especially suitable for applications that can be woken up via external switches. Each pin on Port A can be selected individually to have this wake-up feature using the PAWU register.

Note that only when the Port A pins are configured as general purpose I/Os and the device is in the HALT status, the Port A wake-up functions can be enabled using the relevant bits in the PAWU register. In other conditions, the wake-up functions are disabled.

### PAWU Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | PAWU7 | PAWU6 | PAWU5 | PAWU4 | PAWU3 | PAWU2 | PAWU1 | PAWU0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 ~ 0     **PAWU7~PAWU0**: Port A Pin Wake-up Control
         0: Disable
         1: Enable

### I/O Port Control Registers

Each I/O port has its own control register known as PAC, to control the input/output configuration. With this control register, each CMOS output or input can be reconfigured dynamically under software control. Each pin of the I/O ports is directly mapped to a bit in its associated port control register. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

#### PAC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | PAC7 | PAC6 | PAC5 | PAC4 | PAC3 | PAC2 | PAC1 | PAC0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bit 7 ~ 0    **PAC7~PAC0**: Port A Pin Input/Output Type Selection
        0: Output
        1: Input

### I/O Port Source Current Control

The device supports different source current driving capability for PA port. With the corresponding selection register, SLEDC, each I/O port can support four levels of the source current driving capability. Users should refer to the D.C. characteristics section to select the desired source current for different applications.

#### SLEDC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | — | — | — | — | SLEDC3 | SLEDC2 | SLEDC1 | SLEDC0 |
| R/W | — | — | — | — | R/W | R/W | R/W | R/W |
| POR | — | — | — | — | 0 | 0 | 0 | 0 |

Bit 7~4    Unimplemented, read as "0"

Bit 3~2    **SLEDC3~SLEDC2**: PA7~PA4 Source Current Selection
        00: Source current=Level 0 (min.)
        01: Source current=Level 1
        10: Source current=Level 2
        11: Source current=Level 3 (max.)

Bit 1~0    **SLEDC1~SLEDC0**: PA3, PA2, PA0 Source Current Selection
        00: Source current=Level 0 (min.)
        01: Source current=Level 1
        10: Source current=Level 2
        11: Source current=Level 3 (max.)

Note: Users should refer to the D.C. Characteristics section to obtain the exact value for different applications.

### I/O Port Output Slew Rate Control

The device supports different output slew rate driving capability for PA1 port. With the corresponding selection register, SLEWC, PA1 port can support four levels of the output slew rate driving capability. Users should refer to the D.C. characteristics section to select the desired output slew rate for different applications.

#### SLEWC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | SLEWC1 | SLEWC0 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2    Unimplemented, read as "0"

Bit 1~0    **SLEWC1~SLEWC0**: PA1 Output Slew Rate Selection
00: Slew Rate=Level 0 (min.)
01: Slew Rate=Level 1
10: Slew Rate=Level 2
11: Slew Rate=Level 3 (max.)

Note: Users should refer to the D.C. Characteristics section to obtain the exact value for different applications.

## Pin-shared Function

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers but by supplying pins with multi-functions, many of these difficulties can be overcome. For these pins, the desired function of the multi-function I/O pins is selected by a series of registers via the application program control.

### Pin-shared Function Selection Registers

The most important point to note is to make sure that the desired pin-shared function is properly selected and also deselected. To select the desired pin-shared function, the pin-shared function should first be correctly selected using the corresponding pin-shared control register. After that the corresponding peripheral functional setting should be configured and then the peripheral function can be enabled. To correctly deselect the pin-shared function, the peripheral function should first be disabled and then the corresponding pin-shared function control register can be modified to select other pin-shared functions.

When the pin-shared input function is selected to be used, the corresponding input and output functions selection should be properly managed. For example, if the OCVP is used, the corresponding output pin-shared function should be configured as the OCVPAI0/ OCVPCI function by configuring the CTRL3 register and the OCVPAI0 signal intput should be properly selected using the CTRL2 register. However, if the external interrupt function is selected to be used, the relevant output pin-shared function should be selected as an I/O function and the interrupt input signal should be selected.

- **CTRL3 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | IOCN6 | IOCN5 | IOCN4 | IOCN3 | IOCN2 | IOCN1 | IOCN0 |
| R/W | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7      Unimplemented, read as "0"

Bit 6      **IOCN6**: PA7 pin-shared function selection
         0: PA7
         1: OCVPAI0

Bit 5      **IOCN5**: PA6 pin-shared function selection
         0: PA6
         1: OCVPAI0

Bit 4      **IOCN4**: PA5 pin-shared function selection
         0: INT1/STCK/PA5
         1: OCVPCI

         The INT1 or STCK pin function is furtherly selected using the corresponding function selection bits in the interrupt control register or STM control register.

Bit 3~2      **IOCN3 ~ IOCN2**: PA4 pin-shared function selection
         00: PA4
         01: STP
         10: OCVPAI0
         11: VREF

Bit 1      **IOCN1**: PA3 pin-shared function selection
         0: INT0/PTCK/PA3
         1: OCVPAI0

         The INT0 or PTCK pin function is furtherly selected using the corresponding function selection bits in the interrupt control register or PTM control register.

Bit 0      **IOCN0**: PA1 pin-shared function selection
         0: PA1
         1: PTP

- **CTRL2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | OCVPS1 | OCVPS0 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2      Unimplemented, read as "0"

Bit 1~0      **OCVPS1 ~ OCVPS0**: OCVPAI0 Input Source Pin Selection
         00: OCVPAI0 on PA4
         01: OCVPAI0 on PA3
         10: OCVPAI0 on PA6
         11: OCVPAI0 on PA7

## I/O Pin Structures

The accompanying diagram illustrates the internal structures of the logic I/O fuction. As the exact logical construction of the I/O pin will differ from this diagram, it is supplied as a guide only to assist with the functional understanding of the logic function I/O pins. The wide range of pin-shared structures does not permit all types to be shown.



**Logic Function Input/Output Structure**
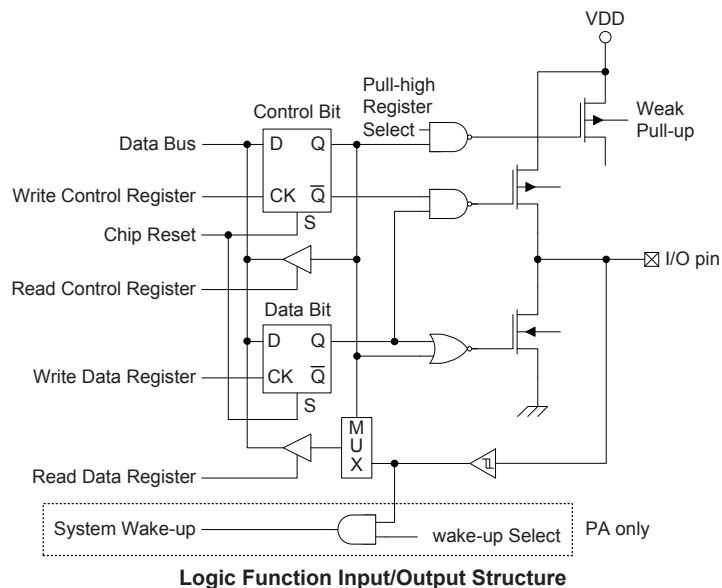
## Programming Considerations

Within the user program, one of the first things to consider is port initialisation. After a reset, all of the I/O data and port control registers will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high selections have been chosen. If the port control registers, PAC, is then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data register, PA, is first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct values into the appropriate port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.

Port A has the additional capability of providing wake-up functions. When the device is in the SLEEP or IDLE Mode, various methods are available to wake the device up. One of these is a high to low transition of any of the Port A pins. Single or multiple pins on Port A can be setup to have this function.

## Timer Modules – TM

One of the most fundamental functions in any microcontroller device is the ability to control and measure time. To implement time related functions the device includes several Timer Modules, abbreviated to the name TM. The TMs are multi-purpose timing units and serve to provide operations such as Timer/Counter, Input Capture, Compare Match Output and Single Pulse Output as well as being the functional unit for the generation of PWM signals. Each of the TMs has two individual interrupts. The addition of input and output pins for each TM ensures that users are provided with timing units with a wide and flexible range of features.

The common features of the different TM types are described here with more detailed information provided in the individual, Standard and Periodic TM sections.

### Introduction

The device contains a 10-bit Standard TM named STM and a 10-bit Periodic TM, named PTM. Although similar in nature, the different TM types vary in their feature complexity. The common features to the Standard and Periodic TMs will be described in this section and the detailed operation will be described in corresponding sections. The main features and differences between the two types of TM are summarised in the accompanying table.

| Function | STM | PTM |
|---|---|---|
| Timer/Counter | √ | √ |
| I/P Capture | √ | √ |
| Compare Match Output | √ | √ |
| PWM Channels | 1 | 1 |
| Single Pulse Output | 1 | 1 |
| PWM Alignment | Edge | Edge |
| PWM Adjustment Period & Duty | Duty or Period | Duty or Period |

**TM Function Summary**

| STM | PTM |
|---|---|
| 10-bit STM | 10-bit PTM |

**TM Name/Type Reference**

### TM Operation

The two different types of TMs offer a diverse range of functions, from simple timing operations to PWM signal generation. The key to understanding how the TM operates is to see it in terms of a free running counter whose value is then compared with the value of pre-programmed internal comparators. When the free running counter has the same value as the pre-programmed comparator, known as a compare match situation, a TM interrupt signal will be generated which can clear the counter and perhaps also change the condition of the TM output pin. The internal TM counter is driven by a user selectable clock source, which can be an internal clock or an external pin.

### TM Clock Source

The clock source which drives the main counter in the TM can originate from various sources. The selection of the required clock source is implemented using the xTCK2~xTCK0 bits in the xTM control registers, where "x" can stand for S or P Type TM. The clock source can be a ratio of either the system clock $f_{SYS}$ or the internal high clock $f_H$, the $f_{SUB}$ clock source or the external xTCK pin. The xTCK pin clock source is used to allow an external signal to drive the TM as an external clock source or for event counting.

## TM Interrupts

The Standard and Periodic type TMs each has two internal interrupts, the internal comparator A or comparator P, which generate a TM interrupt when a compare match condition occurs. When a TM interrupt is generated, it can be used to clear the counter and also to change the state of the TM output pin.

## TM External Pins

Each of the TMs, irrespective of what type, has one TM input pin, with the label xTCK. The TM input pin, xTCK, is essentially a clock source for the TM and is selected using the xTCK2~xTCK0 bits in the xTMC0 register. This external TM input pin allows an external clock source to drive the internal TM. The TM input pin can be chosen to have either a rising or falling active edge.

For the STM and PTM, there is another input pin xTP, which also can be the STM or PTM output pin. The STM or PTM pin is the capture input pin whose active edge can be a rising edge, a falling edge or both rising and falling edges. The active edge transition type is selected using the STIO1~STIO0 bits in the STMC1 register or PTIO1~PTIO0 bits in the PTMC1 register. For the PTM, there is another capture input, PTCK, for PTM capture input mode, which can be used as the external trigger input source.

The TMs each have one output pins, named xTP. The TM output pin can be selected using the corresponding pin-shared function selection bits described in the Pin-shared Function section. When the TM is in the Compare Match Output Mode, these pins can be controlled by the TM to switch to a high or low level or to toggle when a compare match situation occurs. The external xTPn output pin is also the pin where the TM generates the PWM output waveform.

As the TM input or output pins are pin-shared with other functions, the TM external pin function must first be setup using registers. A single bit in the Pin-shared Function Selection Registers determines if its associated pin is to be used as an external TM pin or if it is to have another function.

| STM | | PTM | |
|---|---|---|---|
| **Input** | **Output** | **Input** | **Output** |
| STCK/STP | STP | PTCK/PTP | PTP |

**TM External Pins**

## TM Input/Output Pin Control Register

Selecting to have a TM input/output or whether to retain its other shared function is implemented using one register, with a single bit in the register corresponding to a TM input/output pin. Setting the bit high will setup the corresponding pin as a TM input/output, if reset to zero the pin will retain its original other function.
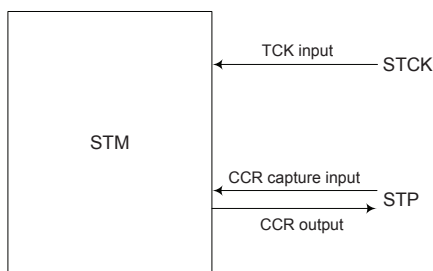


**STM Function Pin Control Block Diagram**
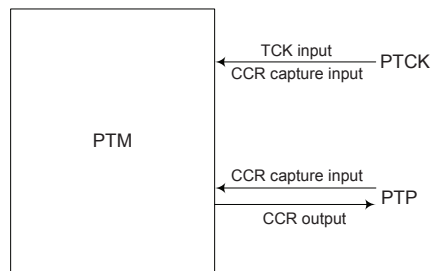
**PTM Function Pin Control Block Diagram**

## Programming Considerations

The TM Counter Registers and the Capture/Compare CCRA and CCRP registers, being 10-bit, all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to note is that data transfer to and from the 8-bit buffer and its related low byte only takes place when a write or read operation to its corresponding high byte is executed.

As the CCRA and CCRP registers are implemented in the way shown in the following diagram and accessing these registers is carried out in a specific way described above, it is recommended to use the "MOV" instruction to access the CCRA and CCRP low byte registers, named xTMAL and PTMRPL, in the following access procedures. Accessing the CCRA or CCRP low byte register without following these access procedures will result in unpredictable values.
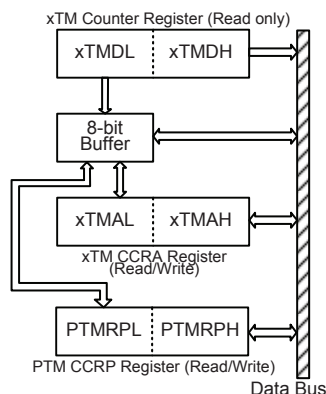


The following steps show the read and write procedures:

- Writing Data to CCRA or CCRP
  - Step 1. Write data to Low Byte xTMAL or PTMRPL
    – note that here data is only written to the 8-bit buffer.
  - Step 2. Write data to High Byte xTMAH or PTMRPH
    – here data is written directly to the high byte registers and simultaneously data is latched from the 8-bit buffer to the Low Byte registers.
- Reading Data from the Counter Registers and CCRA or CCRP
  - Step 1. Read data from the High Byte xTMDH, xTMAH or PTMRPH
    – here data is read directly from the High Byte registers and simultaneously data is latched from the Low Byte register into the 8-bit buffer.
  - Step 2. Read data from the Low Byte xTMDL, xTMAL or PTMRPL
    – this step reads data from the 8-bit buffer.

## Standard Type TM – STM

The Standard Type TM contains five operating modes, which are Compare Match Output, Timer/ Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Standard TM can be controlled with one external input pin and can drive one external output pin.
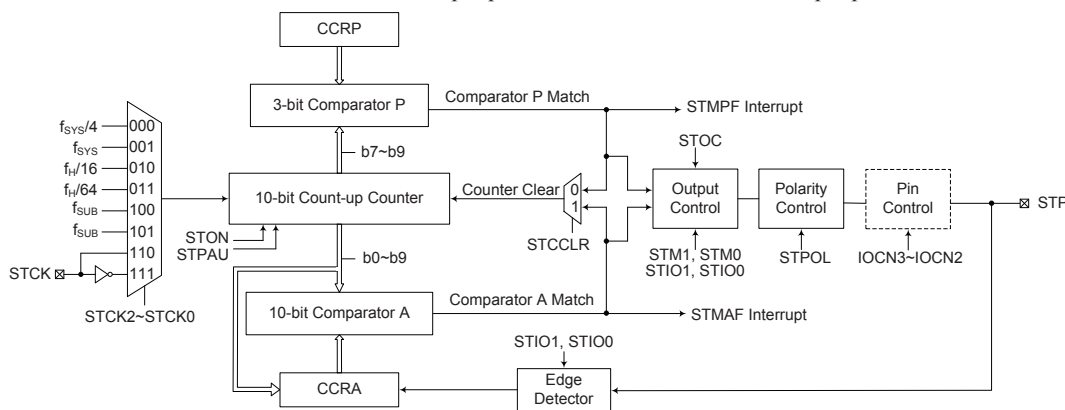


**Standard Type TM Block Diagram**

### Standard TM Operation

At its core is a 10-bit count-up counter which is driven by a user selectable internal clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP is 3-bit wide whose value is compared with the highest 3 bits in the counter while the CCRA is the 10 bits and therefore compares with all counter bits.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the STON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a STM interrupt signal will also usually be generated. The Standard Type TM can operate in a number of different operational modes, can be driven by different clock sources and can also control an output pin. All operating setup conditions are selected using relevant internal registers.

### Standard Type TM Register Description

Overall operation of the Standard TM is controlled using series of registers. A read only register pair exists to store the internal counter 10-bit value, while a read/write register pair exists to store the internal 10-bit CCRA value. The remaining two registers are control registers which setup the different operating and control modes as well as three CCRP bits.

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STMC0 | STPAU | STCK2 | STCK1 | STCK0 | STON | STRP2 | STRP1 | STRP0 |
| STMC1 | STM1 | STM0 | STIO1 | STIO0 | STOC | STPOL | STDPX | STCCLR |
| STMDL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| STMDH | — | — | — | — | — | — | D9 | D8 |
| STMAL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| STMAH | — | — | — | — | — | — | D9 | D8 |

**10-bit Standard TM Register List**

**STMC0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | STPAU | STCK2 | STCK1 | STCK0 | STON | STRP2 | STRP1 | STRP0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7      **STPAU**: STM Counter Pause Control

      0: Run

      1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the STM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4      **STCK2~STCK0**: Select STM Counter clock

      000: $f_{SYS}/4$

      001: $f_{SYS}$

      010: $f_H/16$

      011: $f_H/64$

      100: $f_{SUB}$

      101: $f_{SUB}$

      110: STCK rising edge clock

      111: STCK falling edge clock

These three bits are used to select the clock source for the STM. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source $f_{SYS}$ is the system clock, while $f_H$ and $f_{SUB}$ are other internal clocks, the details of which can be found in the oscillator section.

Bit 3      **STON**: STM Counter On/Off Control

      0: Off

      1: On

This bit controls the overall on/off function of the STM. Setting the bit high enables the counter to run, clearing the bit disables the STM. Clearing this bit to zero will stop the counter from counting and turn off the STM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again. If the STM is in the Compare Match Output Mode or the PWM output Mode or Single Pulse Output Mode then the STM output pin will be reset to its initial condition, as specified by the STOC bit, when the STON bit changes from low to high.

Bit 2~0      **STRP2 ~ STRP0**: STM CCRP 3-bit register, compared with the STM Counter bit 9~bit 7

Comparator P Match Period

      000: 1024 STM clocks

      001: 128 STM clocks

      010: 256 STM clocks

      011: 384 STM clocks

      100: 512 STM clocks

      101: 640 STM clocks

      110: 768 STM clocks

      111: 896 STM clocks

These three bits are used to setup the value on the internal CCRP 3-bit register, which are then compared with the internal counter's highest three bits. The result of this comparison can be selected to clear the internal counter if the STCCLR bit is set to zero. Setting the STCCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest three counter bits, the compare values exist in 128 clock cycle multiples. Clearing all three bits to zero is in effect allowing the counter to overflow at its maximum value.

**STMC1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STM1 | STM0 | STIO1 | STIO0 | STOC | STPOL | STDPX | STCCLR |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~6 **STM1 ~ STM0**: Select STM Operating Mode

00: Compare Match Output Mode
01: Capture Input Mode
10: PWM Output Mode or Single Pulse Output Mode
11: Timer/Counter Mode

These bits setup the required operating mode for the STM. To ensure reliable operation the STM should be switched off before any changes are made to the STM1 and STM0 bits. In the Timer/Counter Mode, the STM output pin state is undefined.

Bit 5~4 **STIO1 ~ STIO0**: Select STM function

Compare Match Output Mode
00: No change
01: Output low
10: Output high
11: Toggle output

PWM output Mode/ Single Pulse Output Mode
00: PWM Output inactive state
01: PWM Output active state
10: PWM output
11: Single pulse output

Capture Input Mode
00: Input capture at rising edge of STP
01: Input capture at falling edge of STP
10: Input capture at falling/rising edge of STP
11: Input capture disabled

Timer/counter Mode
Unused

These two bits are used to determine how the STM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the STM is running.

In the Compare Match Output Mode, the STIO1~STIO0 bits determine how the STM output pin changes state when a compare match occurs from the Comparator A. The STM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the STIO1~STIO0 bits are both zero, then no change will take place on the output. The initial value of the STM output pin should be setup using the STOC bit. Note that the output level requested by the STIO1~STIO0 bits must be different from the initial value setup using the STOC bit otherwise no change will occur on the STM output pin when a compare match occurs. After the STM output pin changes state, it can be reset to its initial level by changing the level of the STON bit from low to high.

In the PWM Output Mode, the STIO1 and STIO0 bits determine how the STM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to change the values of the STIO1 and STIO0 bits only after the STM has been switched off. Unpredictable PWM outputs will occur if the STIO1 and STIO0 bits are changed when the STM is running.

Bit 3　　　**STOC**: STM Output control bit

Compare Match Output Mode

　　0: Initial low

　　1: Initial high

PWM output Mode/ Single Pulse Output Mode

　　0: Active low

　　1: Active high

This is the output control bit for the STM output pin. Its operation depends upon whether STM is being used in the Compare Match Output Mode or in the PWM output Mode/ Single Pulse Output Mode. It has no effect if the STM is in the Timer/ Counter Mode. In the Compare Match Output Mode it determines the logic level of the STM output pin before a compare match occurs. In the PWM output Mode it determines if the PWM signal is active high or active low. In the Single Pulse Output Mode it determines the logic level of the STM output pin when the STON bit changes from low to high.

Bit 2　　　**STPOL**: STM Output polarity Control

　　0: Non-invert

　　1: Invert

This bit controls the polarity of the STM output pin. When the bit is set high the STM output pin will be inverted and not inverted when the bit is zero. It has no effect if the STM is in the Timer/Counter Mode.

Bit 1　　　**STDPX**: STM PWM period/duty Control

　　0: CCRP-period; CCRA-duty

　　1: CCRP-duty; CCRA-period

This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0　　　**STCCLR**: Select STM Counter clear condition

　　0: STM Comparator P match

　　1: STM Comparator A match

This bit is used to select the method which clears the counter. Remember that the Standard TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the STCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The STCCLR bit is not used in the PWM output mode, Single Pulse or Input Capture Mode.

**STMDL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0　　　STM Counter Low Byte Register bit 7 ~ bit 0

　　　　　　STM 10-bit Counter bit 7 ~ bit 0

**STMDH Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | D9 | D8 |
| R/W | — | — | — | — | — | — | R | R |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2　　　Unimplemented, read as "0"

Bit 1~0　　　STM Counter High Byte Register bit 1 ~ bit 0

　　　　　　STM 10-bit Counter bit 9 ~ bit 8

**STMAL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0    STM CCRA Low Byte Register bit 7 ~ bit 0
           STM 10-bit CCRA bit 7 ~ bit 0

**STMAH Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | D9 | D8 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2    Unimplemented, read as "0"

Bit 1~0    STM CCRA High Byte Register bit 1 ~ bit 0
           STM 10-bit CCRA bit 9 ~ bit 8

## Standard Type TM Operating Modes

The Standard Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the STM1 and STM0 bits in the STMC1 register.

### Compare Match Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the STCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both STMAF and STMPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the STCCLR bit in the STMC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the STMAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when STCCLR is high no STMPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA cannot be set to "0". If the CCRA bits are all zero, the counter will overflow when it reaches its maximum 10-bit, 3FF Hex, value, however here the STMAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the STM output pin, will change state. The STM output pin condition however only changes state when an STMAF interrupt request flag is generated after a compare match occurs from Comparator A. The STMPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the STM output pin. The way in which the STM output pin changes state are determined by the condition of the STIO1 and STIO0 bits in the STMC1 register. The STM output pin can be selected using the STIO1 and STIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the STM output pin, which is setup after the STON bit changes from low to high, is setup using the STOC bit. Note that if the STIO1 and STIO0 bits are zero then no pin change will take place.
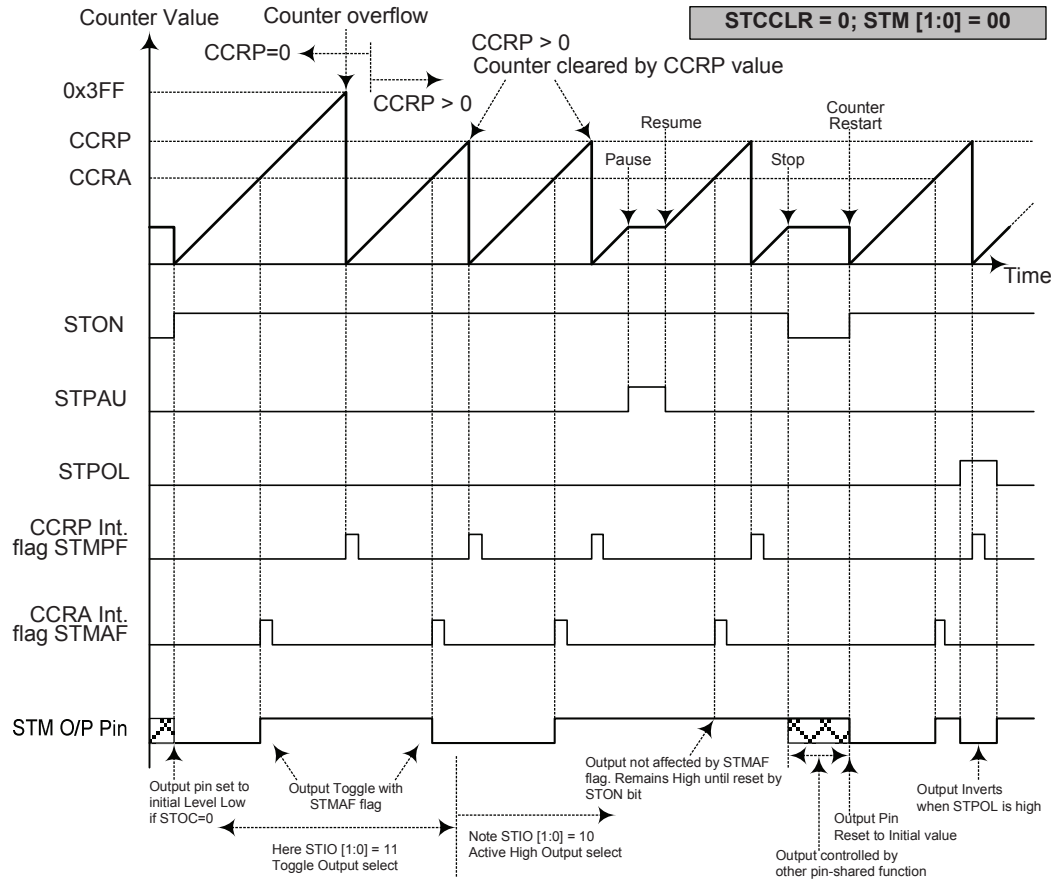
**Compare Match Output Mode – STCCLR=0**

Note: 1. With STCCLR=0 a Comparator P match will clear the counter
2. The STM output pin controlled only by the STMAF flag
3. The output pin reset to initial state by a STON bit rising edge
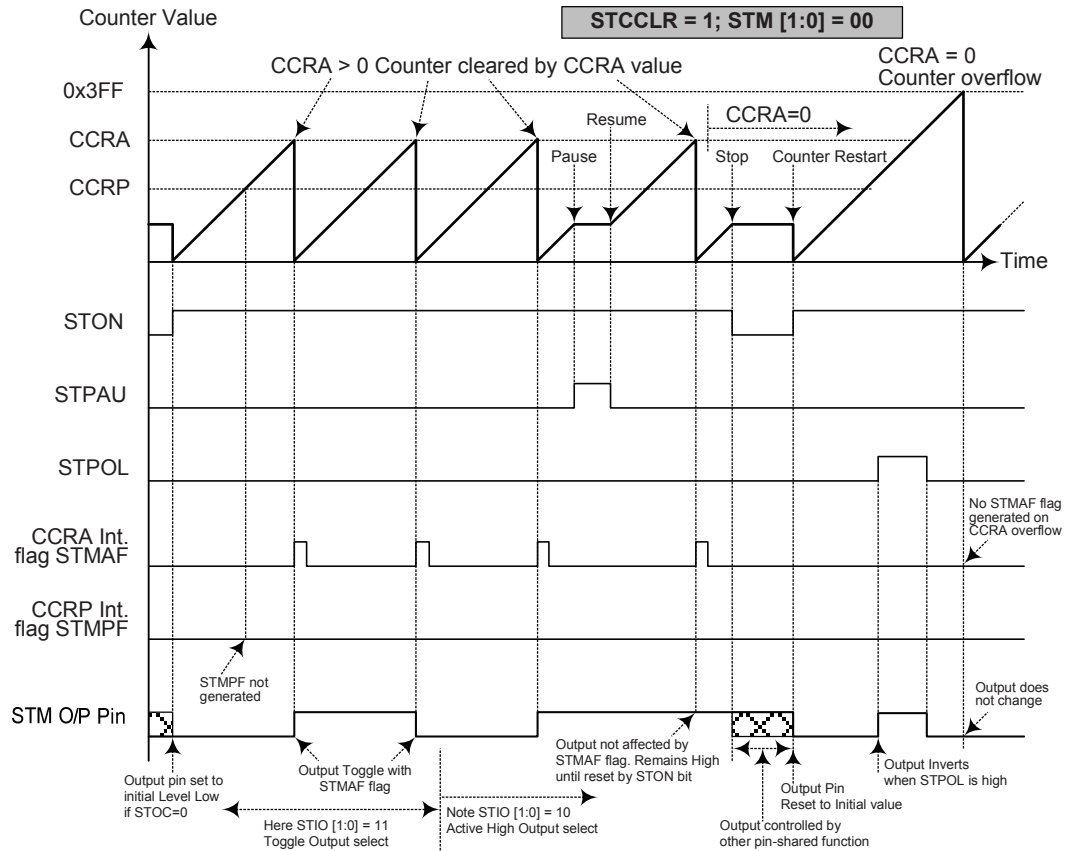
**Compare Match Output Mode – STCCLR=1**

Note: 1. With STCCLR=1 a Comparator A match will clear the counter
2. The STM output pin controlled only by the STMAF flag
3. The output pin reset to initial state by a STON rising edge
4. The STMPF flag is not generated when STCCLR=1

**Timer/Counter Mode**

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the STM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the STM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function by setting pin-share function register.

**PWM Output Mode**

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 10 respectively and also the STIO1 and STIO0 bits should be set to 10 respectively. The PWM function within the STM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the STM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM output mode, the STCCLR bit has no effect as the PWM period. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the STDPX bit in the STMC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The STOC bit in the STMC1 register is used to select the required polarity of the PWM waveform while the two STIO1 and STIO0 bits are used to enable the PWM output or to force the STM output pin to a fixed high or low level. The STPOL bit is used to reverse the polarity of the PWM output waveform.

- **10-bit STM, PWM Output Mode, Edge-aligned Mode, STDPX=0**

| CCRP | 001b | 010b | 011b | 100b | 101b | 110b | 111b | 000b |
|---|---|---|---|---|---|---|---|---|
| Period | 128 | 256 | 384 | 512 | 640 | 768 | 896 | 1024 |
| Duty | CCRA | | | | | | | |

If $f_{SYS}$=4MHz, TM clock source is $f_{SYS}$/4, CCRP=100b and CCRA =128,

The STM PWM output frequency=($f_{SYS}$/4)/512=$f_{SYS}$/2048=1.9531kHz, duty=128/512=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

- **10-bit STM, PWM Output Mode, Edge-aligned Mode, STDPX=1**

| CCRP | 001b | 010b | 011b | 100b | 101b | 110b | 111b | 000b |
|---|---|---|---|---|---|---|---|---|
| Period | CCRA | | | | | | | |
| Duty | 128 | 256 | 384 | 512 | 640 | 768 | 896 | 1024 |

The PWM output period is determined by the CCRA register value together with the STM clock while the PWM duty cycle is defined by the CCRP register value.
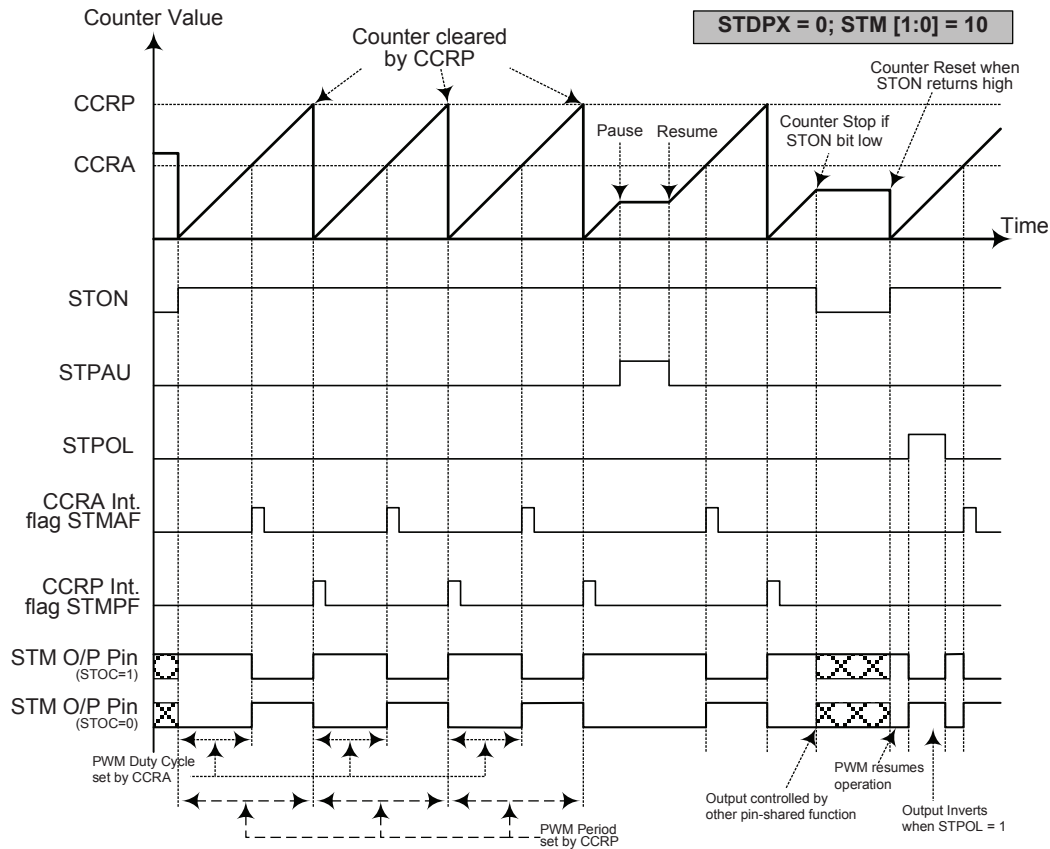
**PWM Output Mode – STDPX=0**

Note: 1. Here STDPX=0 – Counter cleared by CCRP
2. A counter clear sets PWM Period
3. The internal PWM function continues running even when STIO[1:0]=00 or 01
4. The STCCLR bit has no influence on PWM operation
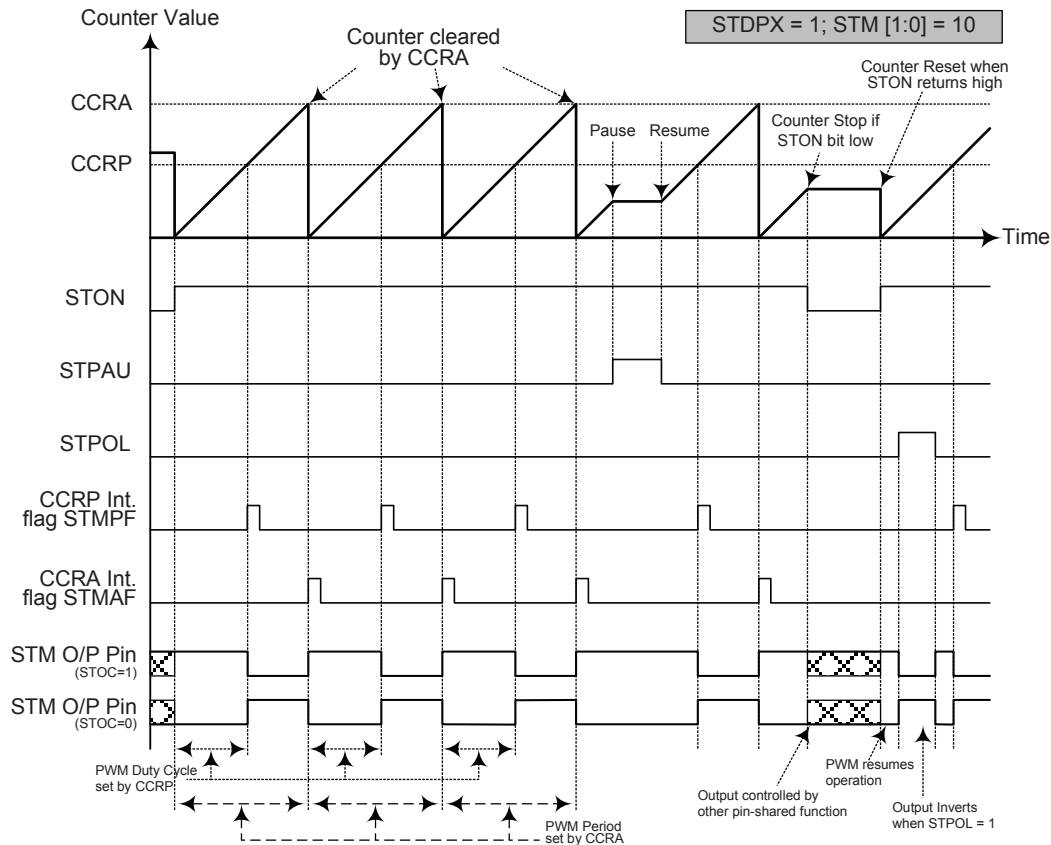
**PWM Output Mode – STDPX=1**

Note: 1. Here STDPX=1 – Counter cleared by CCRA
2. A counter clear sets PWM Period
3. The internal PWM function continues even when STIO[1:0]=00 or 01
4. The STCCLR bit has no influence on PWM operation

**Single Pulse Mode**

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 10 respectively and also the STIO1 and STIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the STM output pin.

The trigger for the pulse output leading edge is a low to high transition of the STON bit, which can be implemented using the application program. However in the Single Pulse Mode, the STON bit can also be made to automatically change from low to high using the external STCK pin, which will in turn initiate the Single Pulse output. When the STON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The STON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the STON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.
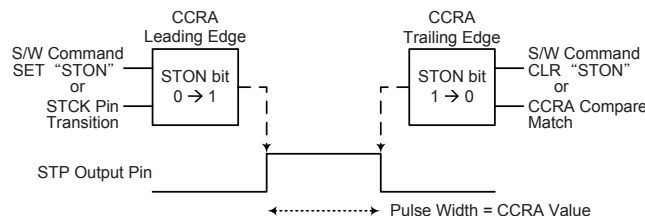


**Single Pulse Generation**
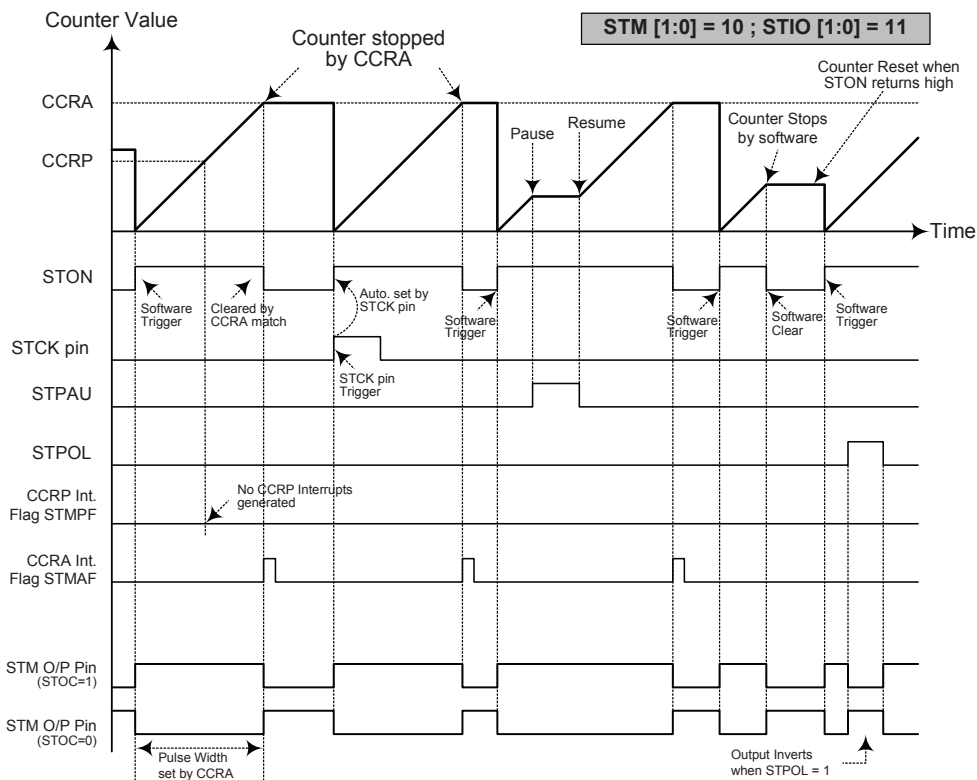


**Single Pulse Mode**

Note: 1. Counter stopped by CCRA match
2. CCRP is not used
3. The pulse is triggered by setting the STON bit high
4. In the Single Pulse Mode, STIO [1:0] must be set to "11" and cannot be changed.

However a compare match from Comparator A will also automatically clear the STON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a STM interrupt. The counter can only be reset back to zero when the STON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The STCCLR and STDPX bits are not used in this Mode.

### Capture Input Mode

To select this mode bits STM1 and STM0 in the STMC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurement. The external signal is supplied on the STP, whose active edge can be either a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the STIO1 and STIO0 bits in the STMC1 register. The counter is started when the STON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the STP the present value in the counter will be latched into the CCRA registers and a STM interrupt generated. Irrespective of what events occur on the STP the counter will continue to free run until the STON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a STM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The STIO1 and STIO0 bits can select the active trigger edge on the STP to be a rising edge, falling edge or both edge types. If the STIO1 and STIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the STP, however it must be noted that the counter will continue to run. The STCCLR and STDPX bits are not used in this Mode.
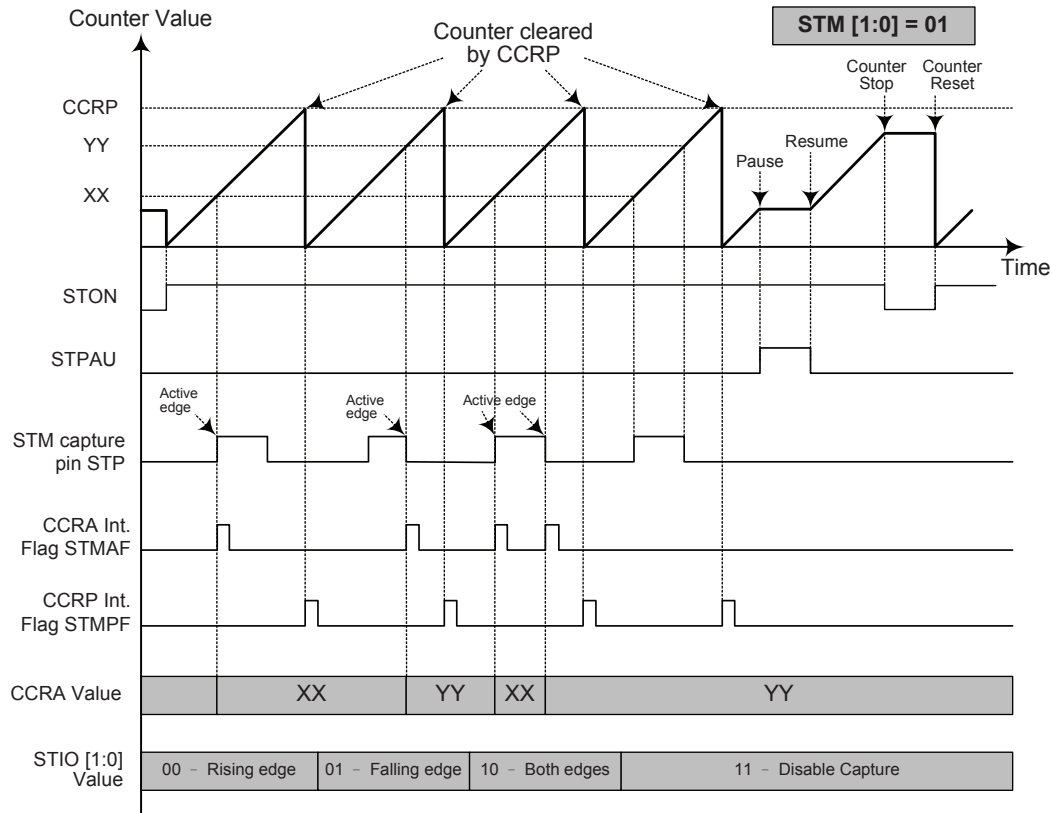
**Capture Input Mode**

Note: 1. STM[1:0]=01 and active edge set by the STIO[1:0] bits
     2. A TM Capture input pin active edge transfers the counter value to CCRA
     3. The STCCLR and STDPX bits are not used
     4. No output function – STOC and STPOL bits are not used
     5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero.

## Periodic Type TM – PTM

The Periodic Type TM contains five operating modes, which are Compare Match Output, Timer/
Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Periodic TM can
be controlled with one external input pin and can drive one external output pin.
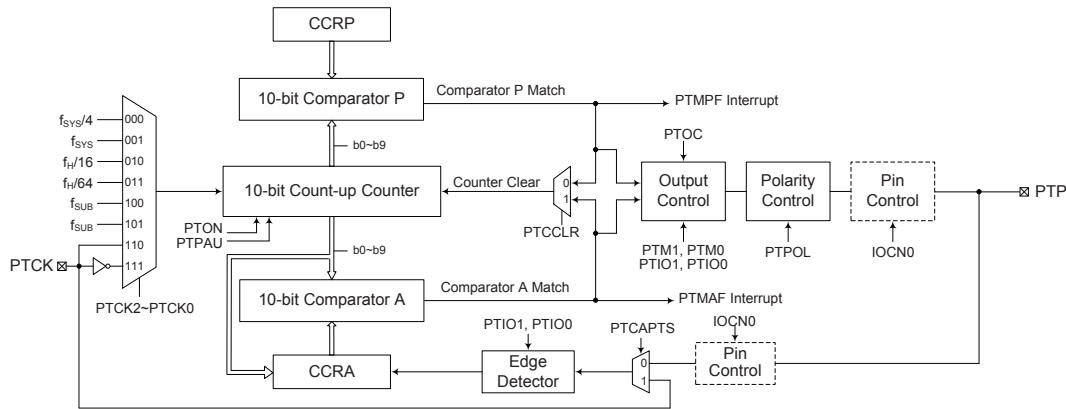


**Periodic Type TM Block Diagram**

### Periodic TM Operation

The Periodic Type TM core is a 10-bit count-up counter which is driven by a user selectable internal
or external clock source. There are also two internal comparators with the names, Comparator A
and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA
registers. The CCRP comparator is 10-bit wide.

The only way of changing the value of the 10-bit counter using the application program, is to
clear the counter by changing the PTON bit from low to high. The counter will also be cleared
automatically by a counter overflow or a compare match with one of its associated comparators.
When these conditions occur, a PTM interrupt signal will also usually be generated. The Periodic
Type TM can operate in a number of different operational modes, can be driven by different clock
sources including an input pin and can also control more than one output pin. All operating setup
conditions are selected using relevant internal registers.

### Periodic Type TM Register Description

Overall operation of the Periodic Type TM is controlled using a series of registers. A read only
register pair exists to store the internal counter 10-bit value, while two read/write register pairs exist
to store the internal 10-bit CCRA value and CCRP value. The remaining two registers are control
registers which setup the different operating and control modes.

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PTMC0 | PTPAU | PTCK2 | PTCK1 | PTCK0 | PTON | — | — | — |
| PTMC1 | PTM1 | PTM0 | PTIO1 | PTIO0 | PTOC | PTPOL | PTCAPTS | PTCCLR |
| PTMDL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PTMDH | — | — | — | — | — | — | D9 | D8 |
| PTMAL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PTMAH | — | — | — | — | — | — | D9 | D8 |
| PTMRPL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PTMRPH | — | — | — | — | — | — | D9 | D8 |

**10-bit Periodic TM Register List**

**PTMC0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------|-------|-------|-------|------|---|---|---|
| Name | PTPAU | PTCK2 | PTCK1 | PTCK0 | PTON | — | — | — |
| R/W | R/W | R/W | R/W | R/W | R/W | — | — | — |
| POR | 0 | 0 | 0 | 0 | 0 | — | — | — |

Bit 7　　　　**PTPAU**: PTM Counter Pause Control

　　　　　　0: Run
　　　　　　1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the PTM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4　　**PTCK2~PTCK0**: Select PTM Counter clock

　　　　　　000: $f_{SYS}/4$
　　　　　　001: $f_{SYS}$
　　　　　　010: $f_H/16$
　　　　　　011: $f_H/64$
　　　　　　100: $f_{SUB}$
　　　　　　101: $f_{SUB}$
　　　　　　110: PTCK rising edge clock
　　　　　　111: PTCK falling edge clock

These three bits are used to select the clock source for the PTM. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source $f_{SYS}$ is the system clock, while $f_H$ and $f_{SUB}$ are other internal clocks, the details of which can be found in the oscillator section.

Bit 3　　　　**PTON**: PTM Counter On/Off Control

　　　　　　0: Off
　　　　　　1: On

This bit controls the overall on/off function of the PTM. Setting the bit high enables the counter to run, clearing the bit disables the PTM. Clearing this bit to zero will stop the counter from counting and turn off the PTM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again.

If the PTM is in the Compare Match Output Mode, PWM output Mode or Single Pulse Output Mode then the PTM output pin will be reset to its initial condition, as specified by the PTOC bit, when the PTON bit changes from low to high.

Bit 2~0　　Unimplemented, read as "0"

**PTMC1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|-------|-------|------|-------|---------|---------|
| Name | PTM1 | PTM0 | PTIO1 | PTIO0 | PTOC | PTPOL | PTCAPTS | PTCCLR |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~6     **PTM1~PTM0**: Select PTM Operating Mode
     00: Compare Match Output Mode
     01: Capture Input Mode
     10: PWM Output Mode or Single Pulse Output Mode
     11: Timer/Counter Mode

These bits setup the required operating mode for the PTM. To ensure reliable operation the PTM should be switched off before any changes are made to the PTM1 and PTM0 bits. In the Timer/Counter Mode, the PTM output pin state is undefined.

Bit 5~4     **PTIO1~PTIO0**: Select PTM pin PTP or PTCK function

Compare Match Output Mode
     00: No change
     01: Output low
     10: Output high
     11: Toggle output

PWM Output Mode/Single Pulse Output Mode
     00: PWM Output inactive state
     01: PWM Output active state
     10: PWM output
     11: Single pulse output

Capture Input Mode
     00: Input capture at rising edge of PTP or PTCK
     01: Input capture at falling edge of PTP or PTCK
     10: Input capture at falling/rising edge of PTP or PTCK
     11: Input capture disabled

Timer/Counter Mode
     Unused

These two bits are used to determine how the PTM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the PTM is running.

In the Compare Match Output Mode, the PTIO1 and PTIO0 bits determine how the PTM output pin changes state when a compare match occurs from the Comparator A. The PTM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the PTM output pin should be setup using the PTOC bit in the PTMC1 register. Note that the output level requested by the PTIO1 and PTIO0 bits must be different from the initial value setup using the PTOC bit otherwise no change will occur on the PTM output pin when a compare match occurs. After the PTM output pin changes state, it can be reset to its initial level by changing the level of the PTON bit from low to high.

In the PWM Output Mode, the PTIO1 and PTIO0 bits determine how the PTM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the PTIO1 and PTIO0 bits only after the TM has been switched off. Unpredictable PWM outputs will occur if the PTIO1 and PTIO0 bits are changed when the PTM is running.

Bit 3     **PTOC**: PTM PTP Output control bit

Compare Match Output Mode

    0: Initial low

    1: Initial high

PWM Output Mode/Single Pulse Output Mode

    0: Active low

    1: Active high

This is the output control bit for the PTM output pin. Its operation depends upon whether PTM is being used in the Compare Match Output Mode or in the PWM Output Mode/Single Pulse Output Mode. It has no effect if the PTM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the PTM output pin before a compare match occurs. In the PWM Output Mode it determines if the PWM signal is active high or active low.

Bit 2     **PTPOL**: PTM PTP Output polarity Control

    0: Non-invert

    1: Invert

This bit controls the polarity of the PTP output pin. When the bit is set high the PTM output pin will be inverted and not inverted when the bit is zero. It has no effect if the PTM is in the Timer/Counter Mode.

Bit 1     **PTCAPTS**: PTM Capture Trigger Source Selection

    0: From PTP pin

    1: From PTCK pin

Bit 0     **PTCCLR**: Select PTM Counter clear condition

    0: PTM Comparator P match

    1: PTM Comparator A match

This bit is used to select the method which clears the counter. Remember that the Periodic TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the PTCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The PTCCLR bit is not used in the PWM Output Mode, Single Pulse or Capture Input Mode.

### PTMDL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0     **D7~D0**: PTM Counter Low Byte Register bit 7 ~ bit 0

PTM 10-bit Counter bit 7 ~ bit 0

### PTMDH Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | D9 | D8 |
| R/W | — | — | — | — | — | — | R | R |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2     Unimplemented, read as "0"

Bit 1~0     **D9~D8**: PTM Counter High Byte Register bit 1 ~ bit 0

PTM 10-bit Counter bit 9 ~ bit 8

**PTMAL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0  **D7~D0**: PTM CCRA Low Byte Register bit 7 ~ bit 0
PTM 10-bit CCRA bit 7 ~ bit 0

**PTMAH Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | — | — | — | — | — | — | D9 | D8 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2  Unimplemented, read as "0"

Bit 1~0  **D9~D8**: PTM CCRA High Byte Register bit 1 ~ bit 0
PTM 10-bit CCRA bit 9 ~ bit 8

**PTMRPL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0  **D7~D0**: PTM CCRP Low Byte Register bit 7 ~ bit 0
PTM 10-bit CCRP bit 7 ~ bit 0

**PTMRPH Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | — | — | — | — | — | — | D9 | D8 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2  Unimplemented, read as "0"

Bit 1~0  **D9~D8**: PTM CCRP High Byte Register bit 1 ~ bit 0
PTM 10-bit CCRP bit 9 ~ bit 8

### Periodic Type TM Operating Modes

The Periodic Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the PTM1 and PTM0 bits in the PTMC1 register.
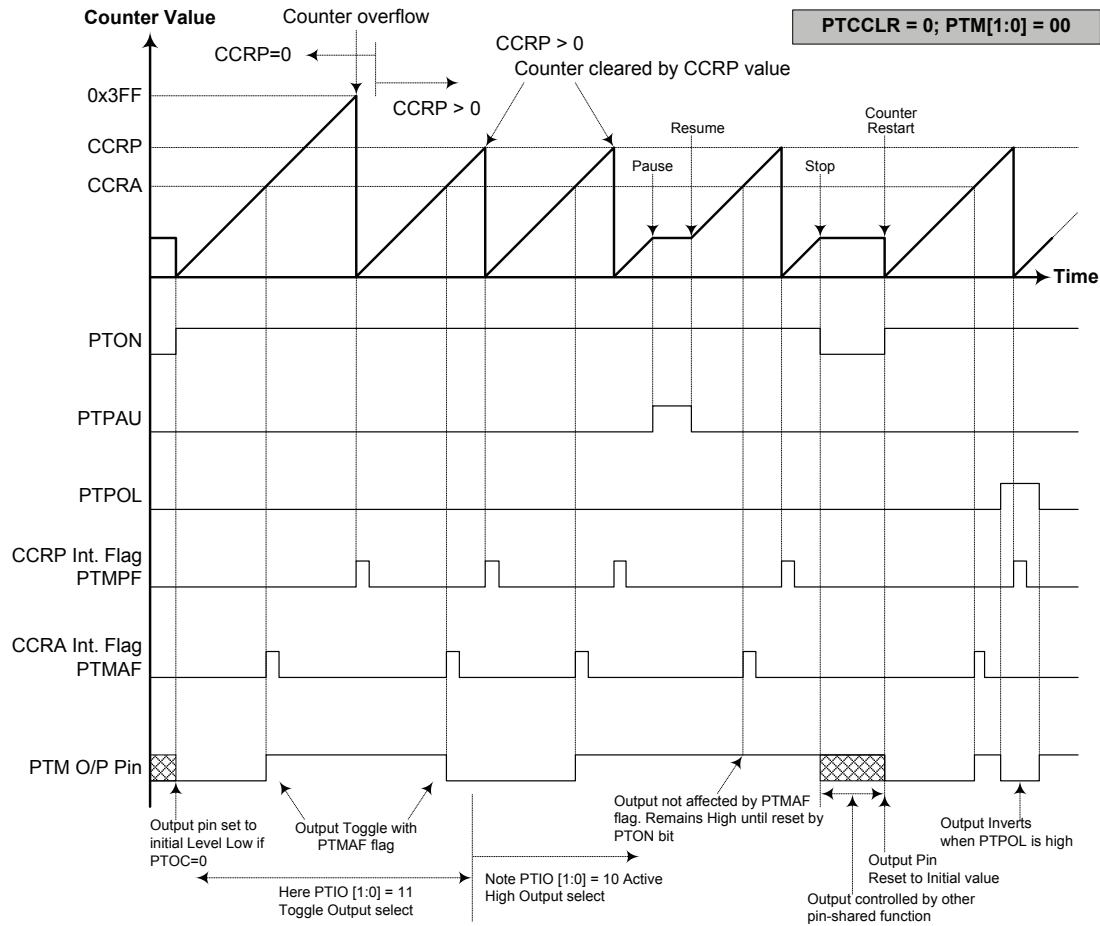
#### Compare Match Output Mode

To select this mode, bits PTM1 and PTM0 in the PTMC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the PTCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both PTMAF and PTMPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the PTCCLR bit in the PTMC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the PTMAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when PTCCLR is high no PTMPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA can not be cleared to zero.

If the CCRA bits are all zero, the counter will overflow when its reaches its maximum 10-bit, 3FF Hex, value, however here the PTMAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the PTM output pin, will change state. The PTM output pin condition however only changes state when a PTMAF interrupt request flag is generated after a compare match occurs from Comparator A. The PTMPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the PTM output pin. The way in which the PTM output pin changes state are determined by the condition of the PTIO1 and PTIO0 bits in the PTMC1 register. The PTM output pin can be selected using the PTIO1 and PTIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the PTM output pin, which is setup after the PTON bit changes from low to high, is setup using the PTOC bit. Note that if the PTIO1 and PTIO0 bits are zero then no pin change will take place.

**Compare Match Output Mode – PTCCLR=0**

Note: 1. With PTCCLR=0 a Comparator P match will clear the counter
    2. The PTM output pin is controlled only by the PTMAF flag
    3. The output pin is reset to its initial state by a PTON bit rising edge
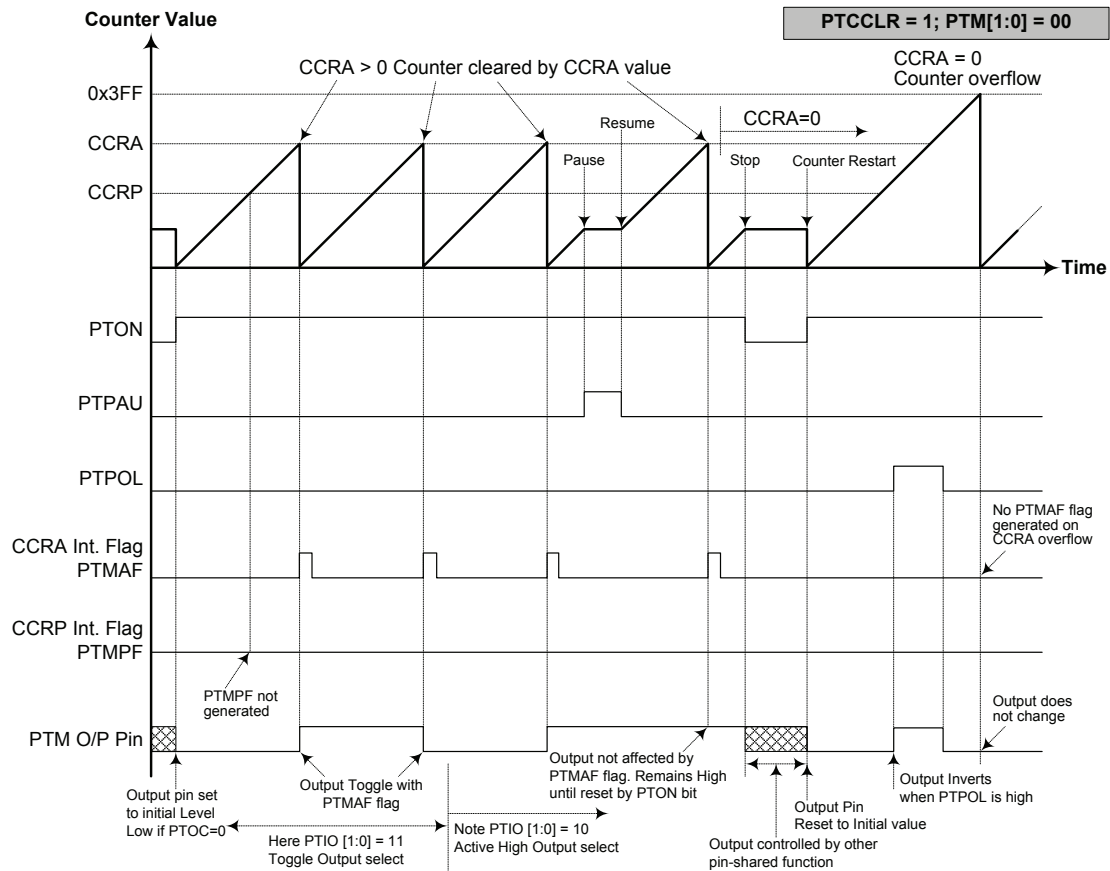
**Compare Match Output Mode – PTCCLR=1**

Note: 1. With PTCCLR=1 a Comparator A match will clear the counter

2. The PTM output pin is controlled only by the PTMAF flag

3. The output pin is reset to its initial state by a PTON bit rising edge

4. A PTMPF flag is not generated when PTCCLR=1

**Timer/Counter Mode**

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the TM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

**PWM Output Mode**

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 10 respectively. The PWM function within the PTM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the PTM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM Output Mode, the PTCCLR bit has no effect on the PWM operation. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The PTOC bit in the PTMC1 register is used to select the required polarity of the PWM waveform while the two PTIO1 and PTIO0 bits are used to enable the PWM output or to force the PTM output pin to a fixed high or low level. The PTPOL bit is used to reverse the polarity of the PWM output waveform.

- **10-bit PTM, PWM Output Mode, Edge-aligned Mode**

| CCRP | 1~1023 | 0 |
|---|---|---|
| Period | 1~1023 | 1024 |
| Duty | CCRA | |

If $f_{SYS}$=12MHz, PTM clock source select $f_{SYS}$/4, CCRP=512 and CCRA=128,

The PTM PWM output frequency=$(f_{SYS}/4)/512$=$f_{SYS}/2048$=5.8594kHz, duty=128/(2×256)=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

**PWM Output Mode**
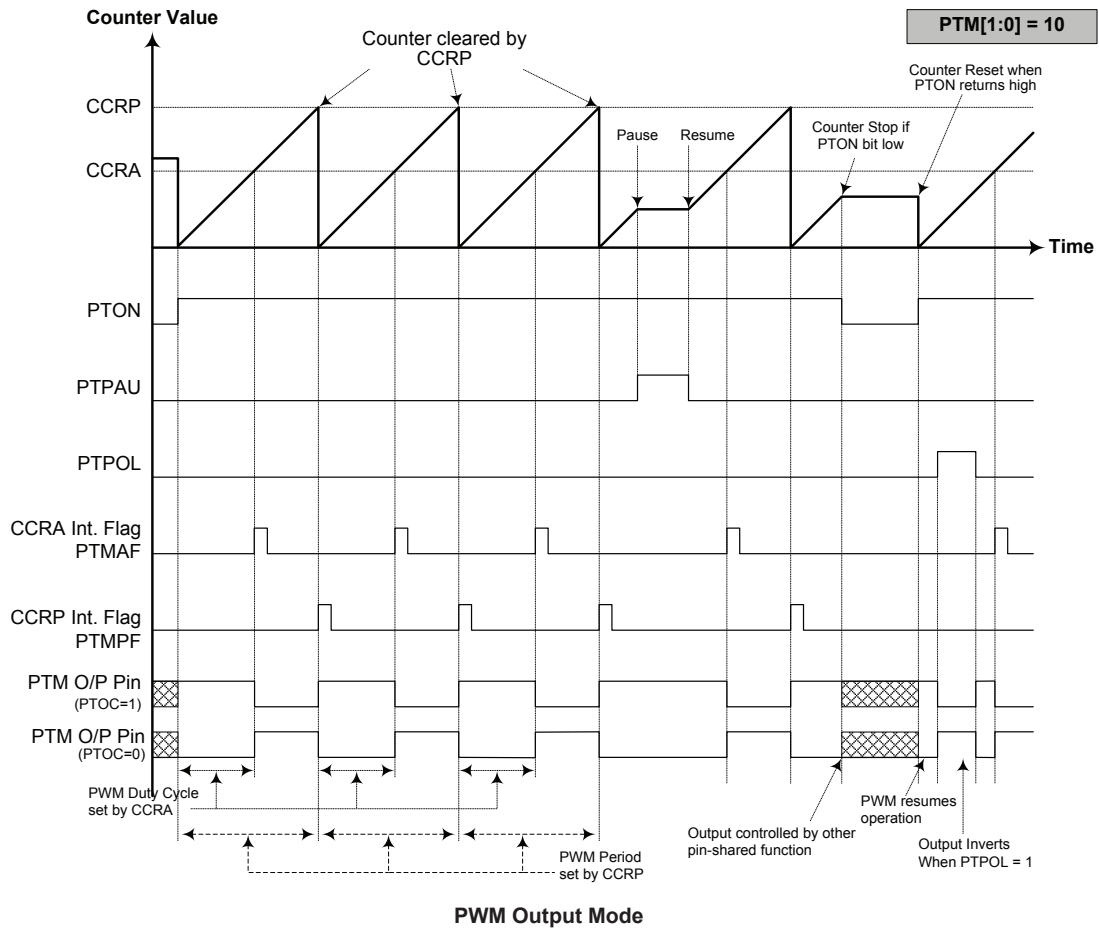
Note: 1. Counter cleared by CCRP
    2. A counter clear sets the PWM Period
    3. The internal PWM function continues running even when PTIO[1:0]=00 or 01
    4. The PTCCLR bit has no influence on PWM operation

**Single Pulse Mode**

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 10 respectively and also the PTIO1 and PTIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the PTM output pin.

The trigger for the pulse output leading edge is a low to high transition of the PTON bit, which can be implemented using the application program. However in the Single Pulse Mode, the PTON bit can also be made to automatically change from low to high using the external PTCK pin, which will in turn initiate the Single Pulse output. When the PTON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The PTON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the PTON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the PTON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a PTM interrupt. The counter can only be reset back to zero when the PTON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The PTCCLR bit is not used in this Mode.



**Single Pulse Generation**

**Single Pulse Mode**
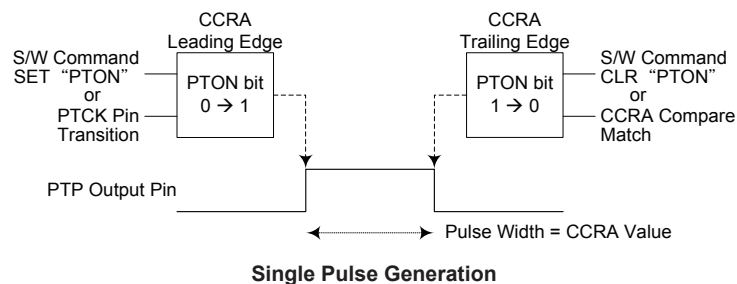
Note: 1. Counter stopped by CCRA
2. CCRP is not used
3. The pulse is triggered by the PTCK pin or by setting the PTON bit high
4. A PTCK pin active edge will automatically set the PTON bit high
5. In the Single Pulse Mode, PTIO[1:0] must be set to "11" and cannot be changed.

**Capture Input Mode**

To select this mode bits PTM1 and PTM0 in the PTMC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the PTP or PTCK pin which is selected using the PTCAPTS bit in the PTMC1 register. The input pin active edge can be either a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the PTIO1 and PTIO0 bits in the PTMC1 register. The counter is started when the PTON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the PTP or PTCK pin the present value in the counter will be latched into the CCRA registers and a PTM interrupt generated. Irrespective of what events occur on the PTP or PTCK pin, the counter will continue to free run until the PTON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a PTM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The PTIO1 and PTIO0 bits can select the active trigger edge on the PTP or PTCK pin to be a rising edge, falling edge or both edge types. If the PTIO1 and PTIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the PTP or PTCK pin, however it must be noted that the counter will continue to run.

As the PTP or PTCK pin is pin shared with other functions, care must be taken if the PTM is in the Capture Input Mode. This is because if the pin is setup as an output, then any transitions on this pin may cause an input capture operation to be executed. The PTCCLR, PTOC and PTPOL bits are not used in this Mode.
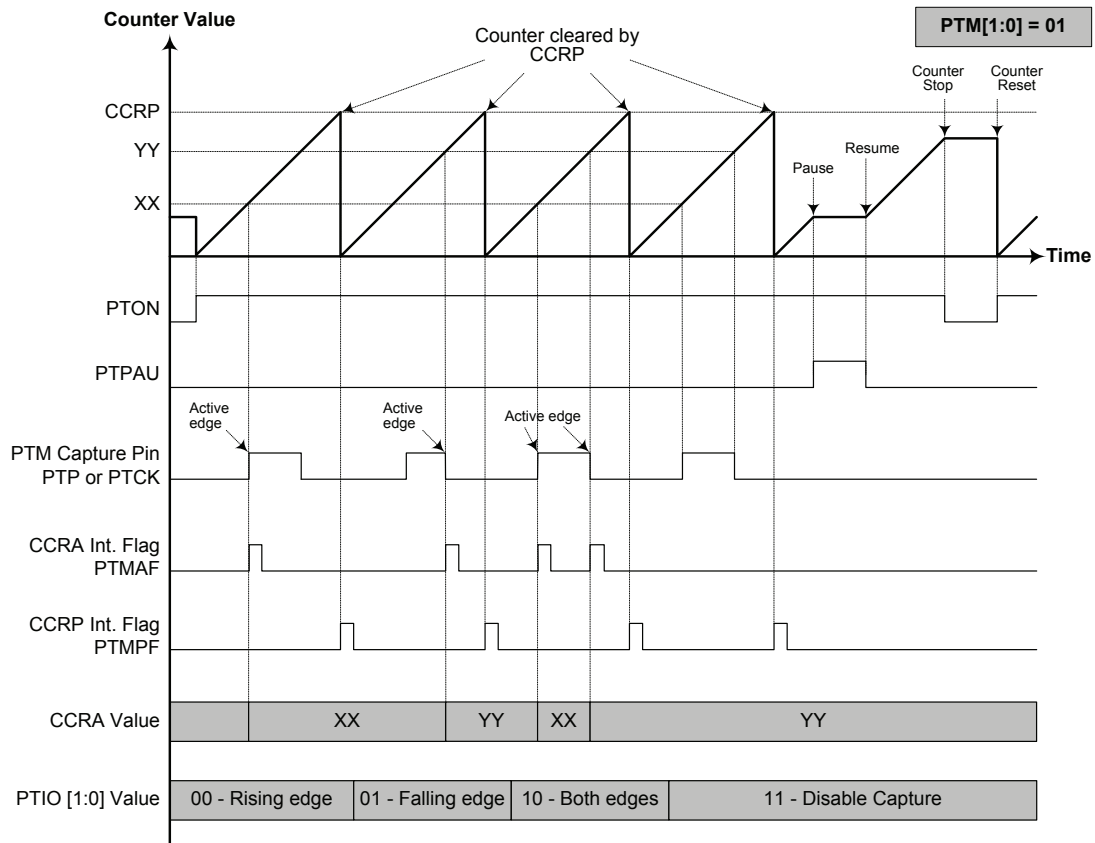
**Capture Input Mode**

Note: 1. PTM[1:0]=01 and active edge set by the PTIO[1:0] bits

    2. A PTM Capture input pin active edge transfers the counter value to CCRA

    3. PTCCLR bit not used

    4. No output function – PTOC and PTPOL bits are not used

    5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero.

## Nebuliser Resonance Detector

Please refer Holtek Applicatoin Notes.

## Water Shortage Protection

Developed by users.

## Over Current/Voltage Protection

The device includes an over current/voltage protection function which provides an over current or over voltage protection protection mechanism for applications. The current on the OCVPAI0 pin is converted to a relevant voltage level according to the current value using the OCVP operational amplifier. It is then compared with a reference voltage generated by an 8-bit D/A converter. The voltage on the OCVPCI pin is compared with a reference voltage generated by the 8-bit D/A converter. When the OCVPF flag changes from 0 to 1 and if the corresponding interrupt control is enabled, an OCVP interrupt will be generated to indicate a specific current or voltage condition has occurred.
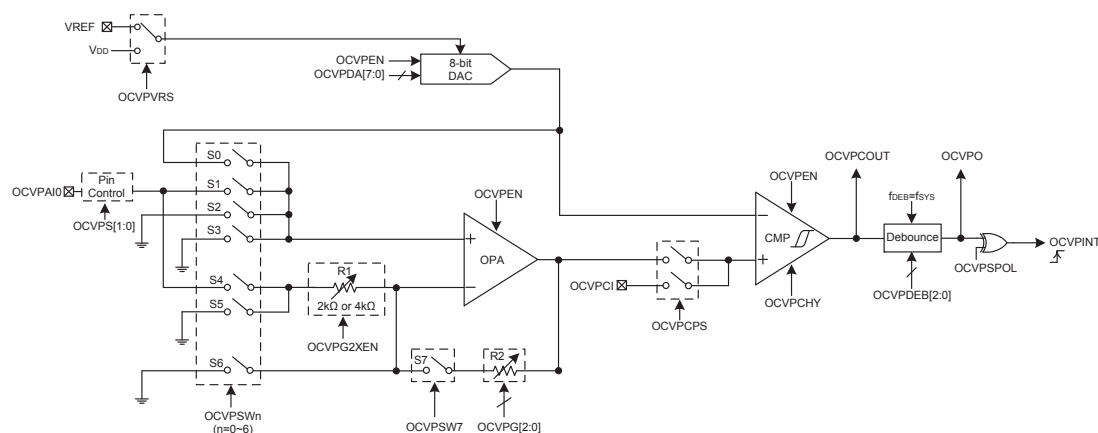


**OCVP Block Diagram**

### OCVP Operation

The OCVP circuit is used to prevent the input current or voltage from being in an unexpected level range. The current on the OCVPAI0 pin is converted to a voltage and then amplified by the OCVP operational amplifier with a programmable gain from 1 to 65 selected by the OCVPG2~OCVPG0 bits in the OCVPC2 register. This is known as the Programmable Gain Amplifier or PGA. This PGA can also be configured to operate in the non-inverting, inverting or input offset cancellation mode determined by the OCVPSW7~OCVPSW0 bits in the OCVPC0 register. After the current is converted and amplified to a specific voltage level, it will be compared with a reference voltage provided by an 8-bit D/A converter. The voltage on the OCVPCI pin is also can be selected to compare with a reference provided by the 8-bit D/A converter.

To compare the OCVPAO output signal or the OCVPCI input signal with the D/A converter output voltage is selected using the OCVPCPS bit in the OCVPC1 register. The 8-bit D/A converter power can be supplied by the external power pin, VDD or VREF, selected by the OCVPVRS bit in the OCVPC1 register. The comparator output, OCVPCOUT, will first be filtered with a certain debounce time period selected by the OCVPDEB2~OCVPDEB0 bits in the OCVPC2 register. Then a filtered OCVP digital comparator output, OCVPO, is obtained to indicate whether a user-defined current or voltage condition occurs or not.

If the OCVPSPOL bit is cleared to 0 and the comparator inputs force the OCVPO bit to change from 0 to 1, or if the OCVPSPOL bit is set to 1 and the comparator inputs force the OCVPO bit changes from 1 to 0, the corresponding interrupt will be generated if the relevant interrupt control bit is enabled. It is important to note that, only an OCVPINT rising edge can trigger an OCVP interrupt request, so the OCVPSPOL bit must be properly configured according to user's application requirements. The comparator in the OCVP circuit also has hysteresis function controlled by OCVPCHY bit.

Note that the debounce clock, $f_{DEB}$, comes from the system clock, $f_{SYS}$. The DAC output voltage is controlled by the OCVPDA register and the DAC output is defined as below:

$$DAC\ V_{OUT}=(DAC\ reference\ voltage/256) \times D[7:0]$$

## OCVP Control Registers

Overall operation of the OCVP function is controlled using several registers. The CTRL2 register is used to select the OCVP input signal input pin. One register is used to provide the reference voltages for the OCVP circuit. Two registers are used for the operational amplifier and comparator input offset calibration. The remaining three registers are control registers which control the OCVP function, D/A converter reference voltage select, switches on/off control, PGA gain select, comparator non-inverting input select, comparator de-bounce time, comparator hysteresis function and comparator output polarity control, etc. For a more detailed description regarding the input offset voltage cancellation procedures, refer to the corresponding input offset cancellation sections.

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CTRL2 | — | — | — | — | — | — | OCVPS1 | OCVPS0 |
| OCVPDA | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OCVPC0 | OCVPSW7 | OCVPSW6 | OCVPSW5 | OCVPSW4 | OCVPSW3 | OCVPSW2 | OCVPSW1 | OCVPSW0 |
| OCVPC1 | OCVPEN | OCVPCHY | OCVPO | OCVPSPOL | — | — | OCVPCPS | OCVPVRS |
| OCVPC2 | — | OCVPG2XEN | OCVPG2 | OCVPG1 | OCVPG0 | OCVPDEB2 | OCVPDEB1 | OCVPDEB0 |
| OCVPOCAL | OCVPOOFM | OCVPORSP | OCVPOOF5 | OCVPOOF4 | OCVPOOF3 | OCVPOOF2 | OCVPOOF1 | OCVPOOF0 |
| OCVPCCAL | OCVPCOUT | OCVPCOFM | OCVPCRSP | OCVPCOF4 | OCVPCOF3 | OCVPCOF2 | OCVPCOF1 | OCVPCOF0 |

OCVP Register List

### CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | OCVPS1 | OCVPS0 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| POR | — | — | — | — | — | — | 0 | 0 |

Bit 7~2     Unimplemented, read as "0"

Bit 1~0     **OCVPS1 ~ OCVPS0**: OCVPAI0 Input Source Pin Selection
    00: OCVPAI0 on PA4
    01: OCVPAI0 on PA3
    10: OCVPAI0 on PA6
    11: OCVPAI0 on PA7

**OCVPC0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | OCVPSW7 | OCVPSW6 | OCVPSW5 | OCVPSW4 | OCVPSW3 | OCVPSW2 | OCVPSW1 | OCVPSW0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

Bit 7　　**OCVPSW7**: OCVP switch S7 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 6　　**OCVPSW6**: OCVP switch S6 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 5　　**OCVPSW5**: OCVP switch S5 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 4　　**OCVPSW4**: OCVP switch S4 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 3　　**OCVPSW3**: OCVP switch S3 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 2　　**OCVPSW2**: OCVP switch S2 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 1　　**OCVPSW1**: OCVP switch S1 on/off control
　　　　　　0: Off
　　　　　　1: On

Bit 0　　**OCVPSW0**: OCVP switch S0 on/off control
　　　　　　0: Off
　　　　　　1: On

**OCVPC1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | OCVPEN | OCVPCHY | OCVPO | OCVPSPOL | — | — | OCVPCPS | OCVPVRS |
| R/W | R/W | R/W | R | R/W | — | — | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | — | — | 0 | 0 |

Bit 7　　**OCVPEN**: OCVP function enable control
　　　　　　0: Disable
　　　　　　1: Enable
　　　　　When this bit is cleared to 0, the overall OCVP operation will be disabled and the comparator output, OCVPCOUT, will be equal to 0.

Bit 6　　**OCVPCHY**: OCVP Comparator Hysteresis function control
　　　　　　0: Disable
　　　　　　1: Enable

Bit 5　　**OCVPO**: OCVP Comparator debounce output
　　　　　This bit is the debounce version of the OCVPCOUT bit.

Bit 4　　**OCVPSPOL**: OCVPO polarity control
　　　　　　0: Non-invert
　　　　　　1: Invert

Bit 3~2　　Unimplemented, read as "0"

Bit 1　　**OCVPCPS**: OCVP Comparator non-inverting input selection
　　　　0: From OCVPAO signal
　　　　1: From OCVPCI pin

Bit 0　　**OCVPVRS**: OCVP D/A Converter reference voltage selection
　　　　0: From $V_{DD}$
　　　　1: From VREF pin

**OCVPC2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | OCVPG2XEN | OCVPG2 | OCVPG1 | OCVPG0 | OCVPDEB2 | OCVPDEB1 | OCVPDEB0 |
| R/W | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7　　Unimplemented, read as "0"

Bit 6　　**OCVPG2XEN**: R2/R1 ratio doubling enable control
　　　　0: Disable (R1=4kΩ)
　　　　1: Enable (R1=2kΩ)
　　　　When this bit is 1, the R2/R1 ratio selected by the OCVPG2~OCVPG0 bits will be doubled.

Bit 5~3　**OCVPG2~OCVPG0**: PGA R2/R1 ratio selection
　　　　000: R2/R1=1
　　　　001: R2/R1=4
　　　　010: R2/R1=6
　　　　011: R2/R1=10
　　　　100: R2/R1=15
　　　　101: R2/R1=25
　　　　110: R2/R1=40
　　　　111: R2/R1=65
　　　　The internal resistors, R1 and R2, should be used when the gain is determined by these bits. This means the S4 or S5 switch together with the S7 switch should be on. Otherwise, the gain accuracy will not be guaranteed. When the OCVPG2XEN bit is set to 1 to enable the R2/R1 ratio doubling function, the above R2/R1 values will be doubled. The calculating formula of the PGA gain for the inverting and non-inverting mode is described in the "Input Voltage Range" section.

Bit 2~0　**OCVPDEB2~OCVPDEB0**: OCVP Comparator output debounce time control
　　　　000: Bypass, no debounce
　　　　001: $(1\sim2) \times t_{DEB}$
　　　　010: $(3\sim4) \times t_{DEB}$
　　　　011: $(7\sim8) \times t_{DEB}$
　　　　100: $(15\sim16) \times t_{DEB}$
　　　　101: $(31\sim32) \times t_{DEB}$
　　　　110: $(63\sim64) \times t_{DEB}$
　　　　111: $(127\sim128) \times t_{DEB}$
　　　　Note: $f_{DEB}=f_{SYS}, t_{DEB}=1/f_{DEB}$

**OCVPDA Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0　OCVP D/A Converter Data Register bit 7 ~ bit 0
　　　　OCVP D/A Converter Output=(DAC reference voltage/256) × D[7:0]

**OCVPOCAL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | OCVPOOFM | OCVPORSP | OCVPOOF5 | OCVPOOF4 | OCVPOOF3 | OCVPOOF2 | OCVPOOF1 | OCVPOOF0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Bit 7      **OCVPOOFM**: OCVP Operational Amplifier operating mode selection
         0: Normal operating mode
         1: Offset cancellation mode
     This bit is used to select the OCVP operating mode. To select the operational amplifier input offset cancellation mode, the OCVPSW7~OCVPSW0 bits must first be set to 28H and then the OCVPOOFM bit must be set to 1 followed by the OCVPCOFM bit being cleared to 0. Refer to the "Operational Amplifier Input Offset Cancellation" section for the detailed offset cancellation procedures.

Bit 6      **OCVPORSP**: OCVP Operational Amplifier input offset voltage cancellation reference selection
         0: Operational amplifier inverting input is selected
         1: Operational amplifier non-verting input is selected

Bit 5~0      **OCVPOOF5~OCVPOOF0**: OCVP Operational Amplifier input offset voltage cancellation value
     This 6-bit field is used to perform the operational amplifier input offset cancellation operation and the value for the OCVP operational amplifier input offset cancellation can be restored into this bit field. More detailed information is described in the "Operational Amplifier Input Offset Cancellation" section.

**OCVPCCAL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | OCVPCOUT | OCVPCOFM | OCVPCRSP | OCVPCOF4 | OCVPCOF3 | OCVPCOF2 | OCVPCOF1 | OCVPCOF0 |
| R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Bit 7      **OCVPCOUT**: OCVP Comparator output
         0: Non-verting input voltage **<** DAC output voltage
         1: Non-verting input voltage **>** DAC output voltage
     This bit is used to indicate whether the non-verting input voltage is greater than the DAC output voltage. If the OCVPCOUT is set to 1, the non-verting input voltage is greater than the DAC output voltage. Otherwise, the non-verting input voltage is less than the DAC output voltage. This bit value can be output on the OCVPCOUT pin.

Bit 6      **OCVPCOFM**: OCVP Comparator operating mode selection
         0: Normal operating mode
         1: Offset cancellation mode
     This bit is used to select the OCVP comparator operating mode. To select the comparator input offset cancellation mode, the OCVPSW7~OCVPSW0 bits must first be set to 28H and then the OCVPCOFM bit must be set to 1 followed by the OCVPOOFM bit being cleared to 0. Refer to the "Comparator Input Offset Cancellation" section for the detailed offset cancellation procedures.

Bit 5      **OCVPCRSP**: OCVP Comparator input offset voltage cancellation reference selection
         0: Inverting input as the reference input
         1: Non-inverting input is selected as the reference input

Bit 4~0      **OCVPCOF4~OCVPCOF0**: OCVP Comparator input offset voltage cancellation value
     This 5-bit field is used to perform the comparator input offset cancellation operation and the value for the OCVP comparator input offset cancellation can be restored into this bit field. More detailed information is described in the "Comparator Input Offset Cancellation" section.

### Input Voltage Range

Together with different PGA operating modes, the input voltage can be positive or negative to provide diverse applications for the device. The PGA output for the positive or negative input voltage is respectively calculated based on different formulas and described by the following examples.

- For $V_{IN} > 0$, the PGA operates in the non-inverting mode and the PGA output is obtained using the formula below:

$$V_{OUT} = (1 + \frac{R_2}{R_1}) \times V_{IN}$$

- When the PGA operates in the non-inverting mode, a unity gain buffer is provided. If OCVPSW6~OCVPSW4 bits are set to "000", the PGA gain will be 1 and the PGA will act as a unity gain buffer. The switches S6, S5 and S4 will be off internally and the output voltage of PGA is:

$$V_{OUT} = V_{IN}$$

- If S3 and S4 are on, the input node is OCVPAI0. For input voltage $0 > V_{IN} > -0.4$, the PGA operates in the inverting mode and the PGA output is obtained using the formula below. Note that if the input voltage $V_{IN}$ is negative, it can not be lower than -0.4V which will result in current leakage.

$$V_{OUT} = -\frac{R_2}{R_1} \times V_{IN}$$

### Offset Calibration

To operate in the input offset cancellation mode for the OCVP circuit, the OCVPSW7~OCVPSW0 bits should first be set to 28H. For operational amplifier and comparator input offset cancellation, the procedures are similar except for setting the respective control bits.

#### Operational Amplifier Input Offset Cancellation

Step 1. Set OCVPSW [7:0]=28H (S3 and S5 are on, other switches are off), OCVPOOFM=1, OCVPCOFM=0 and OCVPORSP=1, the OCVP will operate in the operational amplifier input offset cancellation mode.

Step 2. Set OCVPDA [7:0]=40H

Step 3. Set OCVPOOF [5:0]=000000 and read the OCVPCOUT bit.

Step 4. Increase the OCVPOOF [5:0] value by 1 and then read the OCVPCOUT bit.
   If the OCVPCOUT bit state has not changed, then repeat Step 4 until the OCVPCOUT bit state has changed.
   If the OCVPCOUT bit state has changed, record the OCVPOOF value as VOOS1 and then go to Step 5.

Step 5. Set OCVPOOF [5:0]=111111 and read the OCVPCOUT bit.

Step 6. Decrease the OCVPOOF [5:0] value by 1 and then read the OCVPCOUT bit.
   If the OCVPCOUT bit state has not changed, then repeat Step 6 until the OCVPCOUT bit state has changed.
   If the OCVPCOUT bit state has changed, record the OCVPOOF value as VOOS2 and then go to Step 7.

Step 7. Restore the operational amplifier input offset cancellation value VOOS into the OCVPOOF [5:0] bit field. The offset cancellation procedure is now finished.

Where $VOOS = \dfrac{VOOS1 + VOOS2}{2}$

**Comparator input Offset Cancellation**

Before the offset calibration, the hysteresis voltage should be zero by setting the OCVPCHY bit to 0.

Step 1. Set OCVPSW [7:0]=28H, OCVPCOFM=1, OCVPOOFM=0 and OCVPCRSP=0, the OCVP will now operate in the comparator input offset cancellation mode.

Step 2. Set OCVPDA [7:0]=40H

Step 3. Set OCVPCOF [4:0]=00000 and read the OCVPCOUT bit.

Step 4. Increase the OCVPCOF [4:0] value by 1 and then read the OCVPCOUT bit.

If the OCVPCOUT bit state has not changed, then repeat Step 4 until the OCVPCOUT bit state has changed.

If the OCVPCOUT bit state has changed, record the OCVPCOF value as VCOS1 and then go to Step 5.

Step 5. Set OCVPCOF [4:0]=11111 and read the OCVPCOUT bit.

Step 6. Decrease the OCVPCOF [4:0] value by 1 and then read the OCVPCOUT bit.

If the OCVPCOUT bit state has not changed, then repeat Step 6 until the OCVPCOUT bit state has changed.

If the OCVPCOUT bit state has changed, record the OCVPCOF value as VCOS2 and then go to Step 7.

Step 7. Restore the comparator input offset cancellation value VCOS into the OCVPCOF [4:0] bit field. The offset cancellation procedure is now finished.

Where $VCOS = \dfrac{VCOS1 + VCOS2}{2}$

# Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer Module or an LVD requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. The device contains several external interrupt and internal interrupt functions. The external interrupt is generated by the action of the external INT0 and INT1 pins, while the internal interrupts are generated by various internal functions such as the Timer Modules (TMs), Over Current/Voltage Protection function (OCVP), Time Base, LVD and EEPROM.

## Interrupt Registers

Overall interrupt control, which basically means the setting of request flags when certain microcontroller conditions occur and the setting of interrupt enable bits by the application program, is controlled by a series of registers, located in the Special Purpose Data Memory, as shown in the accompanying table. The interrupt registers fall into three categories. The first is the INTC0~INTC2 registers which setup the primary interrupts, the second is the MFI0~MFI2 registers which setup the Multi-function interrupts. Finally there is an INTEG register to setup the external interrupt trigger edge type.

Each register contains a number of enable bits to enable or disable individual registers as well as interrupt flags to indicate the presence of an interrupt request. The naming convention of these follows a specific pattern. First is listed an abbreviated interrupt type, then the (optional) number of that interrupt followed by either an "E" for enable/disable bit or "F" for request flag.

| Function | Enable Bit | Request Flag | Notes |
|---|---|---|---|
| Global | EMI | — | — |
| OCVP | OCVPE | OCVPF | — |
| INTn Pin | INTnE | INTnF | n=0 or 1 |
| Multi-function | MFnE | MFnF | n=0~2 |
| Time Base | TBnE | TBnF | n=0 or 1 |
| LVD | LVE | LVF | — |
| EEPROM | DEE | DEF | — |
| Timer Module | STMAE | STMAF | — |
|  | STMPE | STMPF | — |
|  | PTMAE | PTMAF | — |
|  | PTMPE | PTMPF | — |

**Interrupt Register Bit Naming Conventions**

| Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
|  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTEG | — | — | — | — | INT1S1 | INT1S0 | INT0S1 | INT0S0 |
| INTC0 | — | — | INT0F | OCVPF | — | INT0E | OCVPE | EMI |
| INTC1 | TB0F | MF2F | MF1F | MF0F | TB0E | MF2E | MF1E | MF0E |
| INTC2 | — | — | INT1F | TB1F | — | — | INT1E | TB1E |
| MFI0 | — | — | STMAF | STMPF | — | — | STMAE | STMPE |
| MFI1 | — | — | PTMAF | PTMPF | — | — | PTMAE | PTMPE |
| MFI2 | — | — | DEF | LVF | — | — | DEE | LVE |

**Interrupt Register List**

### INTEG Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | INT1S1 | INT1S0 | INT0S1 | INT0S0 |
| R/W | — | — | — | — | R/W | R/W | R/W | R/W |
| POR | — | — | — | — | 0 | 0 | 0 | 0 |

Bit 7 ~ 4      Unimplemented, read as "0"

Bit 3 ~ 2      **INT1S1, INT1S0**: Defines INT1 interrupt active edge
         00: Disabled Interrupt
         01: Rising Edge Interrupt
         10: Falling Edge Interrupt
         11: Dual Edge Interrupt

Bit 1 ~ 0      **INT0S1, INT0S0**: Defines INT0 interrupt active edge
         00: Disabled Interrupt
         01: Rising Edge Interrupt
         10: Falling Edge Interrupt
         11: Dual Edge Interrupt

**INTC0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|------|-------|---|-------|-------|------|
| Name | — | — | INT0F | OCVPF | — | INT0E | OCVPE | EMI |
| R/W | — | — | R/W | R/W | — | R/W | R/W | R/W |
| POR | — | — | 0 | 0 | — | 0 | 0 | 0 |

Bit 7~6   Unimplemented, read as "0"

Bit 5   **INT0F**: External interrupt 0 request flag
　　　0: No request
　　　1: Interrupt request

Bit 4   **OCVPF**: Over current/voltage protection interrupt request flag
　　　0: No request
　　　1: Interrupt request

Bit 3   Unimplemented, read as "0"

Bit 2   **INT0E**: External interrupt 0 control
　　　0: Disable
　　　1: Enable

Bit 1   **OCVPE**: Over current/voltage protection interrupt control
　　　0: Disable
　　　1: Enable

Bit 0   **EMI**: Global Interrupt Control
　　　0: Disable
　　　1: Enable

**INTC1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|------|
| Name | TB0F | MF2F | MF1F | MF0F | TB0E | MF2E | MF1E | MF0E |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7   **TB0F**: Time Base 0 request flag
　　　0: No request
　　　1: Interrupt request

Bit 6   **MF2F**: Multi-function interrupt 2 request flag
　　　0: No request
　　　1: Interrupt request

Bit 5   **MF1F**: Multi-function interrupt 1request flag
　　　0: No request
　　　1: Interrupt request

Bit 4   **MF0F**: Multi-function interrupt 0 request flag
　　　0: No request
　　　1: Interrupt request

Bit 3   **TB0E**: Time Base 0 interrupt control
　　　0: Disable
　　　1: Enable

Bit 2   **MF2E**: Multi-function interrupt 2 control
　　　0: Disable
　　　1: Enable

Bit 1   **MF1E**: Multi-function interrupt 1 control
　　　0: Disable
　　　1: Enable

Bit 0   **MF0E**: Multi-function interrupt 0 control
　　　0: Disable
　　　1: Enable

**INTC2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | INT1F | TB1F | — | — | INT1E | TB1E |
| R/W | — | — | R/W | R/W | — | — | R/W | R/W |
| POR | — | — | 0 | 0 | — | — | 0 | 0 |

Bit 7~6      Unimplemented, read as "0"

Bit 5      **INT1F**: External interrupt 1 request flag
         0: No request
         1: Interrupt request

Bit 4      **TB1F**: Time Base 1 interrupt request flag
         0: No request
         1: Interrupt request

Bit 3~2      Unimplemented, read as "0"

Bit 1      **INT1E**: External interrupt 1 control
         0: Disable
         1: Enable

Bit 0      **TB1E**: Time Base 1 interrupt control
         0: Disable
         1: Enable

**MFI0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | STMAF | STMPF | — | — | STMAE | STMPE |
| R/W | — | — | R/W | R/W | — | — | R/W | R/W |
| POR | — | — | 0 | 0 | — | — | 0 | 0 |

Bit 7 ~ 6      Unimplemented, read as "0"

Bit 5      **STMAF**: STM comparator A match interrupt request flag
         0: No request
         1: Interrupt request

Bit 4      **STMPF**: STM comparator P match interrupt request flag
         0: No request
         1: Interrupt request

Bit 3 ~ 2      Unimplemented, read as "0"

Bit 1      **STMAE**: STM comparator A match interrupt control
         0: Disable
         1: Enable

Bit 0      **STMPE**: STM comparator P match interrupt control
         0: Disable
         1: Enable

**MFI1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | PTMAF | PTMPF | — | — | PTMAE | PTMPE |
| R/W | — | — | R/W | R/W | — | — | R/W | R/W |
| POR | — | — | 0 | 0 | — | — | 0 | 0 |

Bit 7 ~ 6    Unimplemented, read as "0"

Bit 5    **PTMAF**: PTM comparator A match interrupt request flag
         0: No request
         1: Interrupt request

Bit 4    **PTMPF**: PTM comparator P match interrupt request flag
         0: No request
         1: Interrupt request

Bit 3 ~ 2    Unimplemented, read as "0"

Bit 1    **PTMAE**: PTM comparator A match interrupt control
         0: Disable
         1: Enable

Bit 0    **PTMPE**: PTM comparator P match interrupt control
         0: Disable
         1: Enable

**MFI2 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | DEF | LVF | — | — | DEE | LVE |
| R/W | — | — | R/W | R/W | — | — | R/W | R/W |
| POR | — | — | 0 | 0 | — | — | 0 | 0 |

Bit 7 ~ 6    Unimplemented, read as "0"

Bit 5    **DEF**: Data EEPROM interrupt request flag
         0: No request
         1: Interrupt request

Bit 4    **LVF**: LVD interrupt request flag
         0: No request
         1: Interrupt request

Bit 3~2    Unimplemented, read as "0"

Bit 1    **DEE**: Data EEPROM interrupt control
         0: Disable
         1: Enable

Bit 0    **LVE**: LVD interrupt control
         0: Disable
         1: Enable

## Interrupt Operation

When the conditions for an interrupt event occur, such as a TM Comparator P or Comparator A match etc, the relevant interrupt request flag will be set. Whether the request flag actually generates a program jump to the relevant interrupt vector is determined by the condition of the interrupt enable bit. If the enable bit is set high then the program will jump to its relevant vector; if the enable bit is zero then although the interrupt request flag is set an actual interrupt will not be generated and the program will not jump to the relevant interrupt vector. The global interrupt enable bit, if cleared to zero, will disable all interrupts.

When an interrupt is generated, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a "JMP" which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a "RETI", which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagrams    with their order of priority. Some interrupt sources have their own individual vector while others share the same multi-function interrupt vector. Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the global interrupt enable bit, EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded.

If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full. In case of simultaneous requests, the accompanying diagram shows the priority that is applied. All of the interrupt request flags when set will wake-up the device if it is in SLEEP or IDLE Mode, however to prevent a wake-up from occurring the corresponding flag should be set before the device is in SLEEP or IDLE Mode.
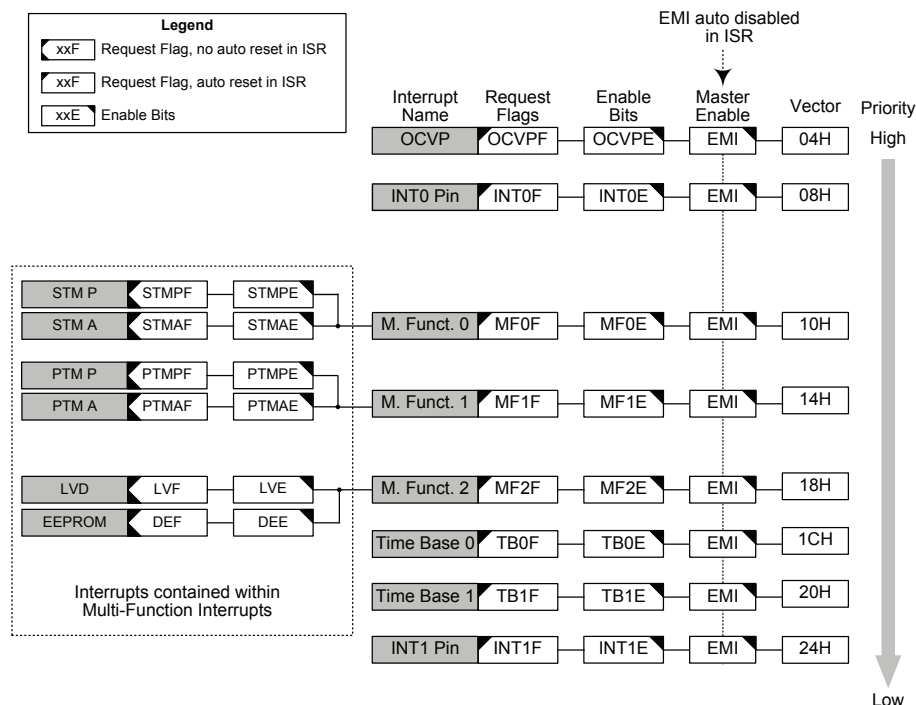
**Interrupt Structure**

## External Interrupts

The external interrupts are controlled by signal transitions on the pins INT0~INT1. An external interrupt request will take place when the external interrupt request flags, INT0F~INT1F, are set, which will occur when a transition, whose type is chosen by the edge select bits, appears on the external interrupt pins. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and respective external interrupt enable bit, INT0E~INT1E, must first be set. Additionally the correct interrupt edge type must be selected using the INTEG register to enable the external interrupt function and to choose the trigger edge type. As the external interrupt pins are pin-shared with I/O pins, they can only be configured as external interrupt pins if their external interrupt enable bit in the corresponding interrupt register has been set. The pin must also be setup as an input by setting the corresponding bit in the port control register as well as the relevant pin-shared function selection bits. When the interrupt is enabled, the stack is not full and the correct transition type appears on the external interrupt pin, a subroutine call to the external interrupt vector, will take place. When the interrupt is serviced, the external interrupt request flags, INT0F~INT1F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor selections on the external interrupt pins will remain valid even if the pin is used as an external interrupt input.

The INTEG register is used to select the type of active edge that will trigger the external interrupt. A choice of either rising or falling or both edge types can be chosen to trigger an external interrupt. Note that the INTEG register can also be used to disable the external interrupt function.

## OCVP Interrupt

An OCVP interrupt request will take place when the OCVP Interrupt request flag, OCVPF, is set, which occurs when the OCVP circuit detects a specific current or voltage condition. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the OCVP Interrupt enable bit, OCVPE, must first be set. When the interrupt is enabled, the stack is not full and a user-defined current or voltage condition occurs, a subroutine call to the OCVP Interrupt vector, will take place. When the OCVP Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts and the OCVP interrupt request flag will be also automatically cleared.

## Multi-function Interrupts

Within the device there are three Multi-function interrupts. Unlike the other independent interrupts, these interrupts have no independent source, but rather are formed from other existing interrupt sources, namely the TM Interrupts, LVD Interrupt and EEPROM Interrupt.

A Multi-function interrupt request will take place when any of the Multi-function interrupt request flags, MFnF are set. The Multi-function interrupt flags will be set when any of their included functions generate an interrupt request flag. To allow the program to branch to its respective interrupt vector address, when the Multi-function interrupt is enabled and the stack is not full, and either one of the interrupts contained within each of Multi-function interrupt occurs, a subroutine call to one of the Multi-function interrupt vectors will take place. When the interrupt is serviced, the related Multi-Function request flag, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

However, it must be noted that, although the Multi-function Interrupt flags will be automatically reset when the interrupt is serviced, the request flags from the original source of the Multi-function interrupts, namely the TM Interrupts, LVD Interrupt  and EEPROM Interrupt will not be automatically reset and must be manually reset by the application program.

## Time Base Interrupts

The function of the Time Base interrupts is to provide regular time signal in the form of an internal interrupt. They are controlled by the overflow signals from their respective timer functions. When these happens their respective interrupt request flags, TB0F or TB1F will be set. To allow the program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI and Time Base enable bits, TB0E or TB1E, must first be set. When the interrupt is enabled, the stack is not full and the Time Base overflows, a subroutine call to their respective vector locations will take place. When the interrupt is serviced, the respective interrupt request flag, TB0F or TB1F, will be automatically reset and the EMI bit will be cleared to disable other interrupts.

The purpose of the Time Base Interrupt is to provide an interrupt signal at fixed time periods. Their clock sources originate from the internal clock source $f_{TB}$. This $f_{TB}$ input clock passes through a divider, the division ratio of which is selected by programming the appropriate bits in the TBC register to obtain longer interrupt periods whose value ranges. The clock source that generates $f_{TB}$, which in turn controls the Time Base interrupt period, can originate from several different sources which is selected using the TBCK bit in the TBC register.

**TBC Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TBON | TBCK | TB11 | TB10 | — | TB02 | TB01 | TB00 |
| R/W | R/W | R/W | R/W | R/W | — | R/W | R/W | R/W |
| POR | 0 | 0 | 1 | 1 | — | 1 | 1 | 1 |

Bit 7      **TBON**: TB0 and TB1 Control bit
         0: Disable
         1: Enable

Bit 6      **TBCK**: Select $f_{TB}$ Clock Source
         0: $f_{TBC}$
         1: $f_{SYS}/4$

Bit 5 ~ 4      **TB11 ~ TB10**: Select Time Base 1 Time-out Period
         00: $2^{12}/f_{TB}$
         01: $2^{13}/f_{TB}$
         10: $2^{14}/f_{TB}$
         11: $2^{15}/f_{TB}$

Bit 3      Unimplemented, read as "0"

Bit 2 ~ 0      **TB02 ~ TB00**: Select Time Base 0 Time-out Period
         000: $2^{8}/f_{TB}$
         001: $2^{9}/f_{TB}$
         010: $2^{10}/f_{TB}$
         011: $2^{11}/f_{TB}$
         100: $2^{12}/f_{TB}$
         101: $2^{13}/f_{TB}$
         110: $2^{14}/f_{TB}$
         111: $2^{15}/f_{TB}$



**Time Base Interrupt**
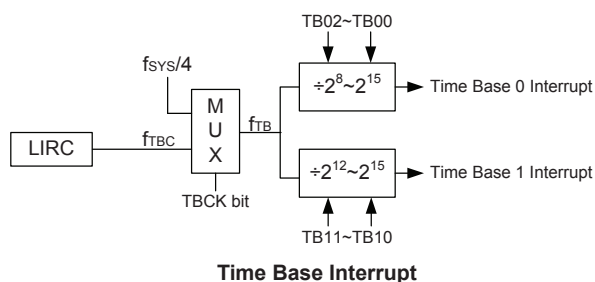
### EEPROM Interrupt

The EEPROM interrupt is contained within the Multi-function Interrupt. An EEPROM Interrupt request will take place when the EEPROM Interrupt request flag, DEF, is set, which occurs when an EEPROM Write cycle ends. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and EEPROM Interrupt enable bit, DEE, and associated Multi-function interrupt enable bit, MF2E, must first be set. When the interrupt is enabled, the stack is not full and an EEPROM Write cycle ends, a subroutine call to the respective EEPROM Interrupt vector, will take place. When the EEPROM Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the DEF flag will not be automatically cleared, it has to be cleared by the application program.

### LVD Interrupt

The LVD interrupt is contained within the Multi-function Interrupt. An LVD Interrupt request will take place when the LVD Interrupt request flag, LVF, is set, which occurs when the Low Voltage Detector function detects a low power supply voltage. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and Low Voltage Interrupt enable bit, LVE, and associated Multi-function interrupt enable bit, MF2E, must first be set. When the interrupt is enabled, the stack is not full and a low voltage condition occurs, a subroutine call to the LVD Interrupt vector, will take place. When the Low Voltage Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the LVD interrupt request flag, LVF, will not be automatically cleared, it has to be cleared by the application program.

### TM Interrupts

The Standard and Periodic Type TMs each have two interrupts. All of the TM interrupts are contained within the Multi-function Interrupts. For the different Type TMs there are two interrupt request flags xTMPF and xTMAF and two enable bits xTMPE and xTMAE. A TM interrupt request will take place when any of the TM request flags are set, a situation which occurs when a TM comparator P or comparator A match situation happens.

To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the respective TM Interrupt enable bit, and associated Multi-function interrupt enable bit, MFnF, must first be set. When the interrupt is enabled, the stack is not full and a TM comparator match situation occurs, a subroutine call to the relevant TM Interrupt vector locations, will take place. When the TM interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the related MFnF flag will be automatically cleared. As the TM interrupt request flags will not be automatically cleared, they have to be cleared by the application program.

### Interrupt Wake-up Function

Each of the interrupt functions has the capability of waking up the microcontroller when in the SLEEP or IDLE Mode. A wake-up is generated when an interrupt request flag changes from low to high and is independent of whether the interrupt is enabled or not. Therefore, even though the device is in the SLEEP or IDLE Mode and its system oscillator stopped, situations such as external edge transitions on the external interrupt pins or a low power supply voltage may cause their respective interrupt flag to be set high and consequently generate an interrupt. Care must therefore be taken if spurious wake-up situations are to be avoided. If an interrupt wake-up function is to be disabled then the corresponding interrupt request flag should be set high before the device enters the SLEEP or IDLE Mode. The interrupt enable bits have no effect on the interrupt wake-up function.

### Programming Considerations

By disabling the relevant interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt register until the corresponding interrupt is serviced or until the request flag is cleared by the application program.

Where a certain interrupt is contained within a Multi-function interrupt, then when the interrupt service routine is executed, as only the Multi-function interrupt request flags, MF0F~MF2F, will be automatically cleared, the individual request flag for the function needs to be cleared by the application program.

It is recommended that programs do not use the "CALL" instruction within the interrupt service subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a CALL subroutine is executed in the interrupt subroutine.

Every interrupt has the capability of waking up the microcontroller when it is in SLEEP or IDLE Mode, the wake up being generated when the interrupt request flag changes from low to high. If it is required to prevent a certain interrupt from waking up the microcontroller then its respective request flag should be first set high before enter SLEEP or IDLE Mode.

As only the Program Counter is pushed onto the stack, then when the interrupt is serviced, if the contents of the accumulator, status register or other registers are altered by the interrupt service program, their contents should be saved to the memory at the beginning of the interrupt service routine.

To return from an interrupt subroutine, either a RET or RETI instruction may be executed. The RETI instruction in addition to executing a return to the main program also automatically sets the EMI bit high to allow further interrupts. The RET instruction however only executes a return to the main program leaving the EMI bit in its present zero state and therefore disabling the execution of further interrupts.

# Low Voltage Detector – LVD

The device has a Low Voltage Detector function, also known as LVD. This enables the device to monitor the power supply voltage, $V_{DD}$, and provides a warning signal should it fall below a certain level. This function may be especially useful in battery applications where the supply voltage will gradually reduce as the battery ages, as it allows an early warning battery low signal to be generated. The Low Voltage Detector also has the capability of generating an interrupt signal.

## LVD Register

The Low Voltage Detector function is controlled using a single register with the name LVDC. Three bits in this register, VLVD2~VLVD0, are used to select one of eight fixed voltages below which a low voltage condition will be determined. A low voltage condition is indicated when the LVDO bit is set. If the LVDO bit is low, this indicates that the $V_{DD}$ voltage is above the preset low voltage value. The LVDEN bit is used to control the overall on/off function of the low voltage detector. Setting the bit high will enable the low voltage detector. Clearing the bit to zero will switch off the internal low voltage detector circuits. As the low voltage detector will consume a certain amount of power, it may be desirable to switch off the circuit when not in use, an important consideration in power sensitive battery powered applications.

### LVDC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
| Name | — | — | LVDO | LVDEN | — | VLVD2 | VLVD1 | VLVD0 |
| R/W | — | — | R | R/W | — | R/W | R/W | R/W |
| POR | — | — | 0 | 0 | — | 0 | 0 | 0 |

Bit 7 ~ 6    Unimplemented, read as "0"

Bit 5    **LVDO**: LVD Output Flag
　　　　0: No Low Voltage Detected
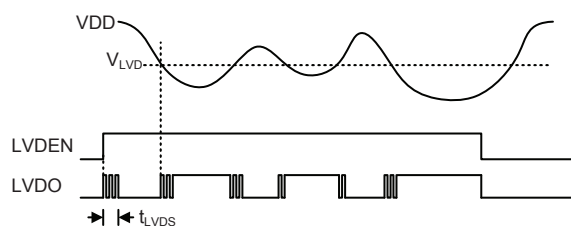　　　　1: Low Voltage Detected

Bit 4    **LVDEN**: Low Voltage Detector Control
　　　　0: Disable
　　　　1: Enable

Bit 3    Unimplemented, read as "0"

Bit 2~0    **VLVD2 ~ VLVD0**: Select LVD Voltage
　　　　000: 2.0V
　　　　001: 2.2V
　　　　010: 2.4V
　　　　011: 2.7V
　　　　100: 3.0V
　　　　101: 3.3V
　　　　110: 3.6V
　　　　111: 4.0V

### LVD Operation

The Low Voltage Detector function operates by comparing the power supply voltage, $V_{DD}$, with a pre-specified voltage level stored in the LVDC register. This has a range of between 2.0V and 4.0V. When the power supply voltage, $V_{DD}$, falls below this pre-determined value, the LVDO bit will be set high indicating a low power supply voltage condition. The Low Voltage Detector function is supplied by a reference voltage which will be automatically enabled. After enabling the Low Voltage Detector, a time delay $t_{LVDS}$ should be allowed for the circuitry to stabilise before reading the LVDO bit. Note also that as the $V_{DD}$ voltage may rise and fall rather slowly, at the voltage nears that of $V_{LVD}$, there may be multiple bit LVDO transitions.
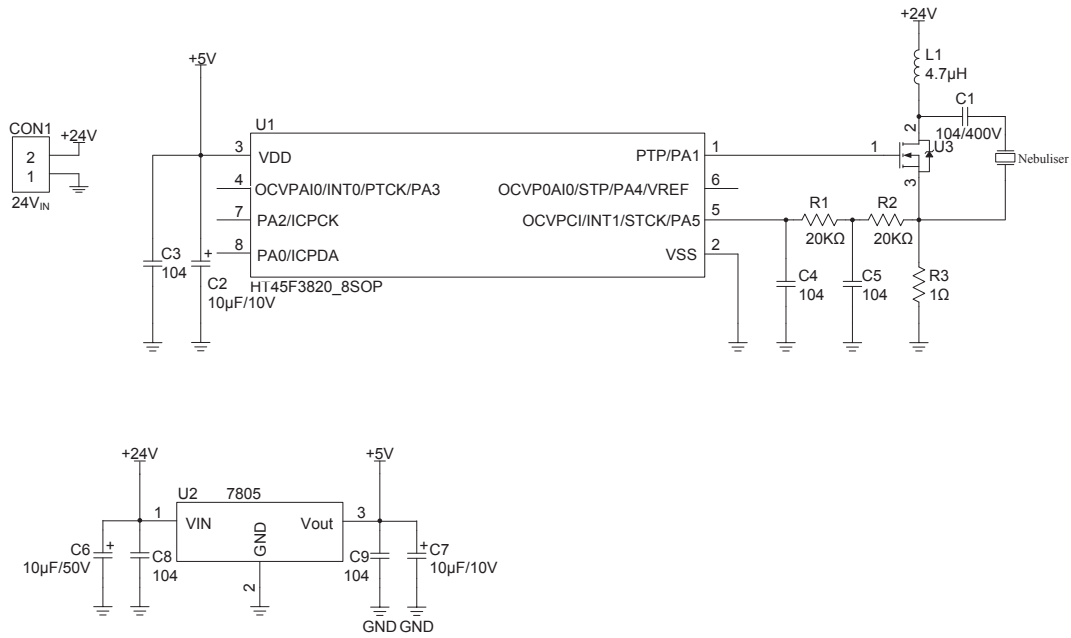


**LVD Operation**

The Low Voltage Detector also has its own interrupt which is contained within one of the multi-function interrupts, providing an alternative means of low voltage detection, in addition to polling the LVDO bit. The interrupt will only be generated after a delay of $t_{LVD}$ after the LVDO bit has been set high by a low voltage condition. In this case, the LVF interrupt request flag will be set, causing an interrupt to be generated if $V_{DD}$ falls below the preset LVD voltage. This will cause the device to wake-up from the SLEEP or IDLE Mode, however if the Low Voltage Detector wake up function is not required then the LVF flag should be first set high before the device enters the SLEEP or IDLE Mode.

## Configuration Options

Configuration options refer to certain options within the MCU that are programmed into the device during the programming process. During the development process, these options are selected using the HT-IDE software development tools. As these options are programmed into the device using the hardware programming tools, once they are selected they cannot be changed later using the application program. All options must be defined for proper system function, the details of which are shown in the table.

| No. | Options |
|---|---|
| **Watchdog Timer Option** | |
| 1 | Watchdog Timer Enable/disable Selection:<br>Controlled by WDTC register<br>Always enabled |

## Application Circuits

## Instruction Set

### Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontroller, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

### Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be "CLR PCL" or "MOV PCL, A". For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

### Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

### Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

## Logical and Rotate Operation

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application which rotate data operations are used is to implement multiplication and division calculations.

## Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction "RET" in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

## Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

## Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be set as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

## Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

## Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

### Table Conventions

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

| Mnemonic | Description | Cycles | Flag Affected |
|---|---|---|---|
| **Arithmetic** | | | |
| ADD A,[m] | Add Data Memory to ACC | 1 | Z, C, AC, OV |
| ADDM A,[m] | Add ACC to Data Memory | 1[Note] | Z, C, AC, OV |
| ADD A,x | Add immediate data to ACC | 1 | Z, C, AC, OV |
| ADC A,[m] | Add Data Memory to ACC with Carry | 1 | Z, C, AC, OV |
| ADCM A,[m] | Add ACC to Data memory with Carry | 1[Note] | Z, C, AC, OV |
| SUB A,x | Subtract immediate data from the ACC | 1 | Z, C, AC, OV |
| SUB A,[m] | Subtract Data Memory from ACC | 1 | Z, C, AC, OV |
| SUBM A,[m] | Subtract Data Memory from ACC with result in Data Memory | 1[Note] | Z, C, AC, OV |
| SBC A,[m] | Subtract Data Memory from ACC with Carry | 1 | Z, C, AC, OV |
| SBCM A,[m] | Subtract Data Memory from ACC with Carry, result in Data Memory | 1[Note] | Z, C, AC, OV |
| DAA [m] | Decimal adjust ACC for Addition with result in Data Memory | 1[Note] | C |
| **Logic Operation** | | | |
| AND A,[m] | Logical AND Data Memory to ACC | 1 | Z |
| OR A,[m] | Logical OR Data Memory to ACC | 1 | Z |
| XOR A,[m] | Logical XOR Data Memory to ACC | 1 | Z |
| ANDM A,[m] | Logical AND ACC to Data Memory | 1[Note] | Z |
| ORM A,[m] | Logical OR ACC to Data Memory | 1[Note] | Z |
| XORM A,[m] | Logical XOR ACC to Data Memory | 1[Note] | Z |
| AND A,x | Logical AND immediate Data to ACC | 1 | Z |
| OR A,x | Logical OR immediate Data to ACC | 1 | Z |
| XOR A,x | Logical XOR immediate Data to ACC | 1 | Z |
| CPL [m] | Complement Data Memory | 1[Note] | Z |
| CPLA [m] | Complement Data Memory with result in ACC | 1 | Z |
| **Increment & Decrement** | | | |
| INCA [m] | Increment Data Memory with result in ACC | 1 | Z |
| INC [m] | Increment Data Memory | 1[Note] | Z |
| DECA [m] | Decrement Data Memory with result in ACC | 1 | Z |
| DEC [m] | Decrement Data Memory | 1[Note] | Z |
| **Rotate** | | | |
| RRA [m] | Rotate Data Memory right with result in ACC | 1 | None |
| RR [m] | Rotate Data Memory right | 1[Note] | None |
| RRCA [m] | Rotate Data Memory right through Carry with result in ACC | 1 | C |
| RRC [m] | Rotate Data Memory right through Carry | 1[Note] | C |
| RLA [m] | Rotate Data Memory left with result in ACC | 1 | None |
| RL [m] | Rotate Data Memory left | 1[Note] | None |
| RLCA [m] | Rotate Data Memory left through Carry with result in ACC | 1 | C |
| RLC [m] | Rotate Data Memory left through Carry | 1[Note] | C |

| Mnemonic | Description | Cycles | Flag Affected |
|----------|-------------|--------|---------------|
| **Data Move** | | | |
| MOV A,[m] | Move Data Memory to ACC | 1 | None |
| MOV [m],A | Move ACC to Data Memory | 1[Note] | None |
| MOV A,x | Move immediate data to ACC | 1 | None |
| **Bit Operation** | | | |
| CLR [m].i | Clear bit of Data Memory | 1[Note] | None |
| SET [m].i | Set bit of Data Memory | 1[Note] | None |
| **Branch Operation** | | | |
| JMP addr | Jump unconditionally | 2 | None |
| SZ [m] | Skip if Data Memory is zero | 1[Note] | None |
| SZA [m] | Skip if Data Memory is zero with data movement to ACC | 1[Note] | None |
| SZ [m].i | Skip if bit i of Data Memory is zero | 1[Note] | None |
| SNZ [m].i | Skip if bit i of Data Memory is not zero | 1[Note] | None |
| SIZ [m] | Skip if increment Data Memory is zero | 1[Note] | None |
| SDZ [m] | Skip if decrement Data Memory is zero | 1[Note] | None |
| SIZA [m] | Skip if increment Data Memory is zero with result in ACC | 1[Note] | None |
| SDZA [m] | Skip if decrement Data Memory is zero with result in ACC | 1[Note] | None |
| CALL addr | Subroutine call | 2 | None |
| RET | Return from subroutine | 2 | None |
| RET A,x | Return from subroutine and load immediate data to ACC | 2 | None |
| RETI | Return from interrupt | 2 | None |
| **Table Read Operation** | | | |
| TABRD [m] | Read table (specific page) to TBLH and Data Memory | 2[Note] | None |
| TABRDC [m] | Read table (current page) to TBLH and Data Memory | 2[Note] | None |
| TABRDL [m] | Read table (last page) to TBLH and Data Memory | 2[Note] | None |
| **Miscellaneous** | | | |
| NOP | No operation | 1 | None |
| CLR [m] | Clear Data Memory | 1[Note] | None |
| SET [m] | Set Data Memory | 1[Note] | None |
| CLR WDT | Clear Watchdog Timer | 1 | TO, PDF |
| CLR WDT1 | Pre-clear Watchdog Timer | 1 | TO, PDF |
| CLR WDT2 | Pre-clear Watchdog Timer | 1 | TO, PDF |
| SWAP [m] | Swap nibbles of Data Memory | 1[Note] | None |
| SWAPA [m] | Swap nibbles of Data Memory with result in ACC | 1 | None |
| HALT | Enter power down mode | 1 | TO, PDF |

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.

2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.

3. For the "CLR WDT1" and "CLR WDT2" instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both "CLR WDT1" and "CLR WDT2" instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

## Instruction Definition

| **ADC A,[m]** | Add Data Memory to ACC with Carry |
|---|---|
| Description | The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator. |
| Operation | ACC ← ACC + [m] + C |
| Affected flag(s) | OV, Z, AC, C |

| **ADCM A,[m]** | Add ACC to Data Memory with Carry |
|---|---|
| Description | The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory. |
| Operation | [m] ← ACC + [m] + C |
| Affected flag(s) | OV, Z, AC, C |

| **ADD A,[m]** | Add Data Memory to ACC |
|---|---|
| Description | The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator. |
| Operation | ACC ← ACC + [m] |
| Affected flag(s) | OV, Z, AC, C |

| **ADD A,x** | Add immediate data to ACC |
|---|---|
| Description | The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator. |
| Operation | ACC ← ACC + x |
| Affected flag(s) | OV, Z, AC, C |

| **ADDM A,[m]** | Add ACC to Data Memory |
|---|---|
| Description | The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory. |
| Operation | [m] ← ACC + [m] |
| Affected flag(s) | OV, Z, AC, C |

| **AND A,[m]** | Logical AND Data Memory to ACC |
|---|---|
| Description | Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC ″AND″ [m] |
| Affected flag(s) | Z |

| **AND A,x** | Logical AND immediate data to ACC |
|---|---|
| Description | Data in the Accumulator and the specified immediate data perform a bit wise logical AND operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC ″AND″ x |
| Affected flag(s) | Z |

| **ANDM A,[m]** | Logical AND ACC to Data Memory |
|---|---|
| Description | Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory. |
| Operation | [m] ← ACC ″AND″ [m] |
| Affected flag(s) | Z |

| **CALL addr** | Subroutine call |
|---|---|
| Description | Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction. |
| Operation | Stack ← Program Counter + 1 <br> Program Counter ← addr |
| Affected flag(s) | None |

| **CLR [m]** | Clear Data Memory |
|---|---|
| Description | Each bit of the specified Data Memory is cleared to 0. |
| Operation | [m] ← 00H |
| Affected flag(s) | None |

| **CLR [m].i** | Clear bit of Data Memory |
|---|---|
| Description | Bit i of the specified Data Memory is cleared to 0. |
| Operation | [m].i ← 0 |
| Affected flag(s) | None |

| **CLR WDT** | Clear Watchdog Timer |
|---|---|
| Description | The TO, PDF flags and the WDT are all cleared. |
| Operation | WDT cleared <br> TO ← 0 <br> PDF ← 0 |
| Affected flag(s) | TO, PDF |

| **CLR WDT1** | Pre-clear Watchdog Timer |
|---|---|
| Description | The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repetitively executing this instruction without alternately executing CLR WDT2 will have no effect. |
| Operation | WDT cleared <br> TO ← 0 <br> PDF ← 0 |
| Affected flag(s) | TO, PDF |

| **CLR WDT2** | Pre-clear Watchdog Timer |
|---|---|
| Description | The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repetitively executing this instruction without alternately executing CLR WDT1 will have no effect. |
| Operation | WDT cleared <br> TO ← 0 <br> PDF ← 0 |
| Affected flag(s) | TO, PDF |

| **CPL [m]** | Complement Data Memory |
|---|---|
| Description | Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. |
| Operation | [m] ← $\overline{[m]}$ |
| Affected flag(s) | Z |

| **CPLA [m]** | Complement Data Memory with result in ACC |
|---|---|
| Description | Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC \leftarrow \overline{[m]}$ |
| Affected flag(s) | Z |

| **DAA [m]** | Decimal-Adjust ACC for addition with result in Data Memory |
|---|---|
| Description | Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition. |
| Operation | $[m] \leftarrow ACC + 00H$ or<br>$[m] \leftarrow ACC + 06H$ or<br>$[m] \leftarrow ACC + 60H$ or<br>$[m] \leftarrow ACC + 66H$ |
| Affected flag(s) | C |

| **DEC [m]** | Decrement Data Memory |
|---|---|
| Description | Data in the specified Data Memory is decremented by 1. |
| Operation | $[m] \leftarrow [m] - 1$ |
| Affected flag(s) | Z |

| **DECA [m]** | Decrement Data Memory with result in ACC |
|---|---|
| Description | Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged. |
| Operation | $ACC \leftarrow [m] - 1$ |
| Affected flag(s) | Z |

| **HALT** | Enter power down mode |
|---|---|
| Description | This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared. |
| Operation | $TO \leftarrow 0$<br>$PDF \leftarrow 1$ |
| Affected flag(s) | TO, PDF |

| **INC [m]** | Increment Data Memory |
|---|---|
| Description | Data in the specified Data Memory is incremented by 1. |
| Operation | $[m] \leftarrow [m] + 1$ |
| Affected flag(s) | Z |

| **INCA [m]** | Increment Data Memory with result in ACC |
|---|---|
| Description | Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged. |
| Operation | $ACC \leftarrow [m] + 1$ |
| Affected flag(s) | Z |

**JMP addr**

| | |
|---|---|
| | Jump unconditionally |
| Description | The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction. |
| Operation | Program Counter ← addr |
| Affected flag(s) | None |

**MOV A,[m]**

| | |
|---|---|
| | Move Data Memory to ACC |
| Description | The contents of the specified Data Memory are copied to the Accumulator. |
| Operation | ACC ← [m] |
| Affected flag(s) | None |

**MOV A,x**

| | |
|---|---|
| | Move immediate data to ACC |
| Description | The immediate data specified is loaded into the Accumulator. |
| Operation | ACC ← x |
| Affected flag(s) | None |

**MOV [m],A**

| | |
|---|---|
| | Move ACC to Data Memory |
| Description | The contents of the Accumulator are copied to the specified Data Memory. |
| Operation | [m] ← ACC |
| Affected flag(s) | None |

**NOP**

| | |
|---|---|
| | No operation |
| Description | No operation is performed. Execution continues with the next instruction. |
| Operation | No operation |
| Affected flag(s) | None |

**OR A,[m]**

| | |
|---|---|
| | Logical OR Data Memory to ACC |
| Description | Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC ″OR″ [m] |
| Affected flag(s) | Z |

**OR A,x**

| | |
|---|---|
| | Logical OR immediate data to ACC |
| Description | Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC ″OR″ x |
| Affected flag(s) | Z |

**ORM A,[m]**

| | |
|---|---|
| | Logical OR ACC to Data Memory |
| Description | Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory. |
| Operation | [m] ← ACC ″OR″ [m] |
| Affected flag(s) | Z |

**RET**

| | |
|---|---|
| | Return from subroutine |
| Description | The Program Counter is restored from the stack. Program execution continues at the restored address. |
| Operation | Program Counter ← Stack |
| Affected flag(s) | None |

| **RET A,x** | Return from subroutine and load immediate data to ACC |
|---|---|
| Description | The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address. |
| Operation | Program Counter ← Stack <br> ACC ← x |
| Affected flag(s) | None |

| **RETI** | Return from interrupt |
|---|---|
| Description | The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program. |
| Operation | Program Counter ← Stack <br> EMI ← 1 |
| Affected flag(s) | None |

| **RL [m]** | Rotate Data Memory left |
|---|---|
| Description | The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. |
| Operation | [m].(i+1) ← [m].i; (i=0~6) <br> [m].0 ← [m].7 |
| Affected flag(s) | None |

| **RLA [m]** | Rotate Data Memory left with result in ACC |
|---|---|
| Description | The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | ACC.(i+1) ← [m].i; (i=0~6) <br> ACC.0 ← [m].7 |
| Affected flag(s) | None |

| **RLC [m]** | Rotate Data Memory left through Carry |
|---|---|
| Description | The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0. |
| Operation | [m].(i+1) ← [m].i; (i=0~6) <br> [m].0 ← C <br> C ← [m].7 |
| Affected flag(s) | C |

| **RLCA [m]** | Rotate Data Memory left through Carry with result in ACC |
|---|---|
| Description | Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | ACC.(i+1) ← [m].i; (i=0~6) <br> ACC.0 ← C <br> C ← [m].7 |
| Affected flag(s) | C |

| **RR [m]** | Rotate Data Memory right |
|---|---|
| Description | The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7. |
| Operation | [m].i ← [m].(i+1); (i=0~6) <br> [m].7 ← [m].0 |
| Affected flag(s) | None |

| **RRA [m]** | Rotate Data Memory right with result in ACC |
|---|---|
| Description | Data in the specified Data Memory is rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC.i \leftarrow [m].(i+1); (i=0\sim6)$<br>$ACC.7 \leftarrow [m].0$ |
| Affected flag(s) | None |

| **RRC [m]** | Rotate Data Memory right through Carry |
|---|---|
| Description | The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. |
| Operation | $[m].i \leftarrow [m].(i+1); (i=0\sim6)$<br>$[m].7 \leftarrow C$<br>$C \leftarrow [m].0$ |
| Affected flag(s) | C |

| **RRCA [m]** | Rotate Data Memory right through Carry with result in ACC |
|---|---|
| Description | Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC.i \leftarrow [m].(i+1); (i=0\sim6)$<br>$ACC.7 \leftarrow C$<br>$C \leftarrow [m].0$ |
| Affected flag(s) | C |

| **SBC A,[m]** | Subtract Data Memory from ACC with Carry |
|---|---|
| Description | The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $ACC \leftarrow ACC - [m] - C$ |
| Affected flag(s) | OV, Z, AC, C |

| **SBCM A,[m]** | Subtract Data Memory from ACC with Carry and result in Data Memory |
|---|---|
| Description | The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $[m] \leftarrow ACC - [m] - C$ |
| Affected flag(s) | OV, Z, AC, C |

| **SDZ [m]** | Skip if decrement Data Memory is 0 |
|---|---|
| Description | The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | $[m] \leftarrow [m] - 1$<br>Skip if [m]=0 |
| Affected flag(s) | None |

| **SDZA [m]** | Skip if decrement Data Memory is zero with result in ACC |
|---|---|
| Description | The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction. |
| Operation | ACC ← [m] − 1<br>Skip if ACC=0 |
| Affected flag(s) | None |

| **SET [m]** | Set Data Memory |
|---|---|
| Description | Each bit of the specified Data Memory is set to 1. |
| Operation | [m] ← FFH |
| Affected flag(s) | None |

| **SET [m].i** | Set bit of Data Memory |
|---|---|
| Description | Bit i of the specified Data Memory is set to 1. |
| Operation | [m].i ← 1 |
| Affected flag(s) | None |

| **SIZ [m]** | Skip if increment Data Memory is 0 |
|---|---|
| Description | The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | [m] ← [m] + 1<br>Skip if [m]=0 |
| Affected flag(s) | None |

| **SIZA [m]** | Skip if increment Data Memory is zero with result in ACC |
|---|---|
| Description | The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | ACC ← [m] + 1<br>Skip if ACC=0 |
| Affected flag(s) | None |

| **SNZ [m].i** | Skip if bit i of Data Memory is not 0 |
|---|---|
| Description | If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction. |
| Operation | Skip if [m].i ≠ 0 |
| Affected flag(s) | None |

| **SUB A,[m]** | Subtract Data Memory from ACC |
|---|---|
| Description | The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | ACC ← ACC − [m] |
| Affected flag(s) | OV, Z, AC, C |

| **SUBM A,[m]** | Subtract Data Memory from ACC with result in Data Memory |
|---|---|
| Description | The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $[m] \leftarrow ACC - [m]$ |
| Affected flag(s) | OV, Z, AC, C |

| **SUB A,x** | Subtract immediate data from ACC |
|---|---|
| Description | The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $ACC \leftarrow ACC - x$ |
| Affected flag(s) | OV, Z, AC, C |

| **SWAP [m]** | Swap nibbles of Data Memory |
|---|---|
| Description | The low-order and high-order nibbles of the specified Data Memory are interchanged. |
| Operation | $[m].3\sim[m].0 \leftrightarrow [m].7\sim[m].4$ |
| Affected flag(s) | None |

| **SWAPA [m]** | Swap nibbles of Data Memory with result in ACC |
|---|---|
| Description | The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged. |
| Operation | $ACC.3\sim ACC.0 \leftarrow [m].7\sim[m].4$ <br> $ACC.7\sim ACC.4 \leftarrow [m].3\sim[m].0$ |
| Affected flag(s) | None |

| **SZ [m]** | Skip if Data Memory is 0 |
|---|---|
| Description | If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | Skip if [m]=0 |
| Affected flag(s) | None |

| **SZA [m]** | Skip if Data Memory is 0 with data movement to ACC |
|---|---|
| Description | The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | $ACC \leftarrow [m]$ <br> Skip if [m]=0 |
| Affected flag(s) | None |

| **SZ [m].i** | Skip if bit i of Data Memory is 0 |
|---|---|
| Description | If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction. |
| Operation | Skip if [m].i=0 |
| Affected flag(s) | None |

| **TABRD [m]** | Read table (specific page) to TBLH and Data Memory |
|---|---|
| Description | The low byte of the program code (specific page) addressed by the table pointer pair (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH. |
| Operation | [m] ← program code (low byte)<br>TBLH ← program code (high byte) |
| Affected flag(s) | None |

| **TABRDC [m]** | Read table (current page) to TBLH and Data Memory |
|---|---|
| Description | The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH. |
| Operation | [m] ← program code (low byte)<br>TBLH ← program code (high byte) |
| Affected flag(s) | None |

| **TABRDL [m]** | Read table (last page) to TBLH and Data Memory |
|---|---|
| Description | The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH. |
| Operation | [m] ← program code (low byte)<br>TBLH ← program code (high byte) |
| Affected flag(s) | None |

| **XOR A,[m]** | Logical XOR Data Memory to ACC |
|---|---|
| Description | Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC ″XOR″ [m] |
| Affected flag(s) | Z |

| **XORM A,[m]** | Logical XOR ACC to Data Memory |
|---|---|
| Description | Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory. |
| Operation | [m] ← ACC ″XOR″ [m] |
| Affected flag(s) | Z |

| **XOR A,x** | Logical XOR immediate data to ACC |
|---|---|
| Description | Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC ″XOR″ x |
| Affected flag(s) | Z |

# Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)

- The Operation Instruction of Packing Materials

- Carton information

### 8-pin SOP (150mil) Outline Dimensions
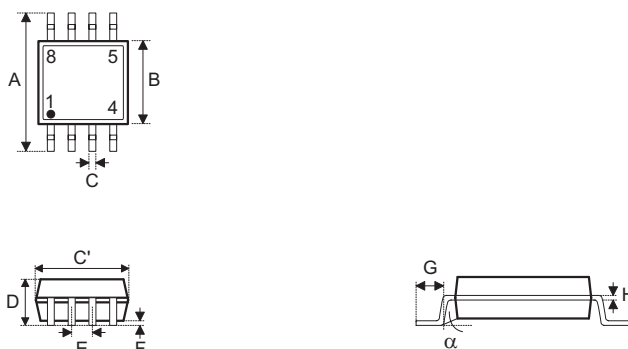
| Symbol | Dimensions in inch | | |
|--------|------|------|------|
| | **Min.** | **Nom.** | **Max.** |
| A | — | 0.236 BSC | — |
| B | — | 0.154 BSC | — |
| C | 0.012 | — | 0.020 |
| C' | — | 0.193 BSC | — |
| D | — | — | 0.069 |
| E | — | 0.050 BSC | — |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|--------|------|------|------|
| | **Min.** | **Nom.** | **Max.** |
| A | — | 6.00 BSC | — |
| B | — | 3.90 BSC | — |
| C | 0.31 | — | 0.51 |
| C' | — | 4.90 BSC | — |
| D | — | — | 1.75 |
| E | — | 1.27 BSC | — |
| F | 0.10 | — | 0.25 |
| G | 0.40 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |

### 10-pin SOP (150mil) Outline Dimensions
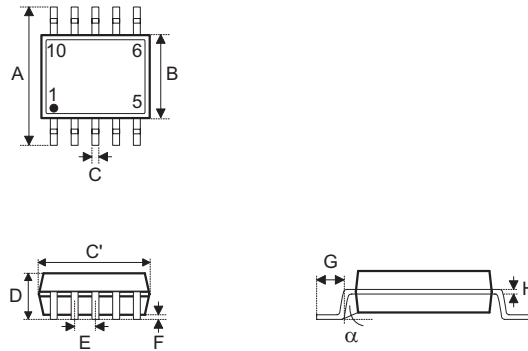


| Symbol | Dimensions in inch | | |
|--------|------|------|------|
| | **Min.** | **Nom.** | **Max.** |
| A | — | 0.236 BSC | — |
| B | — | 0.154 BSC | — |
| C | 0.012 | — | 0.018 |
| C' | — | 0.193 BSC | — |
| D | — | — | 0.069 |
| E | — | 0.039 BSC | — |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|--------|------|------|------|
| | **Min.** | **Nom.** | **Max.** |
| A | — | 6.00 BSC | — |
| B | — | 3.90 BSC | — |
| C | 0.30 | — | 0.45 |
| C' | — | 4.90 BSC | — |
| D | — | — | 1.75 |
| E | — | 1.00 BSC | — |
| F | 0.10 | — | 0.25 |
| G | 0.40 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |