Preliminary

GaN Hybrid Power Amplifier HT1818-15M

Product Features

- E-pHEMT GaAs + GaN on SiC
- 2-Stage Amplifier 50ohms Matching
- Surface Mount Hybrid Type
- Small Size & Mass
- High Efficiency

Applications

- RF Sub-Systems
- Base Station
- Repeater
- 4G/LTE system
- Small cell

Package Type : NP-1EL

Description

The HT1818-15M is designed for LTE Repeater & RF Sub-systems application frequencies from 1805 to 1880MHz
This amplifier uses GaN HEMT technology which performs high breakdown voltage, high efficiency. High In/Output impedance, High power density.

Electrical Specifications @ Vds1 =5V, Vds2 =28V, Ta=25℃

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	1805	-	1880	ZS = ZL = 50 ohm
Power Gain	dB	-	34	-	Amp1 : Idq1 = 140mA Amp2 : Idq2 = 105mA
Gain Flatness		-	0.8	1.5	
Input Return Loss		-	-9	-6	
Pout @ Average	dBm	-	33	-	
Pout @ Psat	dBm	40.5	41.5	-	Pulse Width=20us, Duty10%
ACLR @ BW 10MHz LTE (PAPR 7.5dB)	dBc	-	-39	-30	Non DPD
		-	-54	-	With DPD
Drain Efficiency	%	-	27	-	Pout @ Average
Ids1	mA	-	140	-	
Ids2		-	240	-	
Supply Voltage	V	-	5	-	Drive Amp. (Vds1)
		-	-3.0	-2.0	Gate Bias (Vgs2)
		-	28	-	Main Bias (Vds2)

Caution

The drain voltage must be supplied to the device after the gate voltage is supplied
Turn on : Turn on the Gate Voltage supply and last turn on the Drain voltage supplies
Turn off : Turn off the Drain Voltage and last turn off the Gate voltage

Note

1. ACLR Measured Pout=33dBm @ fc± 10MHz / 9.015MHz
   LTE 10MHz 1FA PAPR=7.5dB @ 0.01% probability on CCDF, (DPD Engine: Optichron OP6180)
2. HT Series have internal DC blocking capacitors at the RF input and output ports

Mechanical Specifications

PARAMETER	UNIT	TYP	REMARK
Mass	g	2	-
Dimension	㎜	20.5 x 15 x 3.5	-

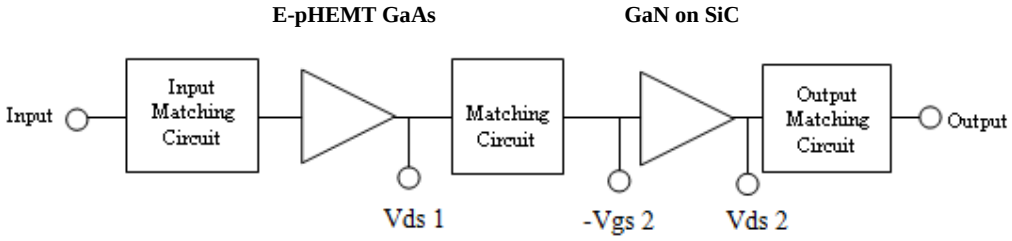
Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL
Gate-Source Voltage	V	-10 ~ 0	Vgs2
Drain-Source Voltage	V	7	Vds1
		50	Vds2
Gate Current	mA	4.0	Igs2
Operating Junction Temperature	°C	225	T_J
Operating Case Temperature	°C	-30 ~ 95	T_C
Storage Temperature	°C	-40 ~ 100	T_{STG}
Maximum Input Level	dBm	20	Pin

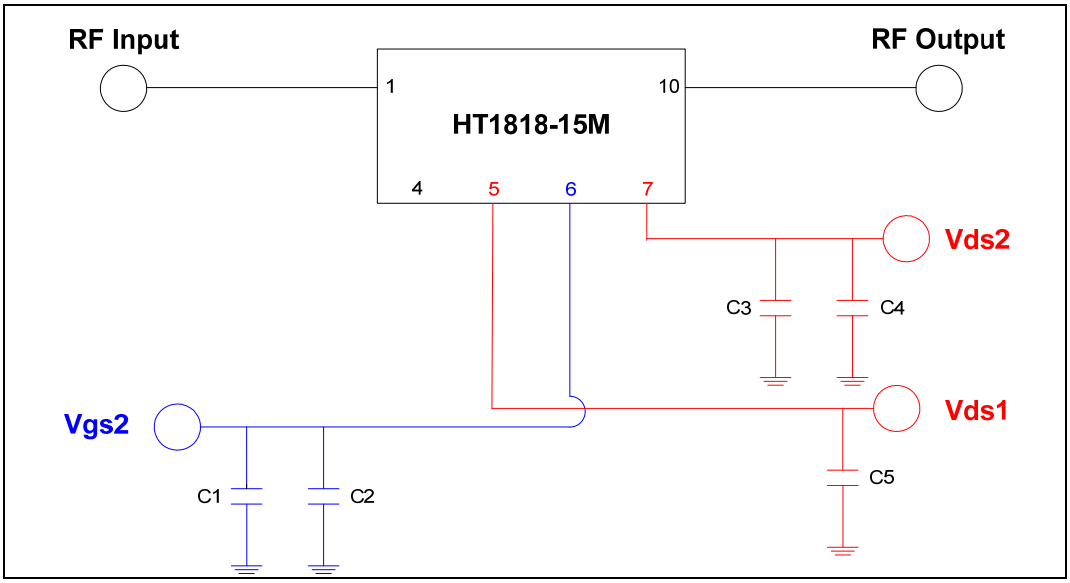
Operating Voltages

PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage	V	4.75	5	5.25	Vds1
		27.5	28	-	Vds2
Gate Voltage (on-stage)	V	-	Vgs2@Idq2	-2	Vgs 2
Gate Voltage (off-stage)	V	-	-8	-	Vgs 2

Block Diagram



Application Circuit



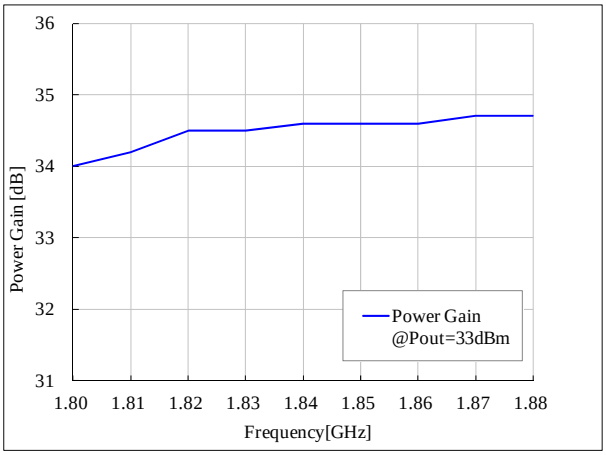
Part List

Location	Model No.	Spec.	Maker
C4	1812C225K101CT	2.2uF / 100V	WALSIN
C1, C5	C3216X7R1C106K	10uF / 16V	TDK
C2, C3	201CHA100JSLE	10pF	TEMEX
Evaluation Board	RO4350B	2Layer, 30mil	ROGERS

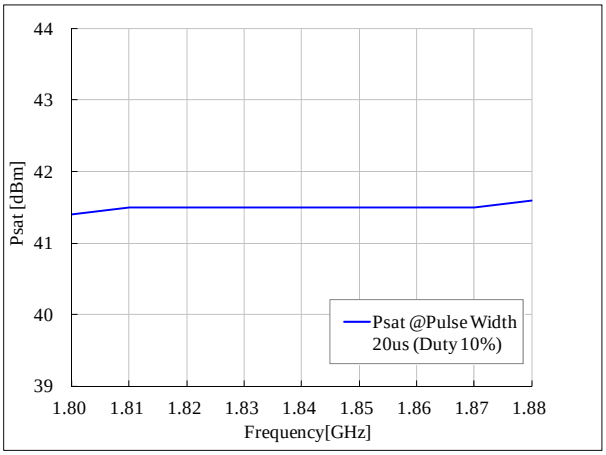
Performance Charts

* **Bias condition** @ Idq1= 140mA, Idq2= 105mA, Ta=25℃

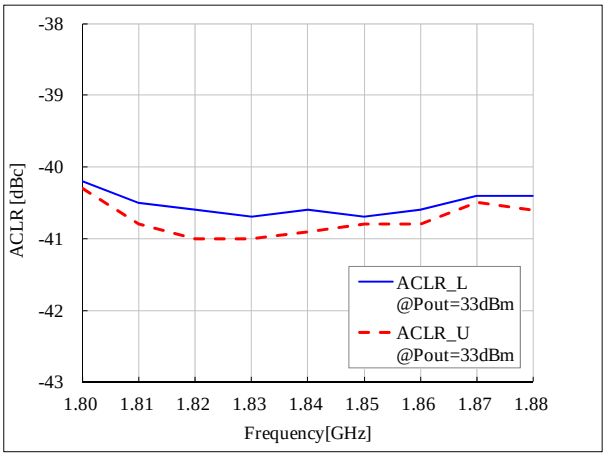
Power Gain vs. Frequency



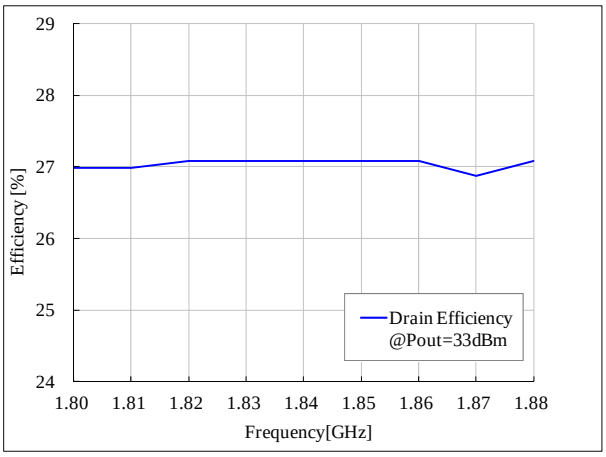
Psat vs. Frequency



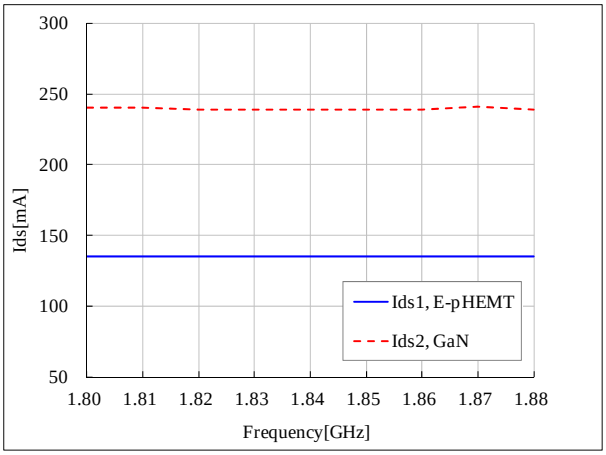
ACLR vs. Frequency



Efficiency vs. Frequency



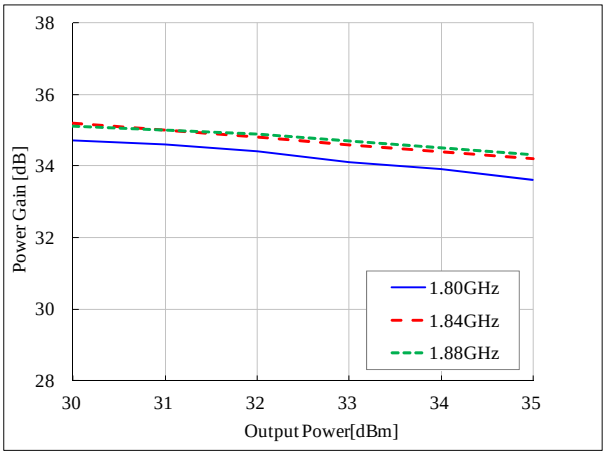
Ids1 vs. Ids2 vs. Frequency



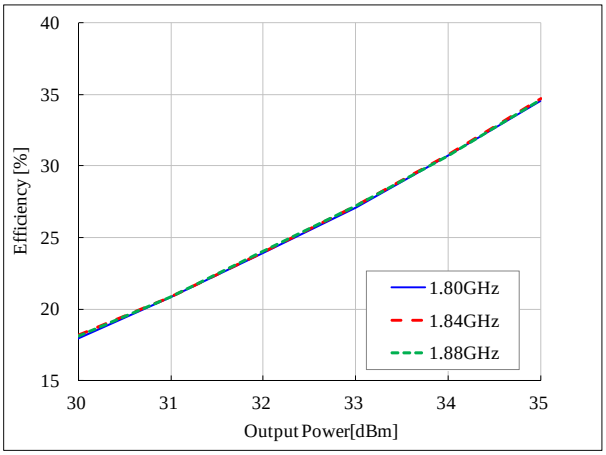
Performance Charts

* **Bias condition** @ Idq1= 140mA, Idq2= 105mA, Ta=25℃

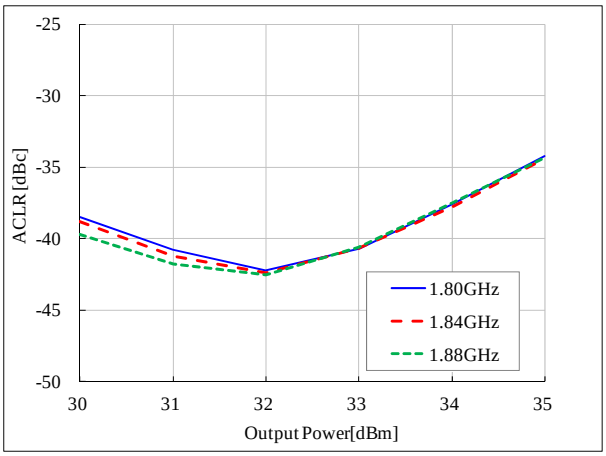
Power Gain vs. Output Power



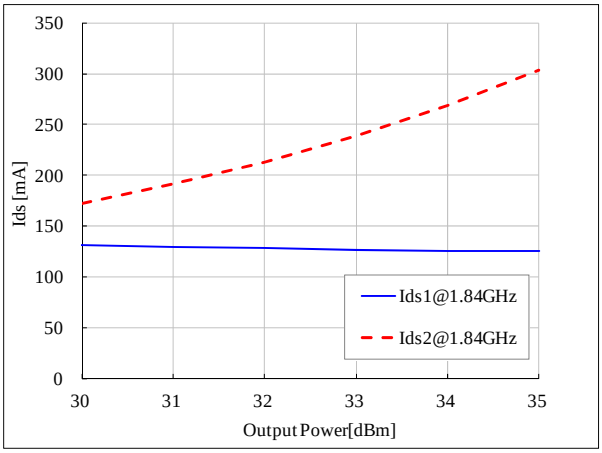
Efficiency vs. Output Power



ACLR vs. Output Power



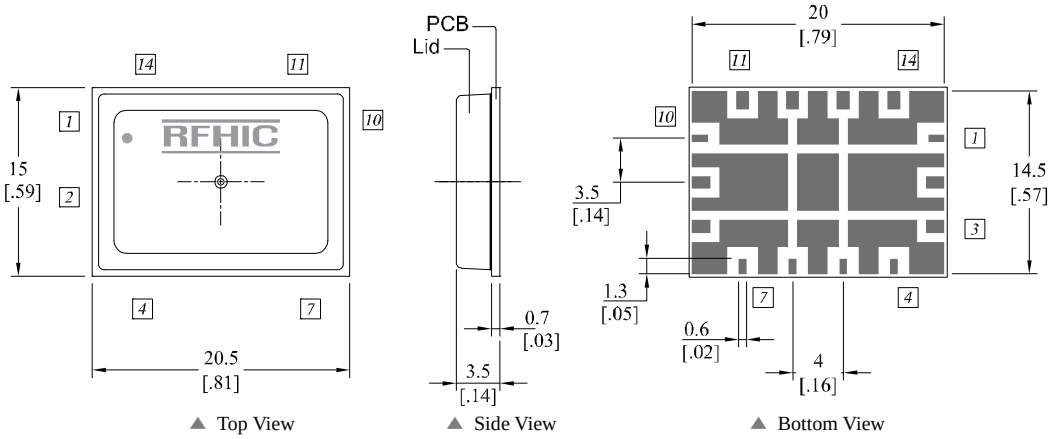
Ids1 vs. Ids2 vs. Output Power



*LTE 10MHz (PAPR=7.5dB) w/o DPD

Package Dimensions (Type: NP-1EL)

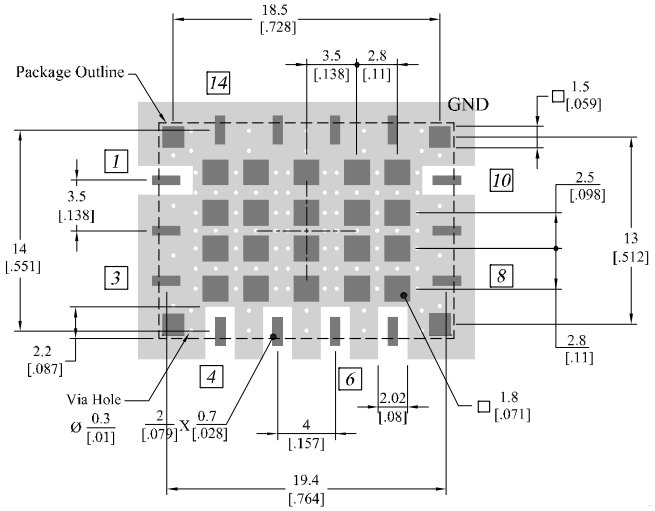
* Unit: mm[inch] | Tolerance: ±0.15[.006]



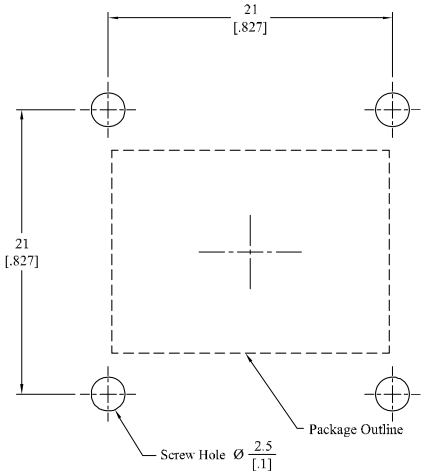
▲ Top View ▲ Side View ▲ Bottom View

Pin Description							
Pin No	**Function**	**Pin No**	**Function**	**Pin No**	**Function**	**Pin No**	**Function**
1	RF Input	4	N.C	8	GND	11	GND
2	GND	5	Vds1	9	GND	12	GND
3	GND	6	Vgs2	10	RF Output	13	GND
-	-	7	Vds2	-	-	14	GND

Recommended Pattern



Recommended Mounting Configuration



*** Mounting Configuration Notes**

1. For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.
2. To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws be added near the heatsink to mount the board
3. In designing the necessary RF trace, width will depend upon the PCB material and construction.
4. Use 1 oz. Copper minimum thickness for the heatsink.
5. Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
6. We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Precautions

This product is a Gallium Nitride Transistor.
The Gallium Nitride Transistor requires a Negative Voltage Bias which operates alongside a Positive Voltage Bias. These Biases are applied in accordance to the Sequence during Turn-On and Turn-Off.
The Pallet Amplifier does not have a built-in Bias Sequence Circuit. Therefore, users need to either apply positive voltages and negative voltages in the required sequence, or add an external Bias Circuit to this Amplifier.
The required sequence for power supply is as follows.

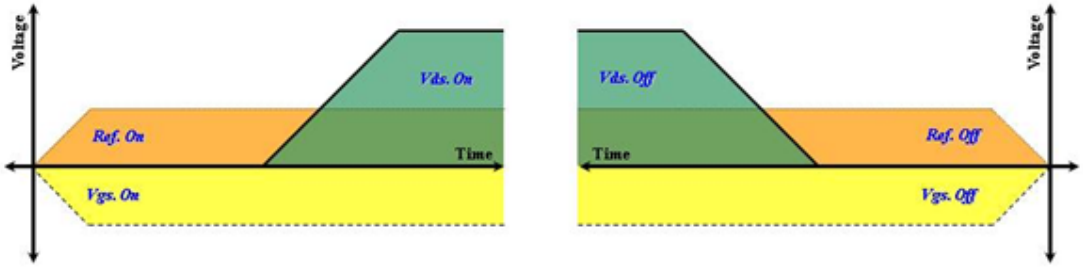
During Turn-On

1. Connect GND.
2. Apply Vgs2.
3. Apply Vds1 and Vds2
4. Apply the RF Power.

During Turn-Off

1. Turn off RF power.
2. Turn off Vds1 and Vds2, and then, turn off the Vgs2.
3. Remove all connections.

Turn On **Turn Off**



- Sequence Timing Diagram -

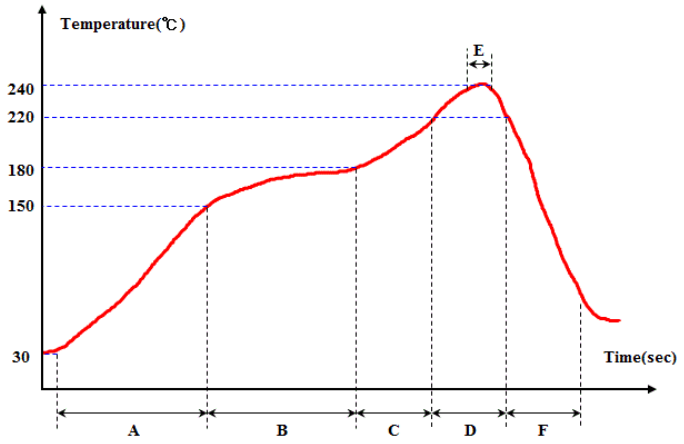
Reflow Profile

*** Reflow oven settings**

Zone	A	B	C	D	E	F
Temperature(°C)	30 ~ 150 ℃	150 ~ 180 ℃	180 ~ 220 ℃	220 ~ 220 ℃	235 ~ 240 ℃	2 ~ 6 ℃/ Sec Drop
Belt speed	55 ~ 115 sec	55 ~ 75 sec	30 ~ 50 sec	30 ~ 50 sec	5 ~ 10 sec	60 ~ 90 sec

Reflow Cycle Limit= 1time

*** Measured reflow profile**



Ordering Information

Part Number	Package Design
HT1818-15M	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

Revision History

Part Number	Release Date	Version	Modification	Data Sheet Status
HT1818-15M	2013.03.25	0.1	Initial Release of Data sheet	Preliminary