Agilent HSDL-3000 # 007/017 IrDA® Data Compliant 115.2 kbps Infrared Transceiver

Data Sheet

Description

The HSDL-3000 is a small form factor infrared (IR) transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data link. The module is compliant to IrDA Physical Layer Specifications 1.3 and is IEC 825-Class 1 eye safe.

The HSDL-3000 can be shut down completely to achieve very low power consumption. In the shutdown mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. Such features are ideal for battery-operated handheld products.

The HSDL-3000 has two front packaging type options (HSDL-3000#007/017). Both options have an integrated shield that helps to ensure low EMI emission and high immunity to EMI field, thus enhancing reliable performance.

Application Support Information

The Application Engineering group is available to assist you with the technical understanding associated with HSDL-3000 infrared transceiver module. You can contact them through your local sales representatives for additional details.

Applications

- **Data communication**
  - **PDAs**
  - **Notebooks**
  - **Printers**
- **Mobile telecom**
  - **Cellular phones**
  - **Pagers**
  - **Smart phones**
- **Digital imaging**
  - **Digital cameras**
  - **Photo-imaging printers**
- **Electronic wallet**
- **Medical and industry data collection**

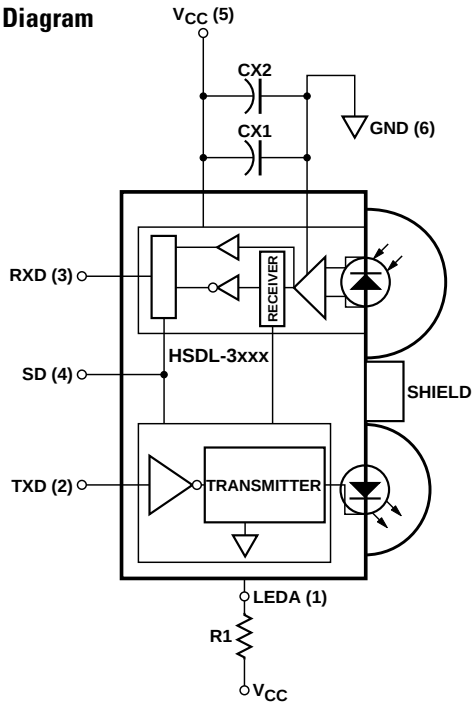
Features

- **Fully compliant to IrDA 1.3 specifications:**
  - **2.4 kbps to 115.2 kbps**
  - **Excellent nose-to-nose operation**
  - **Typical link distance > 1.5 m**
- **Guaranteed temperature performance, –20 to 70 °C**
  - **Critical parameters are guaranteed over temperature and supply voltages**
- **Low power consumption**
  - **Low shutdown current (10 nA typical)**
  - **Complete shutdown for TXD, RXD, and PIN diode**
- **Small module size**
  - **2.70 x 9.10 x 3.65 mm (HxWxD)**
- **Withstands >100 mV_{p-p} power supply ripple typically**
- **V_{CC} supply 2.7 to 5.5 volts**
- **LED stuck-high protection**
- **IEC 825-Class 1 eye safe**
- **Designed to accommodate light loss with cosmetic windows**

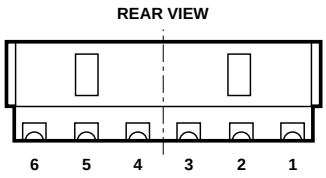
HSDL-3000 Ordering Information

Part Number	Packaging Type	Package	Quantity
HSDL-3000#007	Tape/Reel	Front View	2500
HSDL-3000#017	Strip	Front View	10

Functional Block Diagram



Pinout



I/O Pins Configuration Table

Pin	Symbol	Description	Notes
1	LED A	LED Anode	Tied through external resistor, R1, to regulated V_{CC} from 2.7 to 5.5 volts.
2	TXD	Transmitter Data Input. Active High.	Logic High turns on the LED. If held high longer than ~ 50 µs, the LED is turned off. TXD must be either driven high or low. Do NOT float the pin.
3	RXD	Receiver Data Output. Active Low.	Output is a low pulse response when a light pulse is seen.
4	SD	Shutdown. Active High.	Complete shutdown TXD, RXD, and PIN diode.
5	V_{CC}	Supply Voltage	Regulated, 2.7 to 5.5 volts.
6	GND	Ground	Connect to system ground.
–	SHIELD	EMI Shield	Connect to system ground via a low inductance trace. For best performance, do not connect to GND directly at the part.

Recommended Application Circuit Components

Component	Recommended Value
R1	2.2 Ω ± 5%, 0.25 Watt, for 2.7 ≤ V_{CC} ≤ 3.3 V operation 2.7 Ω ± 5%, 0.25 Watt, for 3.0 ≤ V_{CC} ≤ 3.6 V operation 6.8 Ω ± 5%, 0.25 Watt, for 4.5 ≤ V_{CC} ≤ 5.5 V operation
CX1[1]	0.47 µF ± 20%, X7R Ceramic
CX2[2]	6.8 µF ± 20%, Tantalum

Notes:
1. CX1 must be placed within 0.7 cm of HSDL-3000 to obtain optimum noise immunity.
2. In environments with noisy power supplies, supply rejection can be enhanced by including CX2 as shown in "HSDL-3000 Functional Block Diagram"on page 2.

Marking Information

The HSDL-3000#007/017 is marked "YYWW" on the shield where 'YY' indicates the unit's manufacturing year, and 'WW' refers to the work week in which the unit is tested.

Caution: *The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken during handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.*

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	–40	100	°C	
Operating Temperature	T_A	–20	70	°C	
LED Supply Voltage	V_{LED}	0	7	V	
Supply Voltage	V_{CC}	0	7	V	
Output Voltage: RXD	V_O	–0.5	7	V	
LED Current Pulse Amplitude	ILED		500	mA	≤ 90 µs Pulse Width ≤ 20% Duty Cycle

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Conditions
Operating Temperature		T_A	–20	70	°C	
Supply Voltage		V_{CC}	2.7	5.5	V	
Logic Input Voltage for TXD	Logic High	V_{IH}	2/3 V_{CC}	V_{CC}	V	
	Logic Low	V_{IL}	0	1/3 V_{CC}	V	
Receiver Input Irradiance	Logic High	EI_H	0.0036	500	mW/cm^2	For in-band signals ≤ 115.2 kbps[1]
	Logic Low	EI_L		0.3	µW/cm^2	For in-band signals[1]
TXD Pulse Width (SIR)		t_{TPW} (SIR)	1.5	1.6	µs	t_{PW} (TXD) = 1.6 µs at 115.2 kbps
Receiver Data Rate			2.4	115.2	kbps	
Ambient Light		See Test Methods on page 16 for details.				

Electrical & Optical Specifications

Specifications (Min. and Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C with V_{CC} set to 3.0 V unless otherwise noted.

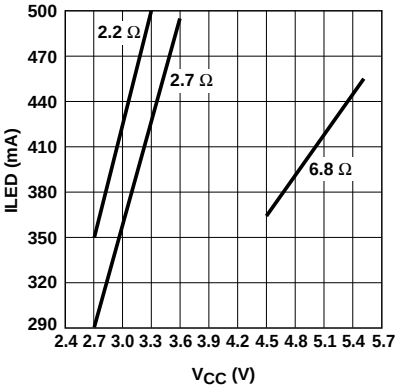
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver						
Viewing Angle	$2\phi_{1/2}$	30			°	
Peak Sensitivity Wavelength	λ_p		875		nm	
RXD Output Voltage						
Logic High	V_{OH}	V_{CC} –0.2		V_{CC}	V	I_{OH} = –200 μA, EI ≤ 0.3 μW/cm^2
Logic Low	V_{OL}	0		0.4	V	
RXD Pulse Width (SIR)[2]	t_{RPW} (SIR)	1		7.5	μs	$\theta_{1/2} \leq 15°$, C_L = 9 pF
RXD Rise and Fall Times	t_r, t_f		25	100	ns	C_L = 9 pF
Receiver Latency Time[3]	t_L		25	50	μs	
Receiver Wake Up Time[4]	t_{RW}		18	100	μs	EI = 10 mW/cm^2
Transmitter						
Radiant Intensity	IE_H	44	75		mW/sr	I_{LEDA} = 350 mA, $\theta_{1/2} \leq 15°$, TXD ≥ V_{IH}, T_A = 25°C
Viewing Angle	$2\theta_{1/2}$	30		60	°	
Peak Wavelength	λ_p		875		nm	
TXD Logic Levels						
High	V_{IH}	2/3 V_{CC}		V_{CC}	V	
Low	V_{IL}	0		1/3 V_{CC}	V	
TXD Input Current						
High	I_H		0.02	1	μA	$V_I \geq V_{IH}$
Low	I_L	–1	–0.02	1	μA	$0 \leq V_I \leq V_{IL}$
LED Current						
Shutdown	I_{VLED}		20	1000	NA	V_I (SD) ≥ V_{IH}, T_A = 25°C
Wakeup Time[5]	t_{TW}		30	100	ns	
Maximum Optical Pulse Width[6]	$t_{PW(Max)}$		25	50	μs	
TXD Rise and Fall Time (Optical)	t_r, t_f			600	ns	
LED Anode on State Voltage	V_{ON} (LEDA)			2.2	V	I_{LEDA} = 350 mA, V_I (TXD) ≤ V_{IL}

Electrical & Optical Specifications (Continued)

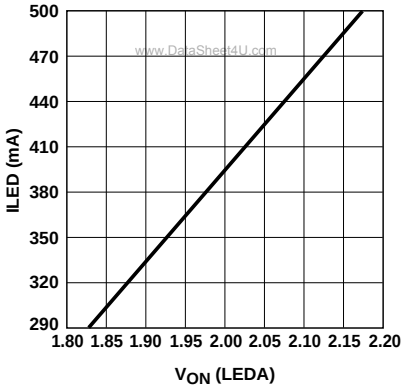
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Transceiver						
Input Current						
High	I_H		0.01	1	µA	$V_I \geq V_{IH}$
Low	I_L	–1	-0.02	1	µA	$0 \leq V_I \leq V_{IL}$
Supply Current						
Shutdown	I_{CC1}		0.01	1	µA	$V_{SD} \geq V_{CC} - 0.5$, $T_A = 25°C$
Idle	I_{CC2}		290	450	µA	$V_I(TXD) \leq V_{IL}$, EI = 0
Active	I_{CC3}		2	8	mA	$V_I(TXD) \geq V_{IL}$

Notes:

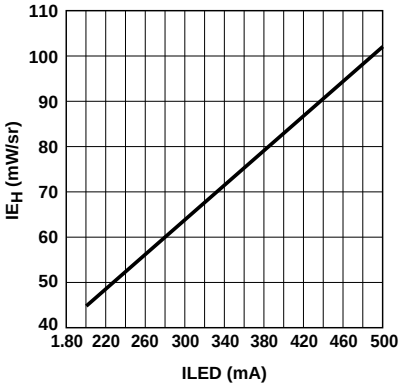
1. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 nm ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
2. For in-band signals 2.4 kbps to 115.2 kbps where 3.6 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.
3. Latency is defined as the time from the last TXD light output pulse until the receiver has recovered full sensitivity.
4. Receiver wake up time is measured from V_{CC} power on to valid RXD output.
5. Transmitter wake up time is measured from V_{CC} power on to valid light output in response to a TXD pulse.
6. Maximum optical pulse width is defined as the maximum time that the LED will remain on. This is to prevent the long turn on time for the LED.



ILED vs. V_{CC}.

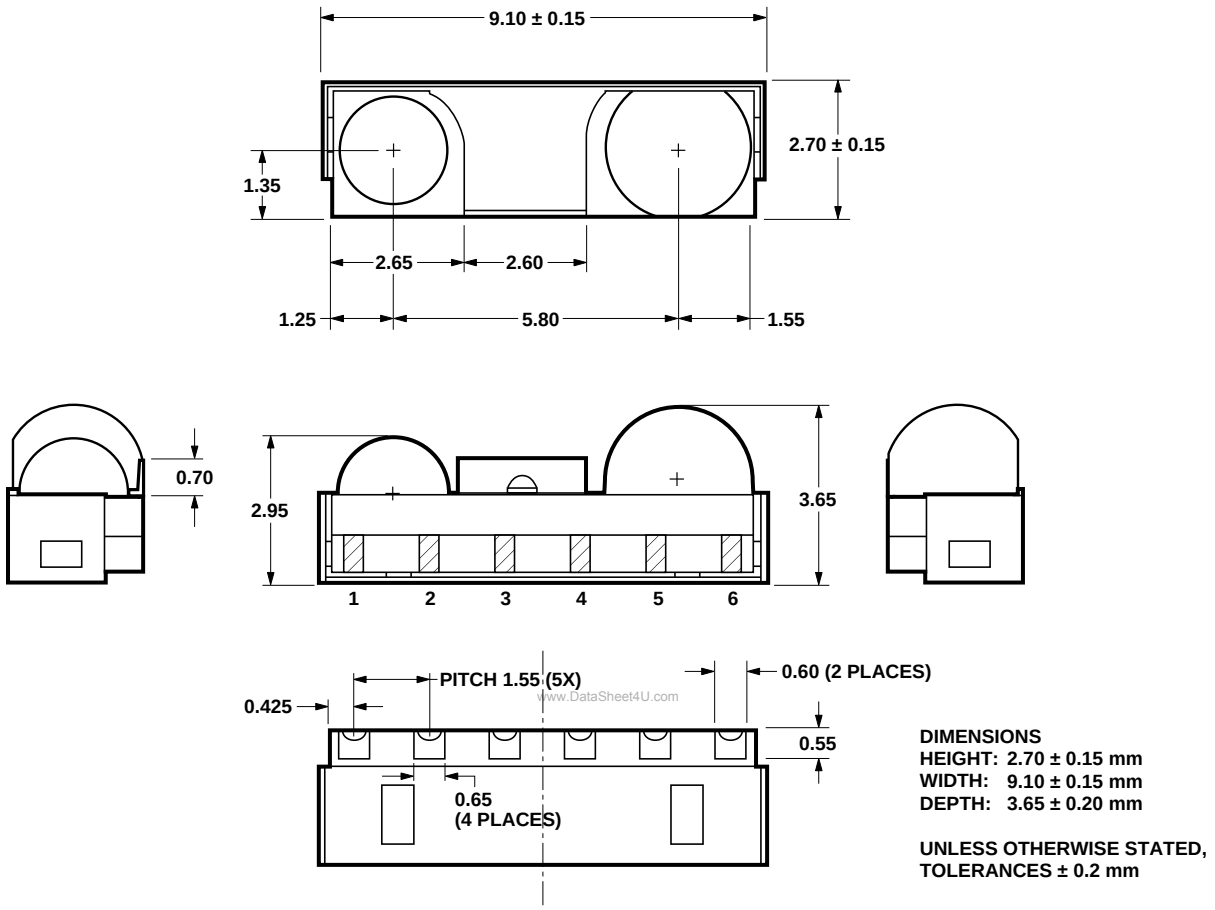


ILED vs. V_{ON} (LEDA).

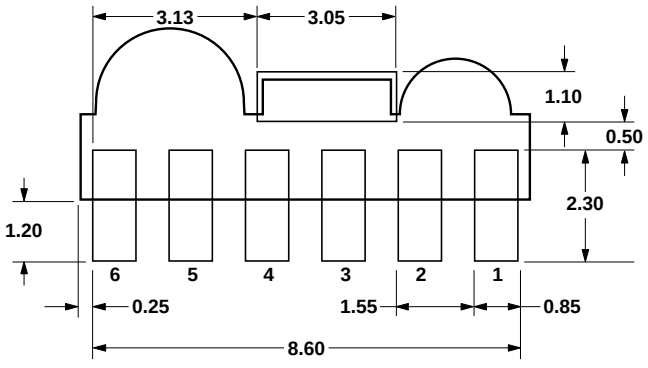


IE_H vs. ILED.

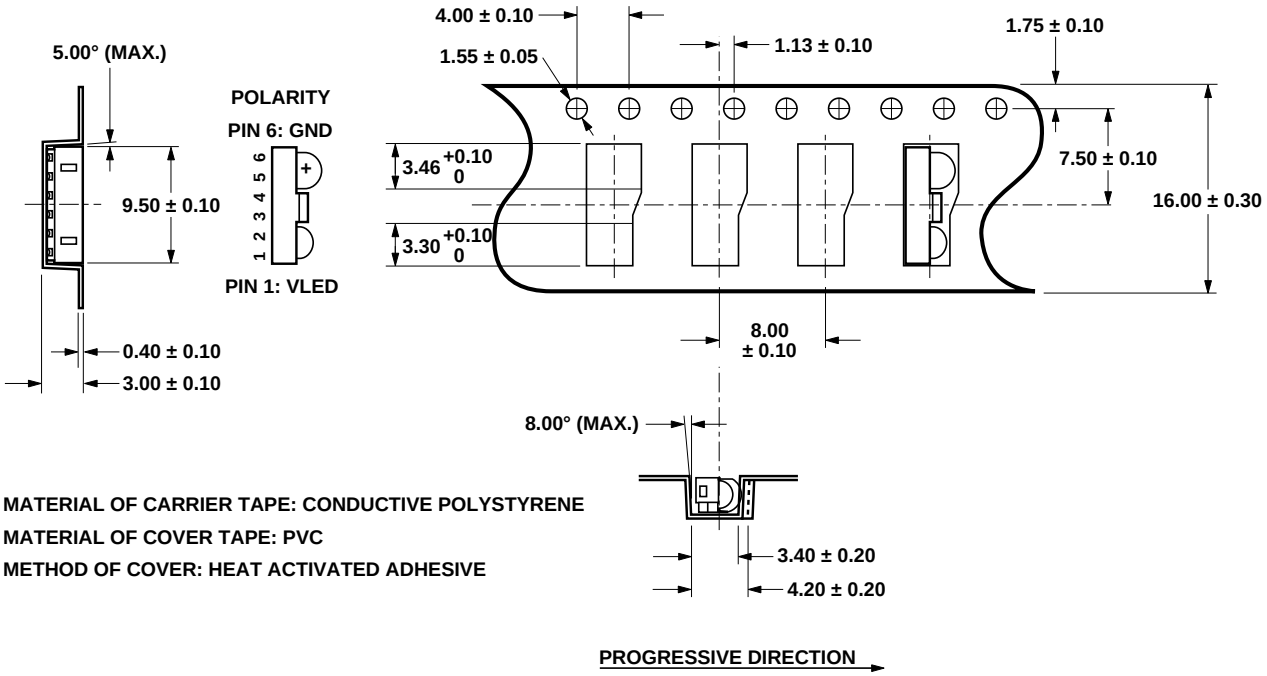
HSDL-3000#007 and HSDL-3000#017 Package Outline with Dimension and Recommended PC Board Pad Layout



RECOMMENDED LAND PATTERN

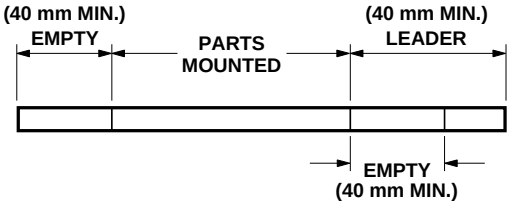


HSDL-3000#007 and HSDL-3000#017 Tape and Reel Dimensions



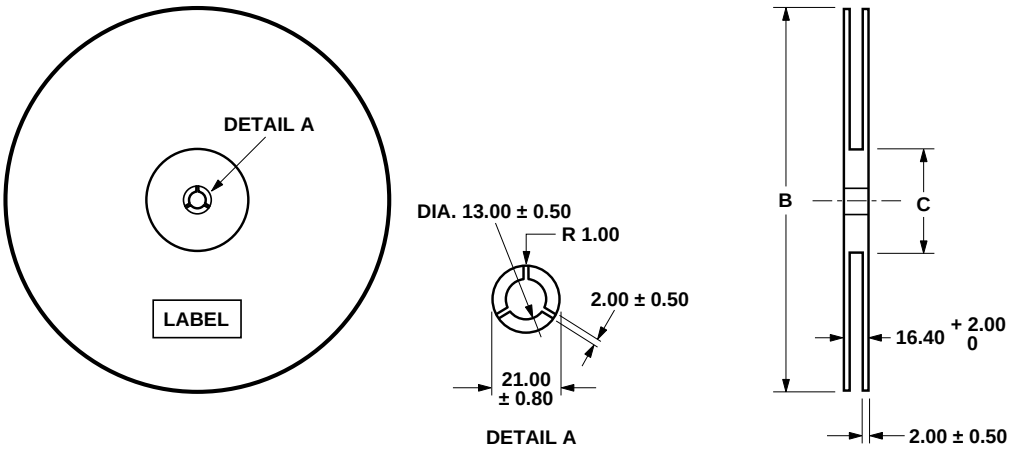
MATERIAL OF CARRIER TAPE: CONDUCTIVE POLYSTYRENE
MATERIAL OF COVER TAPE: PVC
METHOD OF COVER: HEAT ACTIVATED ADHESIVE

PROGRESSIVE DIRECTION



"B"	"C"	QUANTITY
330	80	2500

UNIT: mm



Moisture Proof Packaging

The HSDL-3000 is shipped in moisture proof packaging. Once opened, moisture absorption begins.

Recommended Storage Conditions

Storage Temperature	10 °C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

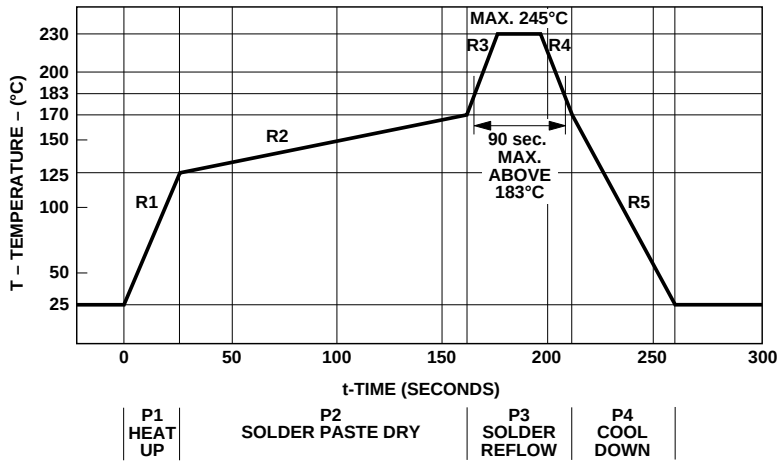
After removal from the bag, the parts should be soldered within two days if stored at the recommended storage conditions. If the parts have been removed from the bag for more than two days, the parts must be stored in a dry box.

Baking

If the parts are not stored in a dry environment, they must be baked before reflow process to prevent damage to parts. Baking should be done only once.

Packaging	Baking Temperature	Baking Time
In Reel	60°C	≥ 48 hours
In Bulk	100°C	≥ 4 hours
	125°C	≥ 2 hours
	150°C	≥ 1 hour

Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3	170°C to 230°C (245°C max.)	4°C/s
	P3, R4	230°C to 170°C	–4°C/s
Cool Down	P4, R5	170°C to 25°C	–3°C/s

The reflow profile is a straight line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed-circuit board connections.

In **process zone P1**, the PC board and HSDL-3000 castellation I/O pins are heated to a temperature of 125 °C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4 °C per second to allow for even heating of both the PC board and HSDL-3000 castellation I/O pins.

Process zone P2 should be of sufficient time duration (> 60 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed –3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3000 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3000 transceiver.

Appendix A : HSDL-3000#007/#017 SMT Assembly Application Note

1.0 Solder Pad, Mask and Metal Solder Stencil Aperture

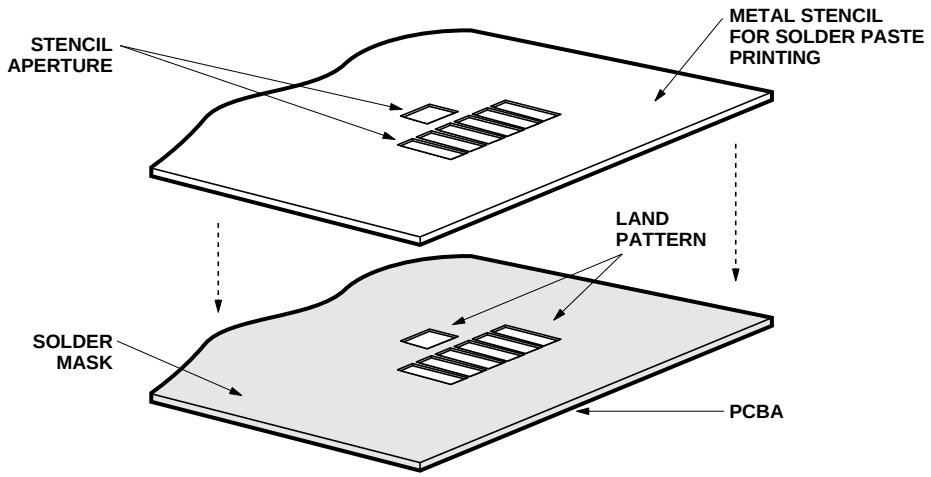


Figure 1. Stencil and PCBA.

1.1 Recommended Land Pattern for HSDL-3000

DIM.	mm	INCHES
a	2.30	0.091
b	0.85	0.034
c (PITCH)	1.55	0.061
d	1.10	0.043
e	3.05	0.120
f	2.20	0.087
g	2.42	0.095
h	0.20	0.008

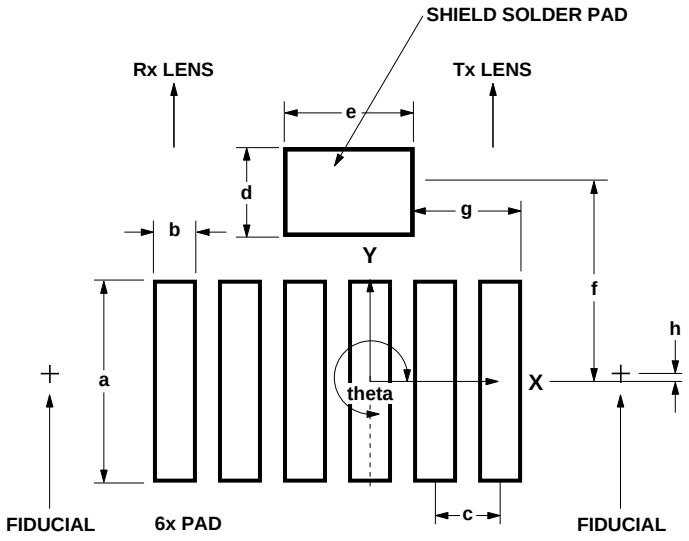


Figure 2. Top view of land pattern.

1.2 Adjacent Land Keep-out and Solder Mask Areas

Dim.	mm	Inches
h	min. 0.40	min. 0.016
j	10.1	0.40
k	3.85	0.15
l	3.2	0.126

- Adjacent land keep-out is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.
- "h" is the minimum solder resist strip width required to avoid solder bridging adjacent pads.
- It is recommended that 2 fiducial cross be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

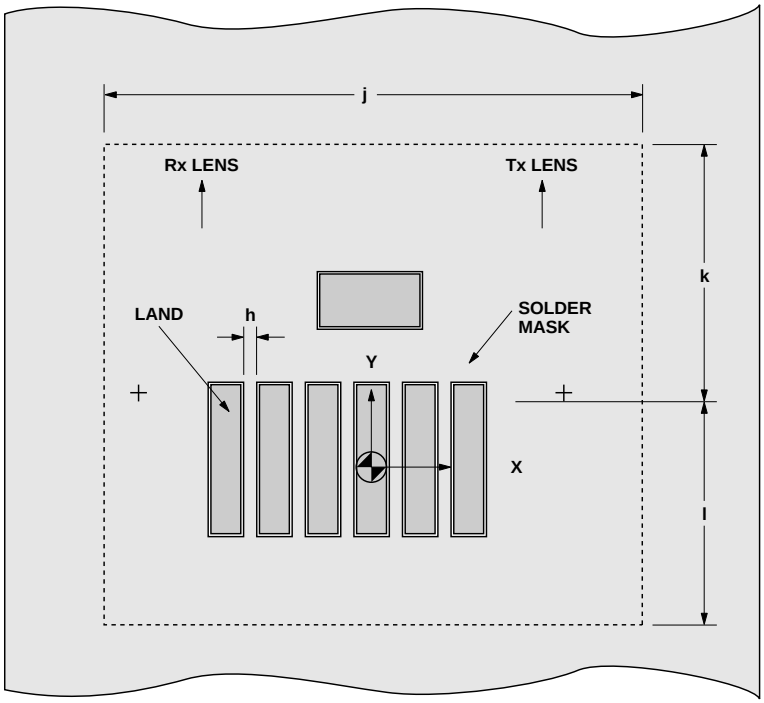


Figure 3. HSDL-3000#007/#017 PCBA – Adjacent land keep-out and solder mask.

2.0 Recommended Solder Paste/ Cream Volume for Castellation Joints

The recommended printed solder paste volume required per castellation pad is 0.30 cubic mm (based on either no-clean or aqueous solder cream types with typically 60 to 65% solid content by volume).

2.1 Recommended Metal Solder Stencil Aperture

It is recommended that only 0.152 mm (0.006 inches) or 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. The following combination of metal stencil aperture and metal stencil thickness should be used:

See Fig. 4.			
t, Nominal Stencil Thickness		**l, Length of Aperture**	
mm	**inches**	**mm**	**inches**
0.152	0.006	2.3 ± 0.05	0.091 ± 0.002
0.127	0.005	2.75 ± 0.05	0.108 ± 0.002
	w, the width of aperture, is fixed at 0.85 mm (0.034 inches).		
Aperture opening for shield pad is 3.05 mm x 1.1 mm as per land dimension.			

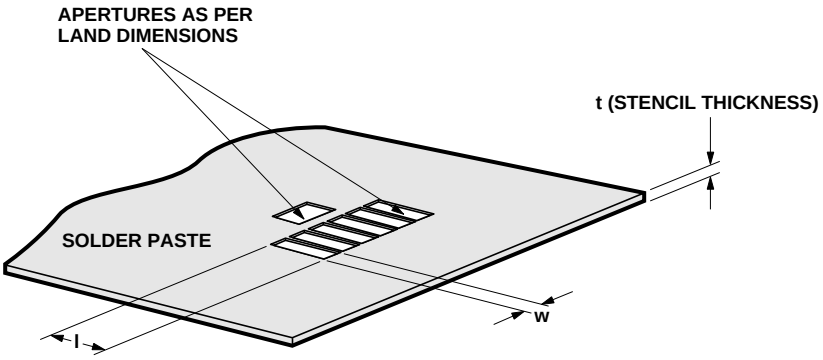


Figure 4. Solder paste stencil aperture.

Appendix B: HSDL-3000#007/#017 – Recommended Optical Port Design

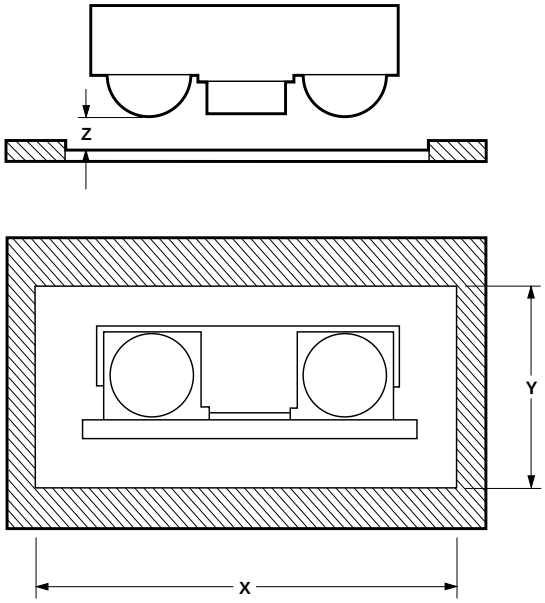
To insure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30 degrees, the maximum, to a cone angle of 60 degrees.

X is the width of the window, Y is the height of the window, and Z is the distance from the HSDL-3000 to the back of the window.

The distance from the center of the LED lens to the center of the photodiode lens is 5.80 mm. The equations for the size of the window are as follows:

$X = 5.80 + 2(Z + D) \tan \theta$
$Y = 2(Z + D) \tan \theta$

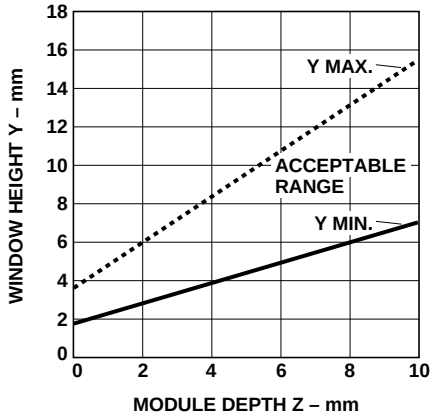
Where θ is the required half angle for viewing. For the IrDA minimum, it is 15 degrees, for the IrDA maximum it is 30 degrees. (D is the depth of the LED image inside the part, 3.2 mm from the Tx lens vertex). These equations result in the following tables and graphs:



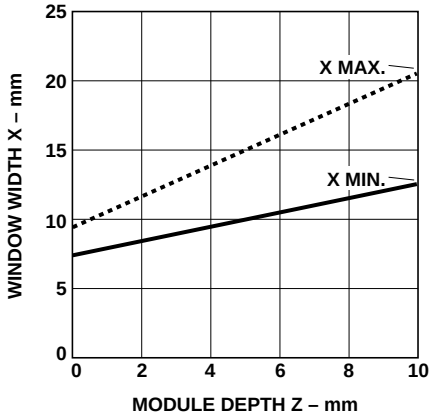
Minimum and Maximum Window Sizes

Dimensions are in mm.

Depth (Z) mm	X min.	Y min.	X max.	Y max.
0	7.34	1.71	9.33	3.70
1	7.88	2.25	10.48	4.85
2	8.42	2.79	11.63	6.00
3	8.95	3.32	12.79	7.16
4	9.49	3.86	13.94	8.31
5	10.02	4.39	15.10	9.47
6	10.56	4.93	16.25	10.62
7	11.10	5.47	17.41	11.78
8	11.63	6.00	18.56	12.93
9	12.17	6.54	19.72	14.09
10	12.70	7.07	20.87	15.24
11	13.24	7.61	22.03	16.40
12	13.77	8.14	23.18	17.55
13	14.31	8.68	24.34	18.71
14	14.85	9.22	25.49	19.86
15	15.38	9.75	26.65	21.01
16	15.92	10.29	27.80	22.17
17	16.46	10.83	28.95	23.32
18	16.99	11.36	30.11	24.48
19	17.53	11.90	31.26	25.63
20	18.06	12.43	32.42	26.79



Window height Y vs. module depth Z.



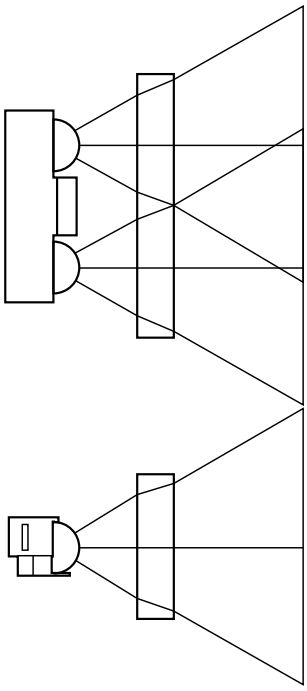
Window width X vs. module depth Z.

Shape of the Window

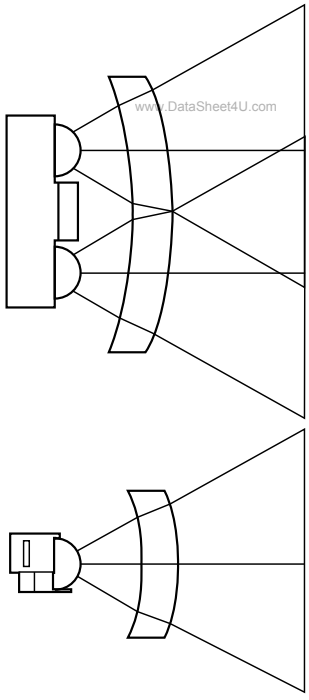
From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical design reasons, place a curve on the back side of the window that has the same radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

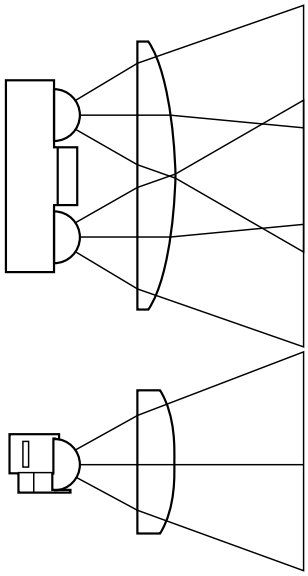
The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.



Flat Window
(first choice)



Curved Front and Back
(second choice)



Curved Front, Flat Back
(do not use)

Test Methods

Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

1. Electromagnetic field:
   3 V/m maximum (please refer to IEC 61000-4-3 severity level 3 for details).

2. Sunlight:
   10 kilolux maximum at the optical port. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased to provide 490 $\mu W/cm^2$ (with no modulation) at the optical port. The light source faces the optical port.

   This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radation is covered by the incandescent condition.

3. Incandescent Lighting:
   1000 lux maximum. This is produced with general service, tungsten-filament, gas-filled, inside frosted lamps in the 60 Watt to 100 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 Kelvin range and a spectral peak in the 850 to 1050 nm range.

4. Fluorescent Lighting:
   1000 lux maximum. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 $\mu W/cm^2$ minimum and 0.3 $\mu W/cm^2$ peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

   Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

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