Unit: mm

TOSHIBA Multichip Discrete Device

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HN7G10FE

Power Management Switch Applications
Driver Circuit Applications
Interface Circuit Applications

Q1 (transistor): 2SC5376F equivalent

• Q2 (MOSFET): SSM3K03FE equivalent

Q1 (transistor) Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	
Collector-base voltage	V_{CBO}	15	٧	
Collector-emitter voltage	V _{CEO}	12	V	
Emitter-base voltage	V _{EBO}	5	٧	
Collector current	I _C	400	mA	
Base current	Ι _Β	50	mA	

Q2 (MOSFET) Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V _{DS}	20	٧	
Gate-source voltage	V _{GSS}	10	V	
Drain current	I _D	50	mA	

1.6±0.05 1.2±0.05 0.2±0.05 1.6±0.05 1. 2. **EMITTER BASE** 3. DRAIN 4. SOURCE GATE COLLECTOR ES6 JEDEC JEITA **TOSHIBA** 2-2J1A

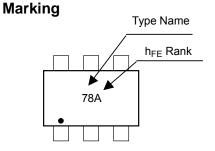
Weight: 0.003 g (typ.)

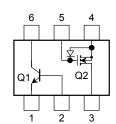
Q1, Q2 Common Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power dissipation	P _C (Note 1)	100	mW
Junction temperature	Tj	150	°C
Storage temperature range	T _{stg}	-55~150	°C

Note 1: Total rating

Pin Assignment (top view)





Q1 (transistor) Electrical Characteristics (Ta = 25°C)

taSheet4U.ccCharacteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Collector cutoff current	I _{CBO}	$V_{CB} = 15 \text{ V}, I_{E} = 0$	_	_	0.1	μА
Emitter cutoff current	I _{EBO}	$V_{EB} = 5 \text{ V}, I_{C} = 0$	_	_	0.1	μА
DC current gain	h _{FE} (Note 2)	$V_{CE} = 2 \text{ V}, I_{C} = 10 \text{ mA}$	300	_	1000	
Collector-emitter saturation voltage	V _{CE} (sat) (1)	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$	_	15	30	mV
	V _{CE (sat) (2)}	$I_C = 200 \text{ mA}, I_B = 10 \text{ mA}$	_	110	250	1110
Base-emitter saturation voltage	V _{BE (sat)}	$I_C = 200 \text{ mA}, I_B = 10 \text{ mA}$		0.87	1.2	V

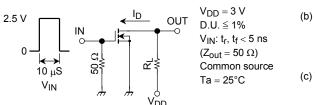
Note 2: hFE classification A: 300~600, B: 500~1000

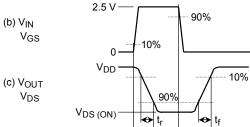
Q2 (MOSFET) Electrical Characteristics (Ta = 25°C)

Chara	octeristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage curre	ent	I _{GSS}	$V_{GS} = 10 \text{ V}, V_{DS} = 0$	_	_	1	μА
Drain-source brea	kdown voltage	V (BR) DSS	$I_D = 100 \ \mu A, \ V_{GS} = 0$	20	_	_	V
Drain cutoff curren	nt	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	_	_	1	μА
Gate threshold vol	tage	V _{th}	$V_{DS} = 3 \text{ V}, I_{D} = 0.1 \text{ mA}$	0.7	_	1.3	V
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = 3 V$, $I_D = 10 \text{ mA}$	25	50	_	mS
Drain-source ON-r	resistance	R _{DS (ON)}	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$	_	4	12	Ω
Input capacitance		C _{iss}	$V_{DS} = 3 V$, $V_{GS} = 0$, $f = 1 MHz$	_	11.0	_	pF
Reverse transfer of	apacitance	C _{rss}	$V_{DS} = 3 V$, $V_{GS} = 0$, $f = 1 MHz$	_	3.3	_	pF
Output capacitance		C _{oss}	$V_{DS} = 3 V$, $V_{GS} = 0$, $f = 1 MHz$	_	9.3	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = 3 \text{ V}, \text{ I}_D = 10 \text{ mA}, \text{ V}_{GS} = 0 \sim 2.5 \text{ V}$	_	0.16	_	0
	Turn-off time	t _{off}	$V_{DD} = 3 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0~2.5 \text{ V}$	_	0.19	_	μS

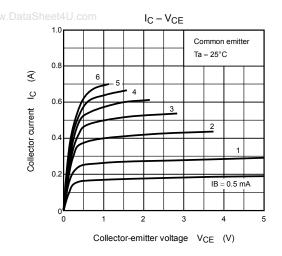
Switching Time Test Circuit

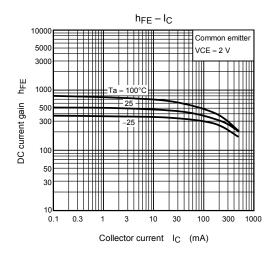
(a) Switching time test circuit

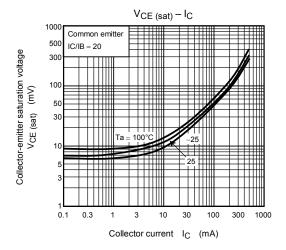


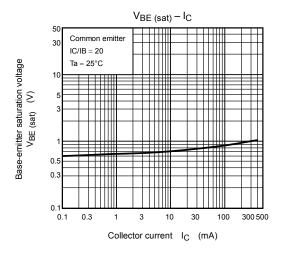


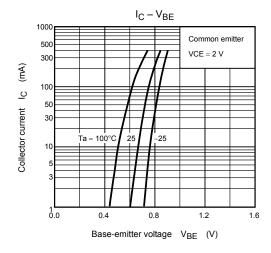
Q1 (Transistor)

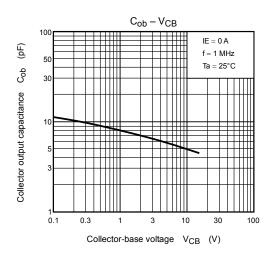




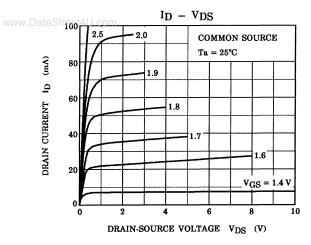


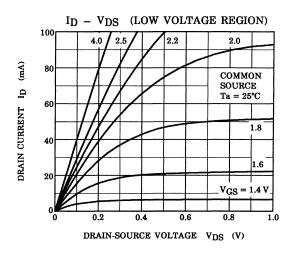


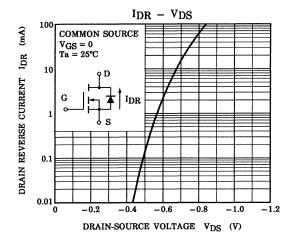


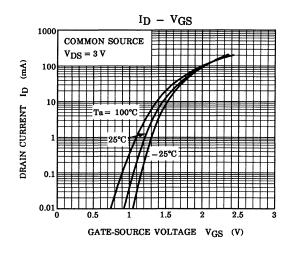


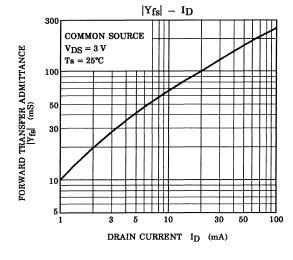
Q2 (S-MOS)

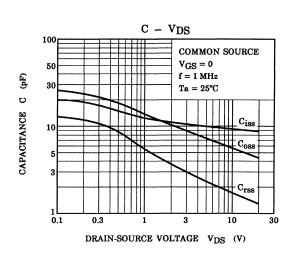




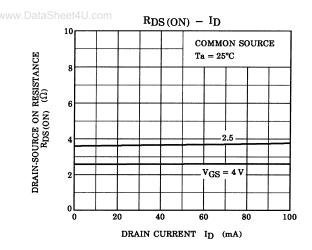


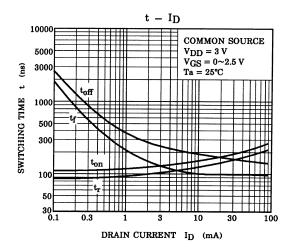


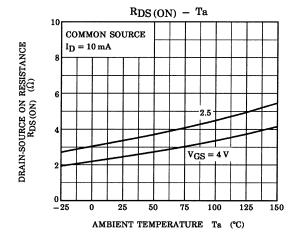




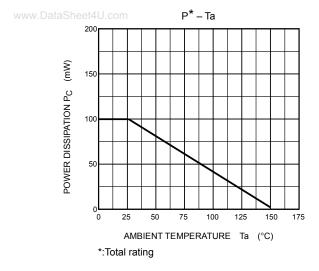
Q2 (S-MOS)







Q1, Q2 Common



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