HN624316 Series

High Speed 1048576-word × 16-bit / 2097152-word × 8-bit
CMOS Mask Programmable Read only Memory

HITACHI

Rev. 0.0
Dec. 1, 1995

Description

The HN624316 is a 16-Mbit CMOS mask-programmable ROM organized either as 1048576 words by 16 bits or as 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8086 and 68000 e.t.c..

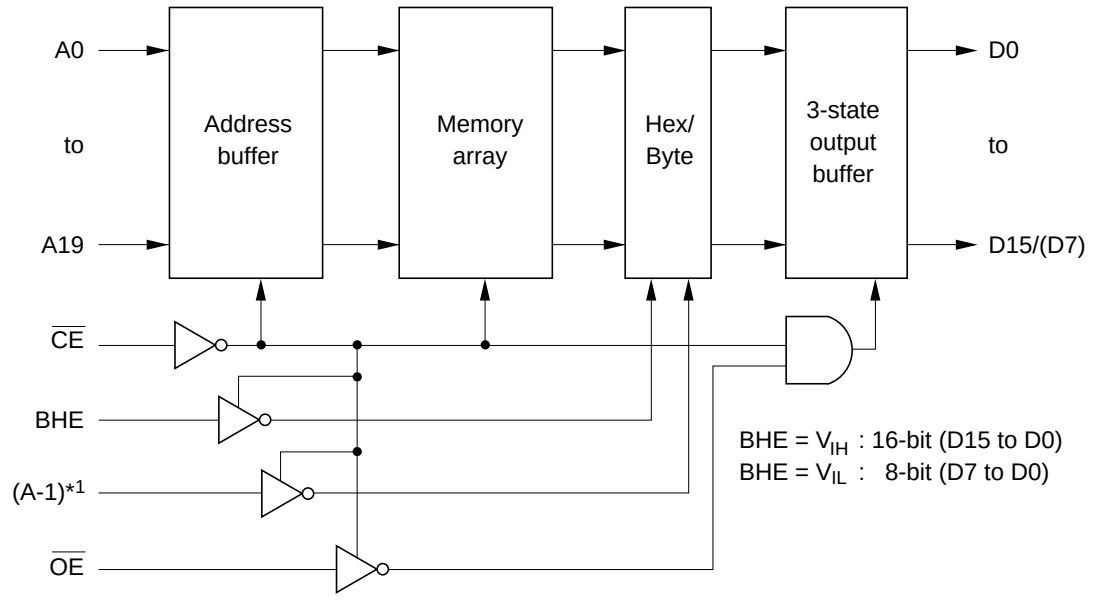
Features

- Single +5 V power supply
- Maximum access time: 120/150 ns (max)
- Low power consumption: 300 mW (typ) active
  5 µW (typ) standby
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access Time	Package
HN624316P-12	120 ns	600 mil 42-pin plastic DIP (DP-42)
HN624316P-15	150 ns	
HN624316FB-12	120 ns	44-pin plastic SOP (FP-44D)
HN624316FB-15	150 ns	

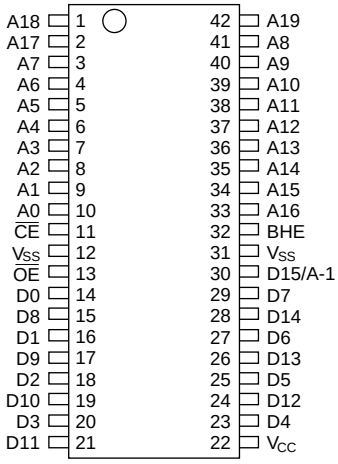
Block Diagram



Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

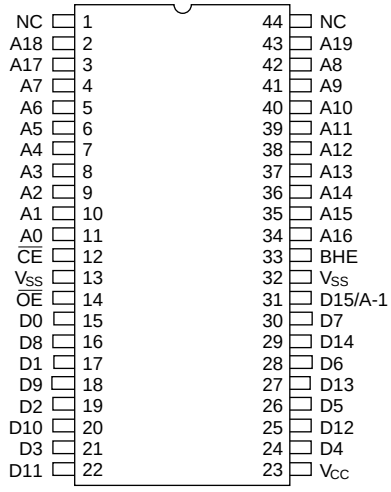
Pin Arrangement

HN624316P



(Top view)

HN624316FB



(Top view)

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	−0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	−0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	−55 to +125	°C	
Temperature under bias	Tbias	−20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test Conditions
Supply current	Active	I_{CC}	—	90/80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 120 ns/150 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq 2.2$ V
Input leakage current		$\lvert I_{IL} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leakage current		$\lvert I_{OL} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta =25°C, V_{IN} = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

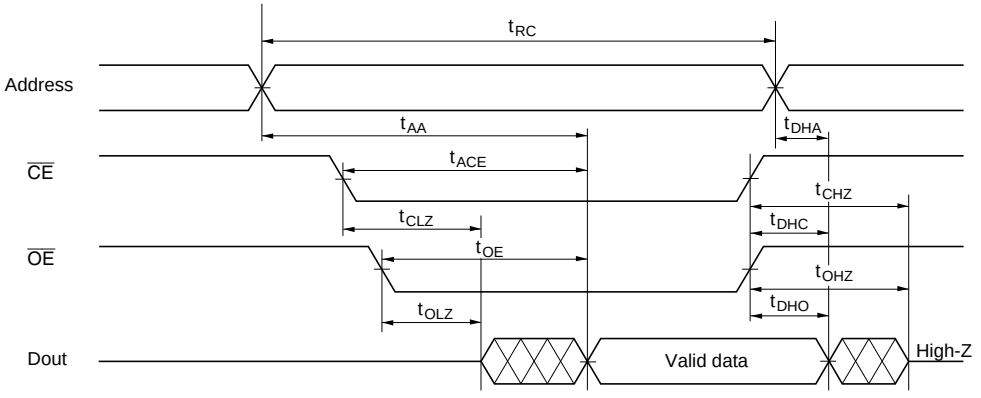
- Output load: 1TTLgate + C_L = 100 pF
  (including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

		HN624316-12		HN624316-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	120	—	150	—	ns
Address access time	t_{AA}	—	120	—	150	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	55	—	70	ns
BHE access time	t_{BHE}	—	120	—	150	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ} *1	—	40	—	70	ns
$\overline{OE}$ to output in high-Z	t_{OHZ} *1	—	40	—	70	ns
BHE to output in high-Z	t_{BHZ} *1	—	40	—	70	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ} and t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels..

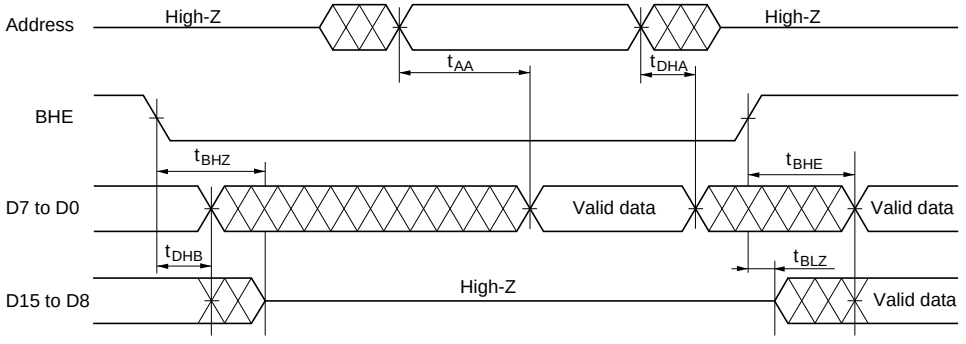
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



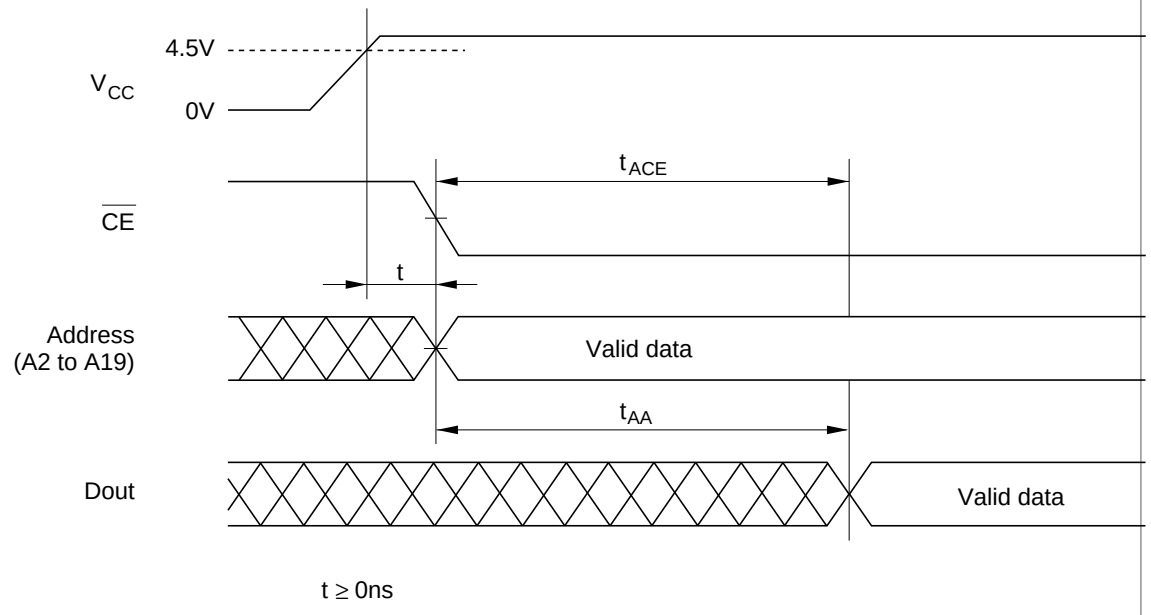
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Power Up Sequence

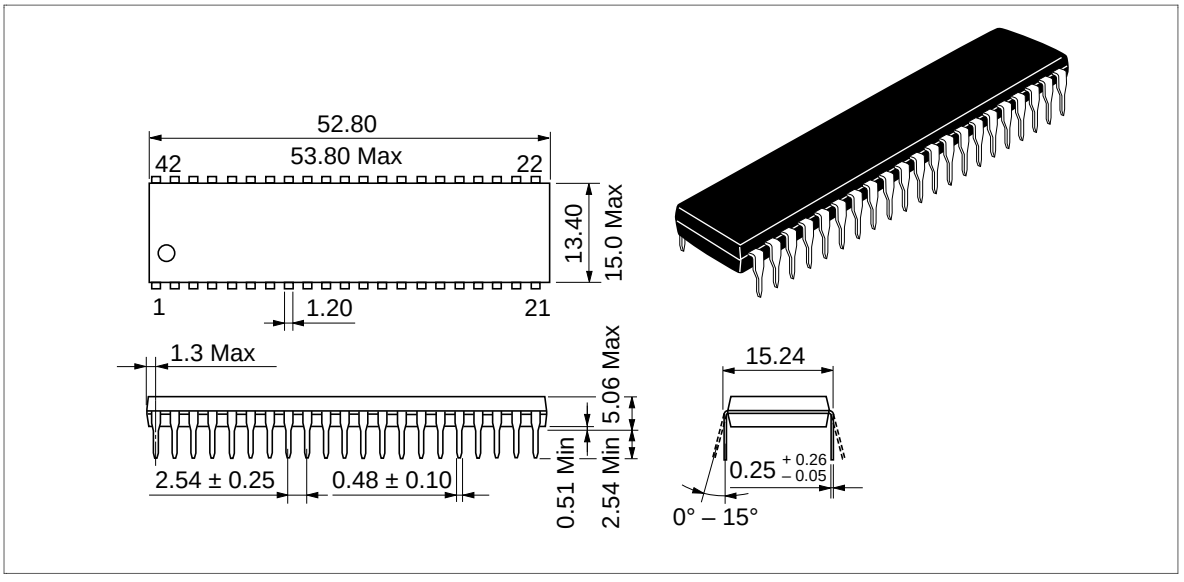


$t \geq 0ns$

Notes: This device is used ATD (Address Transient Detector). Therefore, Transfer either $\overline{CE}$ or address (A2 to A19) after power up to 4.5 V.

Package Information

HN624316P Series (DP-42) Unit: mm



HN624316FB Series (FP-44D) Unit: mm