HN62304B Series
HN62324B Series

T-46-13-15

524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62304B, HN62324B Series is a 4-Mbit CMOS mask-programable ROM organized as 524288-word x 8-bits. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

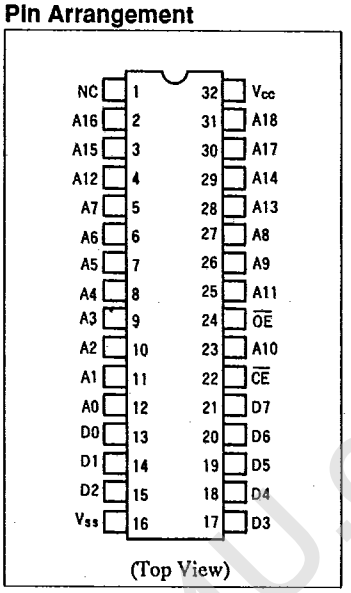
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max.)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide Data Organization

Ordering Information

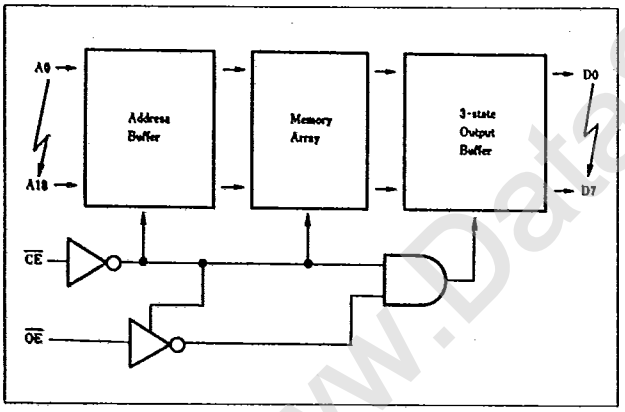
Type No.	Address Access Time	Package
HN62304BP	200 ns	600 mil 32-pin
HN62324BP	150 ns	plastic DIP
HN62304BF	200 ns	32-pin
HN62324BF	150 ns	plastic SOP

Pin Arrangement



(Top View)

Block Diagram



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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	−0.3 to +7.0	V
Terminal voltage*1	VT	−0.3 to Vcc + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Bias temperature	Tbias	−20 to +85	°C

Note: *1. With respect to Vss.

Recommended Operating Conditions (Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	Vcc + 0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Characteristics (Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	Icc	—	50	mA	Vcc = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	Vcc = 5.5 V, $\overline{CE}$ ≥ Vcc − 0.2 V
Input leak current		$\|I_{LI}\|$	—	10	µA	V_{IN} = 0 to Vcc
Output leak current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to Vcc
Output voltage		V_{OH}	2.4	—	V	I_{OH} = −205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (Vcc = 5 V ± 10%, Vss = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

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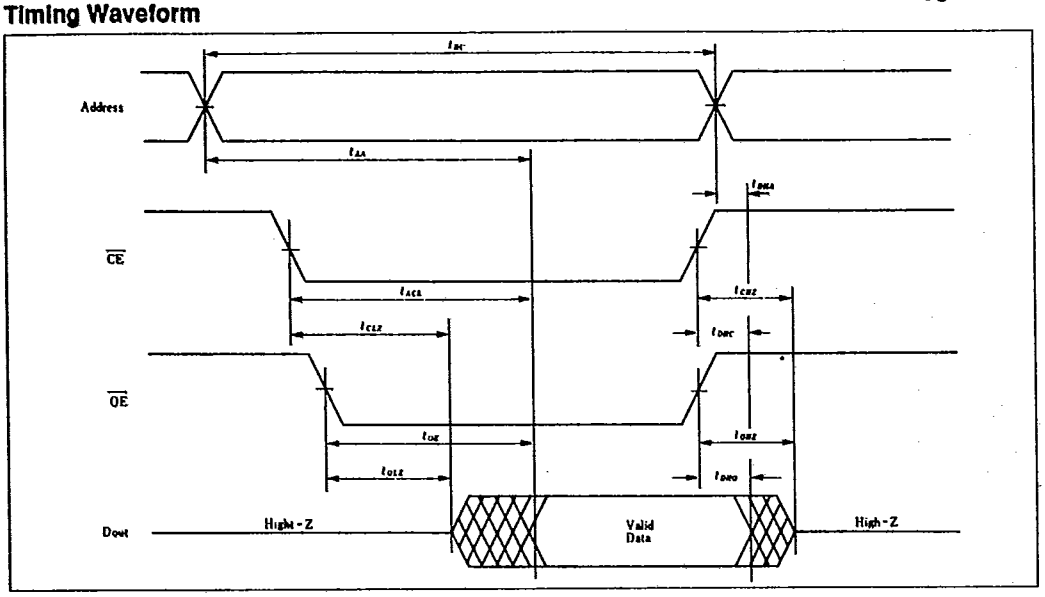
Test Conditions

Input pulse level:	0.8 to 2.4 V	Output load:	1 TTL gate + C_L = 100 pF (including jig capacitance)
I/O timing reference level:	1.5 V		
Input rise/fall time:	10 ns		

Item	Symbol	HN62324B		HN62304B		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

Timing Waveform



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.