

HN27C4096HG/HCC Series

262,144-word × 16-bit CMOS UV Erasable and Programmable ROM

T-46-13-29

HITACHI/ LOGIC/ARRAYS/MEM

HN27C4096HG/HCC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4096HG/HCC makes high speed sub 100 ns access time possible. Therefore, it is suitable for fast 16-bit and 32-bit microcomputer systems using high speed microcomputer such as the 80286/80386 and 68020/68030. The HN27C4096 HG/HCC offers high speed programming using page programming mode. This device has the package variation of cerdip 40-pin and JLCC 44-pin.

Ordering Informations

Type No.	Access time	Package
HN27C4096HG-85	85 ns	600-mil 40-pin Cerdip (DG-40A)
HN27C4906HCC-85	85 ns	44-pin JLCC (CC-44)

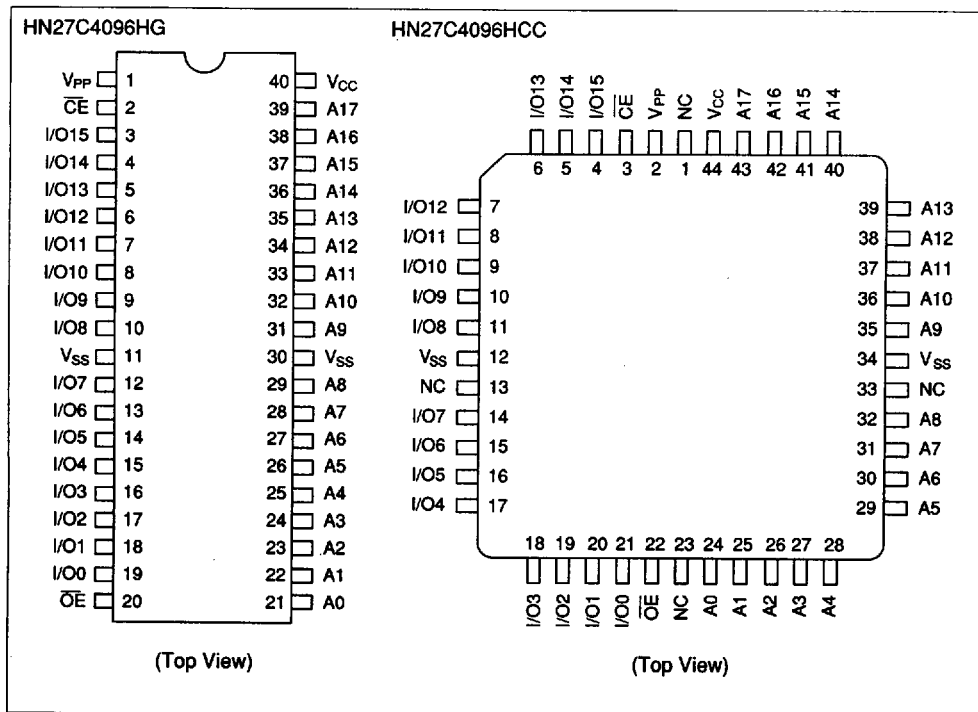
Features

- High speed
 - Access time: 85 ns (max)
- Low power dissipation
 - Active mode: 35 mW/MHz (typ)
- Fast high reliability page programming and fast high-reliability programming
 - Programming voltage: +12.5 V D.C.
 - Programming time: 3.5 sec. (min) (Theoretical in page programming)
- Inputs and outputs TTL compatible during both read and program modes.
- Pin arrangement: 40-pin JEDEC standard, 44-pin JLCC JEDEC standard
- Device identifier mode: Manufacturer code and device code

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Pin Arrangement



Pin Description

Pin name	Function
A0 – A17	Address
I/O0 – I/O15	Input/output
CE	Chip enable
OE	Output enable
VCC	Power supply
VPP	Programming power supply
VSS	Ground

The diagram illustrates the internal architecture of the 2048 x 2048 Memory Matrix. The main components are the X-Decoder, the 2048 x 2048 Memory Matrix, the Input Data Control, the Y-Gating, and the Y-Decoder. The chip is controlled by several pins: A7 and A17 are address inputs to the X-Decoder; I/O0 and I/O15 are data/control inputs to the Input Data Control and Y-Gating; CE (Chip Enable) and OE (Output Enable) are control inputs; VCC, VPP, and VSS are power supply pins. The Y-Decoder outputs address lines A0 through A6. A legend indicates that the 'H' symbol in a circle represents a High Threshold Inverter.

	Pin	CE	OE	A9	V _{PP}	V _{CC}	I/O
	CC	(3)	(22)	(35)	(2)	(44)	(4 – 11, 14 – 21)
Mode	G	(2)	(20)	(31)	(1)	(40)	(3 – 10, 12 – 19)
Read		V _{IL}	V _{IL}	×	V _{SS} – V _{CC}	V _{CC}	Dout
Output disable		V _{IL}	V _{IH}	×	V _{SS} – V _{CC}	V _{CC}	High-Z
Standby		V _{IH}	×	×	V _{SS} – V _{CC}	V _{CC}	High-Z

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Mode Selection (cont)

	Pin	CE	OE	A9	V _{PP}	V _{CC}	I/O
	CC	(3)	(22)	(35)	(2)	(44)	(4 – 11, 14 – 21)
Mode	G	(2)	(20)	(31)	(1)	(40)	(3 – 10, 12 – 19)
Page prog.	Page program set	V _{IH}	V _H ^{*2}	X	V _{PP}	V _{CC}	High-Z
	Page data latch	V _{IL}	V _H ^{*2}	X	V _{PP}	V _{CC}	Din
	Page program	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	High-Z
	Page program verify	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	Dout
	Page program reset	V _{IH}	V _{IH}	X	V _{CC}	V _{CC}	High-Z
Word prog.	Program	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	Din
	Program verify	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	Dout
	Optional verify	V _{IL}	V _{IL}	X	V _{PP}	V _{CC}	Dout
	Program inhibit	V _{IH}	V _{IH}	X	V _{PP}	V _{CC}	High-Z
Identifier		V _{IL}	V _{IL}	V _H ^{*2}	V _{SS} – V _{CC}	V _{CC}	Code

- Notes: 1. X: Don't care.
2. V_H: 12.0 V ± 0.5 V

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
All input and output voltages ^{*1}	V _{in} , V _{out}	–0.6 ^{*2} to +7.0	V
Voltage on pin A9 and OE	V _{ID}	–0.6 ^{*2} to +13.0	V
V _{PP} voltage ^{*1}	V _{PP}	–0.6 to +13.5	V
V _{CC} voltage ^{*1}	V _{CC}	–0.6 to +7.0	V
Operating temperature range	T _{opr}	0 to +70	°C
Storage temperature range ^{*3}	T _{stg}	–65 to +125	°C
Storage temperature under bias	T _{bias}	–20 to +80	°C

- Notes: 1. Relative to V_{SS}.
2. V_{in}, V_{out}, V_{ID} min = –2.0 V for pulse width ≤ 20 ns
3. Storage temperature range of device before programming.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C_{in}	—	—	12	pF	$V_{in} = 0\text{ V}$
Output capacitance	C_{out}	—	—	20	pF	$V_{out} = 0\text{ V}$

Read OperationDC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 5.5\text{ V}$
Output leakage current	I_{LO}	—	—	2	μA	$V_{out} = 5.5\text{ V}/0.45\text{ V}$
V_{PP} current	I_{PP1}	—	1	20	μA	$V_{PP} = 5.5\text{ V}$
Standby V_{CC} current	I_{SB}	—	—	30	mA	$CE = V_{IH}$
Operating V_{CC} current	I_{CC1}	—	—	30	mA	$I_{out} = 0\text{ mA}$, $f = 1\text{ MHz}$
	I_{CC2}	—	—	120	mA	$I_{out} = 0\text{ mA}$, $f = 11.8\text{ MHz}$
Input voltage	V_{IL}	-0.3^{*1}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 1^{*2}$	V	
Output voltage	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$

- Notes: 1. V_{IL} min = -1.0 V for pulse width $\leq 50\text{ ns}$
 V_{IL} min = -2.0 V for pulse width $\leq 20\text{ ns}$
 2. V_{IH} max = $V_{CC} + 1.5\text{ V}$ for pulse width $\leq 20\text{ ns}$
 If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

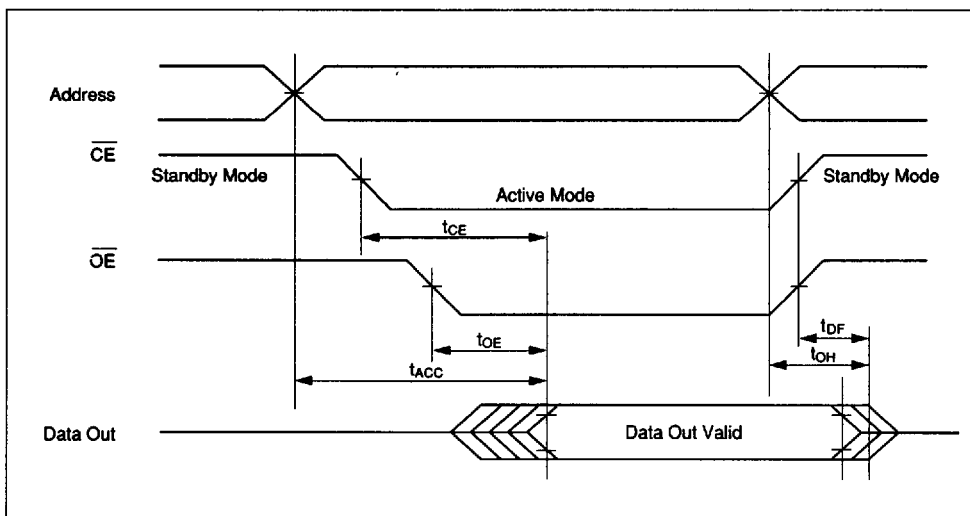
HN27C4096HG/HCC Series**AC Characteristics** ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to $+70^\circ\text{C}$)**Test Conditions**

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 10\text{ ns}$
- Output load: 1 TTL gate + 100 pF
- Reference levels for measuring timing: 1.5 V, 1.5 V

HN27C4096H-85

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	85	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}	—	85	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	—	45	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float *1	t_{DF}	0	30	ns	$\overline{CE} = V_{IL}$
Address to output hold	t_{OH}	5	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform

HN27C4096HG/HCC Series

Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

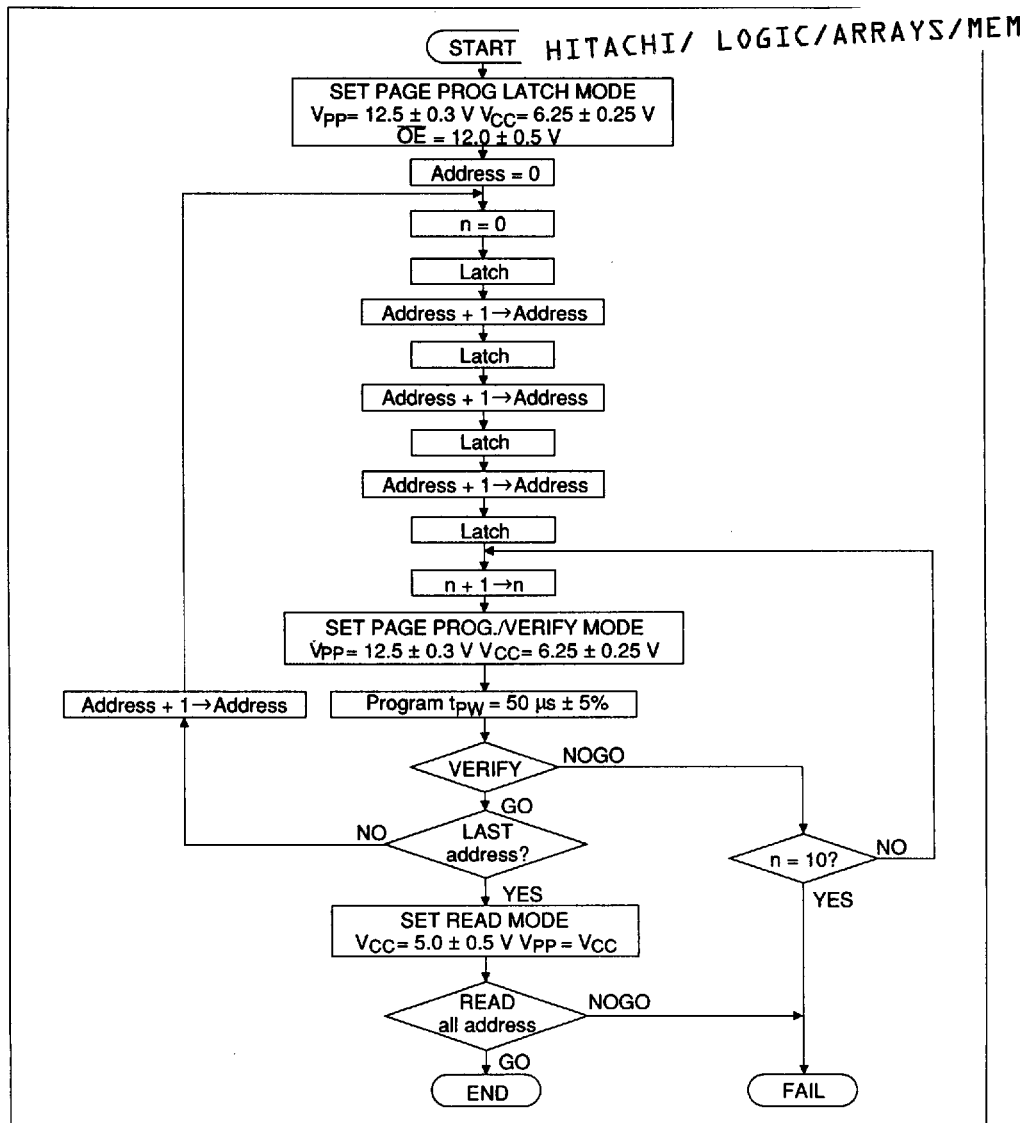
Page Program Set

Apply 12 V to $\overline{OE}$ pin after applying 12.5 V to V_{PP} to set a page program mode.

The device operates in a page program mode until reset.

Page Program Reset

Set V_{PP} to V_{CC} level or less to reset a page program mode.



HN27C4096HG/HCC Series**DC Characteristics** ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
Output voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 2. V_{PP} must not exceed 13.5 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 5. $V_{IL} \text{ min} = -0.6 \text{ V}$ for pulse width $\leq 20 \text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

HN27C4096HG/HCC Series**AC Characteristics** ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)**Test Conditions**

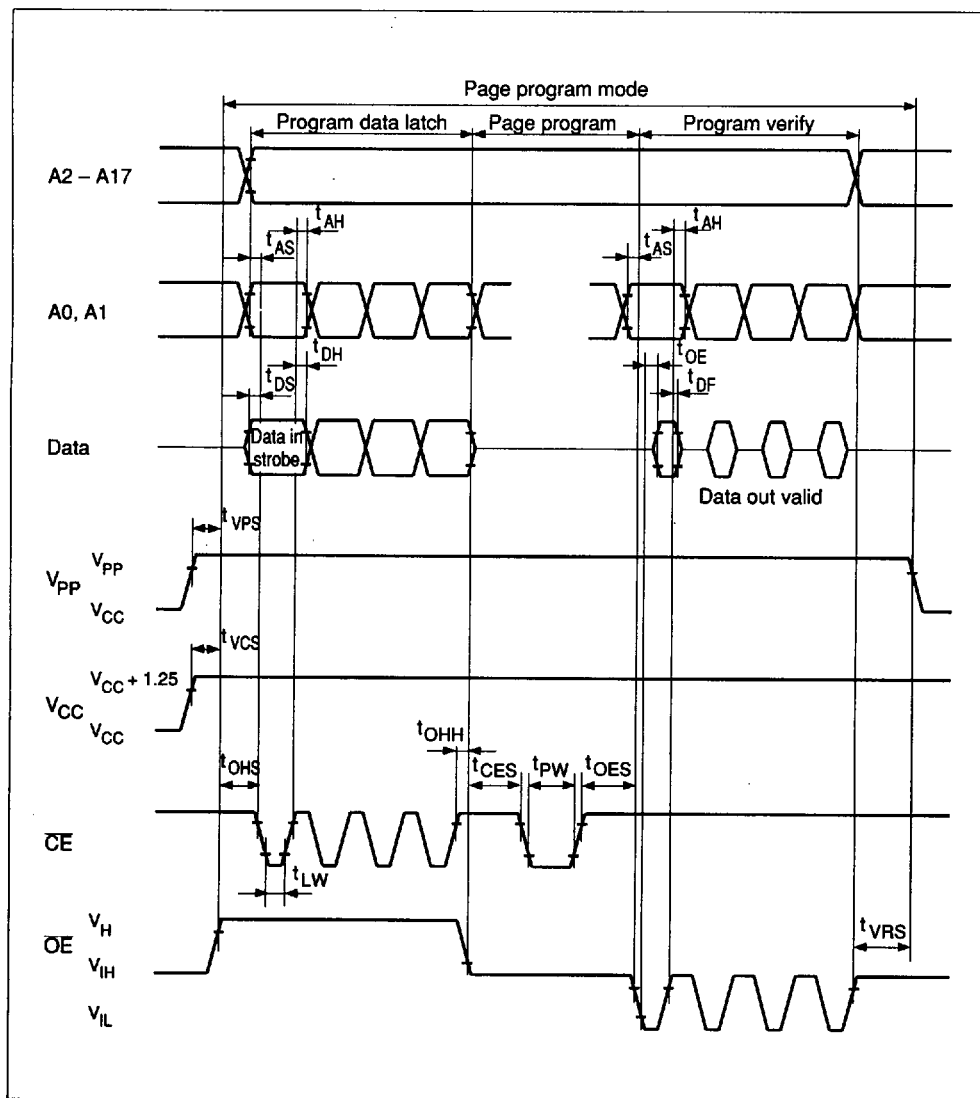
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 20\text{ ns}$

- Reference levels for measuring timing:
Inputs; 0.8 V, 2.0 V
Outputs; 0.8 V, 2.0 V

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Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
OE setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
OE high to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
OE initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
OE setup time	t_{CES}	2	—	—	μs	
Data valid from OE	t_{OE}	0	—	150	ns	
OE pulse width during data latch	t_{LW}	1	—	—	μs	
OE= V_H setup time	t_{OHS}	2	—	—	μs	
OE= V_H hold time	t_{OHH}	2	—	—	μs	
OE hold time	t_{OEH}	2	—	—	μs	
V_{PP} hold time*2	t_{VRS}	1	—	—	μs	

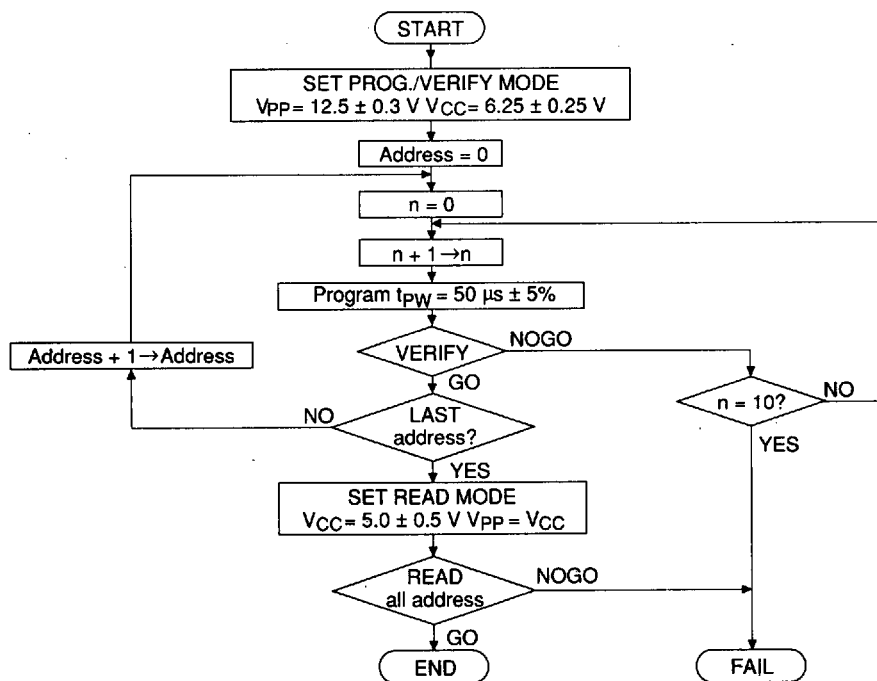
- Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

HN27C4096HG/HCC Series**Fast High-Reliability Page Programming Timing Waveform**

Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster

programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

HN27C4096HG/HCC SeriesDC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE} = V_{IL}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
Output voltage	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$

- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 2. V_{PP} must not exceed 13.5 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 5. V_{IL} min = -0.6 V for pulse width $\leq 20 \text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)**Test Conditions**

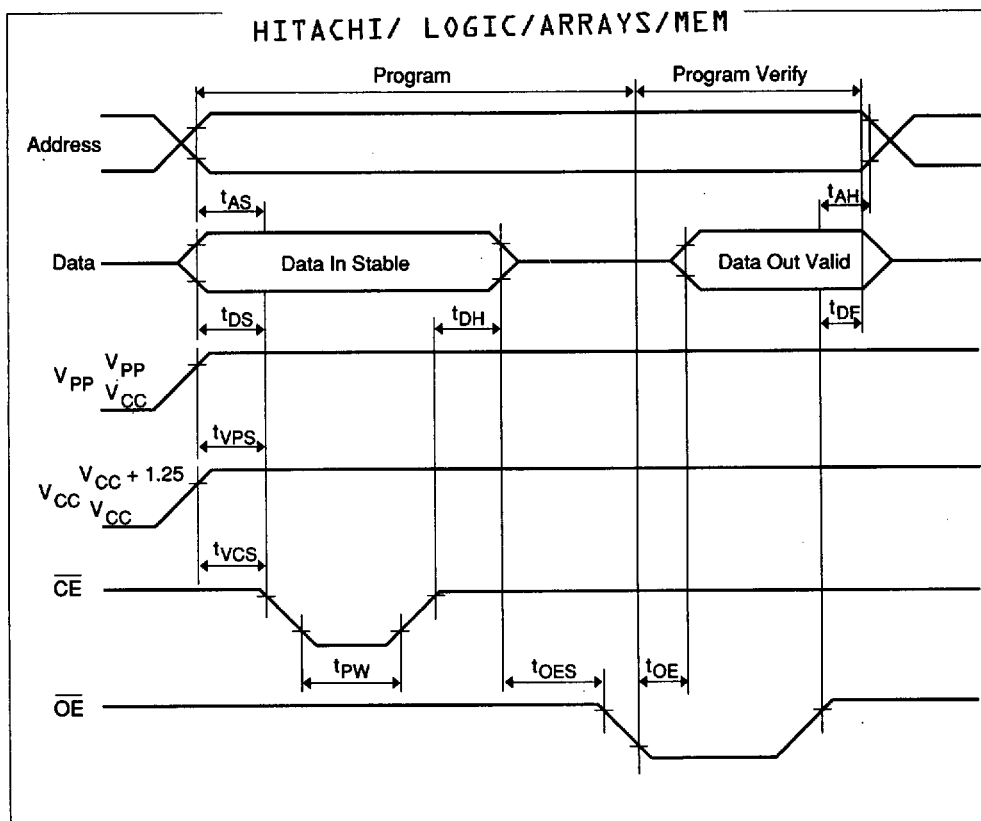
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$

- Reference levels for measuring timings:
0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
OE setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
OE to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{CE}$ initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

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Optional Page Programming

This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

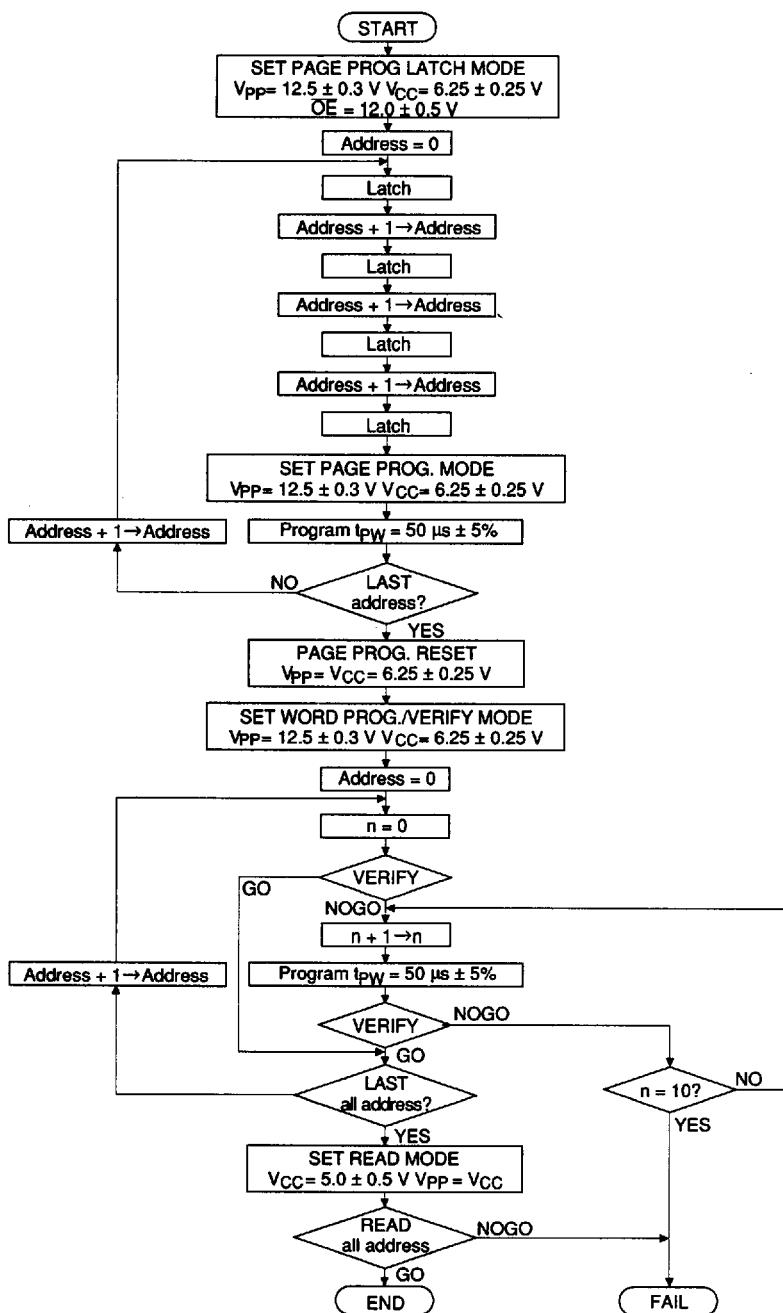
This programming algorithm is the combination of page programming and word verify. It can avoid

the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.

HN27C4096HG/HCC Series

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Optional Page Programming Flowchart

HN27C4096HG/HCC Series**DC Characteristics** ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
Output voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 2. V_{PP} must not exceed 13.5 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 5. $V_{IL} \text{ min} = -0.6 \text{ V}$ for pulse width $\leq 20 \text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

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HN27C4096HG/HCC Series**HITACHI/ LOGIC/ARRAYS/MEM**

AC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 20\text{ ns}$

- Reference levels for measuring timings:

Inputs; 0.8 V, 2.0 V

Outputs; 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
$\overline{\text{OE}}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
$\overline{\text{OE}}$ high to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{\text{CE}}$ initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
$\overline{\text{CE}}$ setup time	t_{CES}	2	—	—	μs	
Data valid from $\overline{\text{OE}}$	t_{OE}	0	—	150	ns	
$\overline{\text{CE}}$ pulse width during data latch	t_{LW}	1	—	—	μs	
$\text{OE} = V_H$ setup time	t_{OHS}	2	—	—	μs	
$\text{OE} = V_H$ hold time	t_{OHH}	2	—	—	μs	
Page programming reset time *2	t_{VLW}	1	—	—	μs	
V_{PP} hold time *2	t_{VRS}	1	—	—	μs	

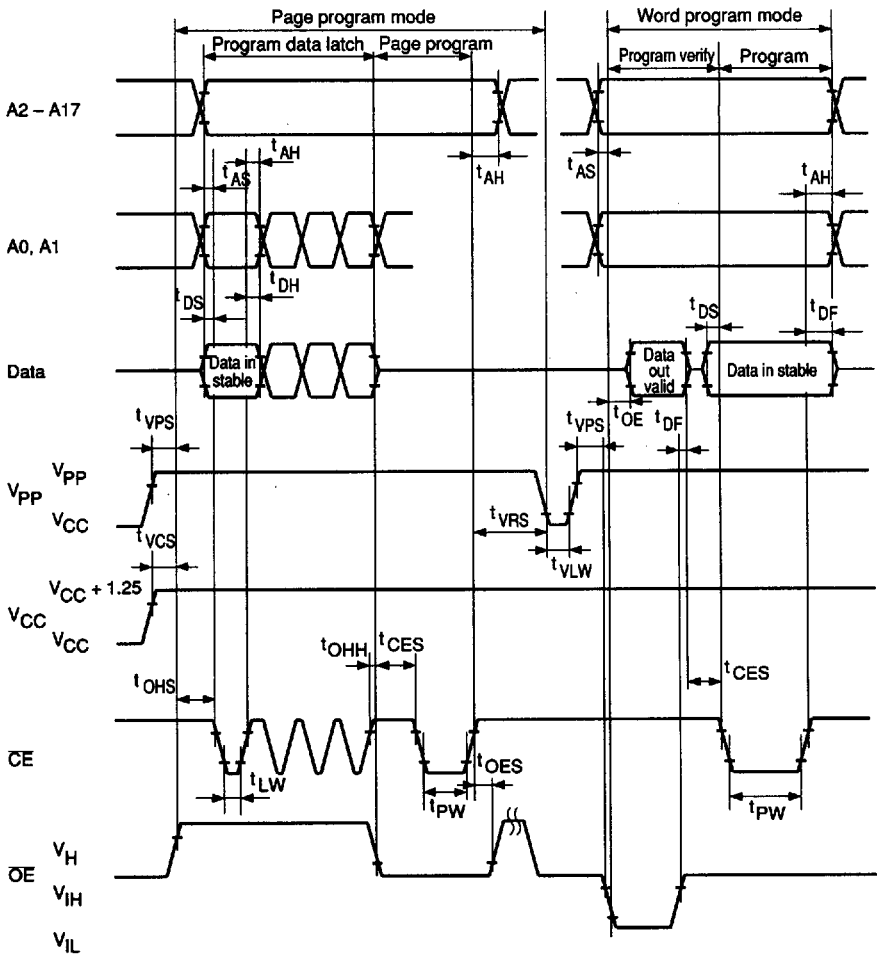
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

HN27C4096HG/HCC Series

Option Page Programming Timing Waveform

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HN27C4096HG/HCC Series**Erase**

Erasure of HN27C4096G/CC is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W•sec/cm².

Mode Description**Device Identifier Mode**

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C4096 Identifier Code

	A0	I/O8 – I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
CC	(24)	(11) – (4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	
Identifier G	(21)	(10) – (3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	Hex Data
Manufacturer code	V _{IL}	×	0	0	0	0	0	1	1	1	07
Device code	V _{IH}	×	1	0	1	0	0	0	1	0	A2

- Notes: 1. V_{CC} = 5.0 V ± 10%
 2. A9 = 12.0 V ± 0.5 V
 3. A1 – A8, A10 – A17, $\overline{\text{CE}}$, $\overline{\text{OE}}$ = V_{IL}
 4. ×: Don't care.

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