

N-Channel Super Trench Power MOSFET

(Primary Version)

Description

The HMS50N10DA uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

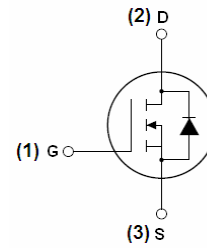
- $V_{DS} = 100V, I_D = 50A$
 $R_{DS(on)} < 10m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} < 13m\Omega @ V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

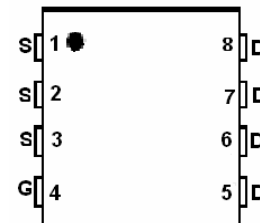
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



DFN5X6-8L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HMS50N10DA	HMS50N10DA	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Package Limited)	I_D	50	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D (100^\circ C)$	35	A
Pulsed Drain Current	I_{DM}	150	A
Maximum Power Dissipation	P_D	105	W
Derating factor		0.7	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	210	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.4	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

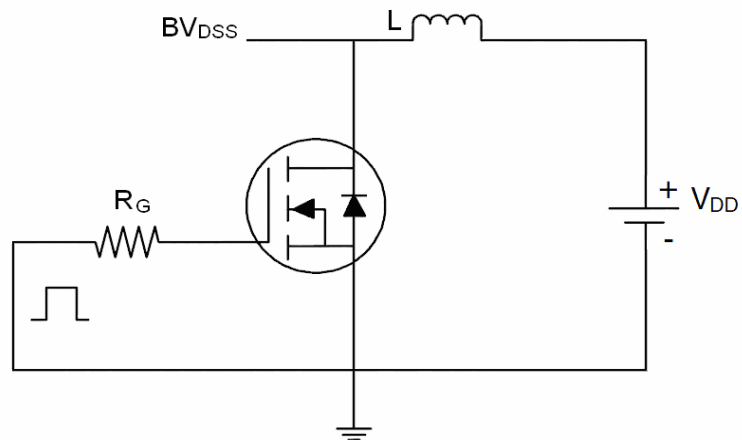
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	8.3	10	mΩ
		V _{GS} =4.5V, I _D =30A	-	10	13	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =30A	40	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	3500	-	PF
Output Capacitance	C _{oss}		-	600	-	PF
Reverse Transfer Capacitance	C _{rss}		-	29	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =30A V _{GS} =10V, R _G =4.7Ω	-	12	-	nS
Turn-on Rise Time	t _r		-	45	-	nS
Turn-Off Delay Time	t _{d(off)}		-	31	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =30A, V _{GS} =10V	-	48		nC
Gate-Source Charge	Q _{gs}		-	15		nC
Gate-Drain Charge	Q _{gd}		-	8		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =50A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	50	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-	55		nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	93		nC

Notes:

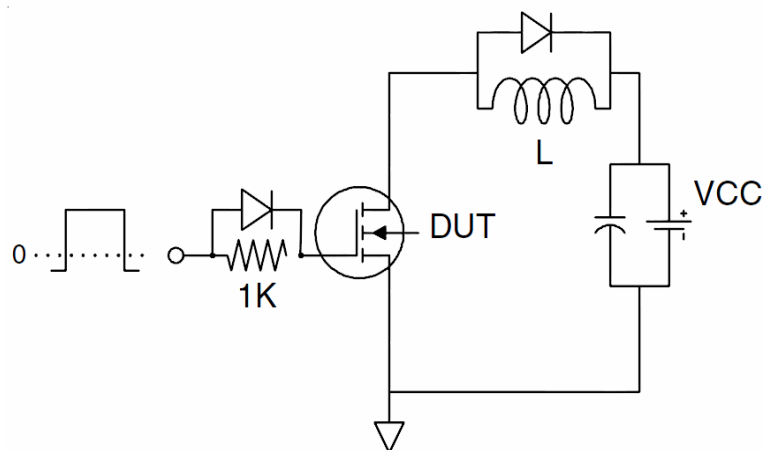
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

Test Circuit

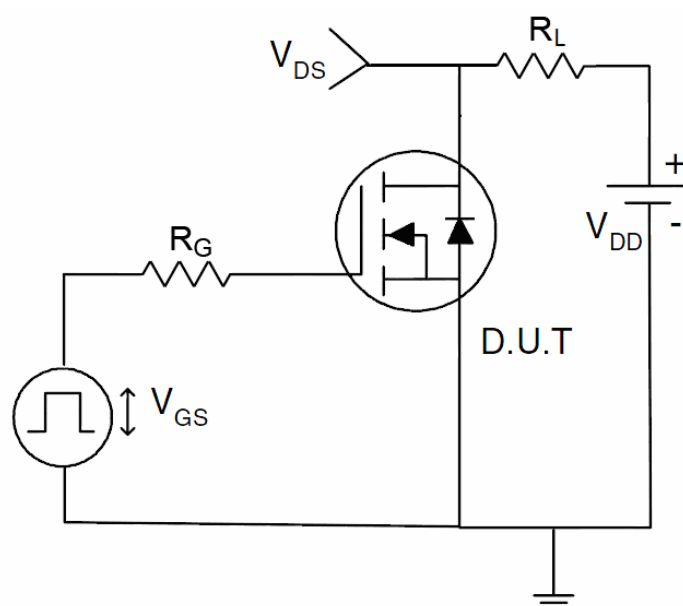
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

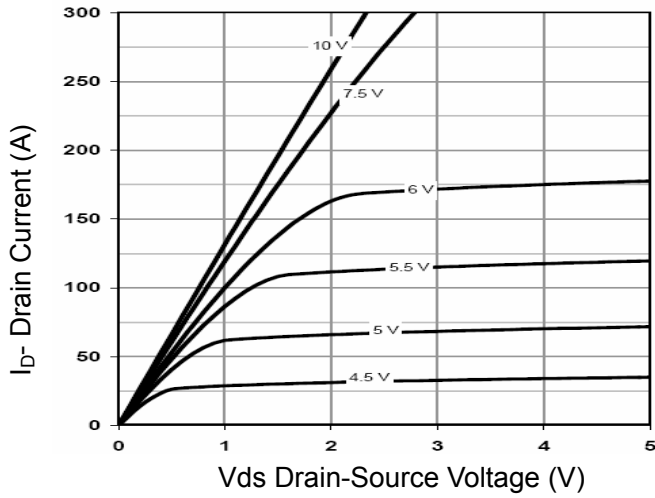


Figure 1 Output Characteristics

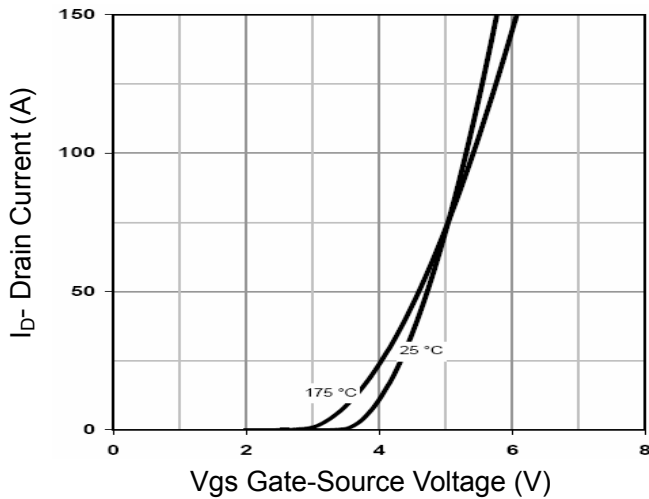


Figure 2 Transfer Characteristics

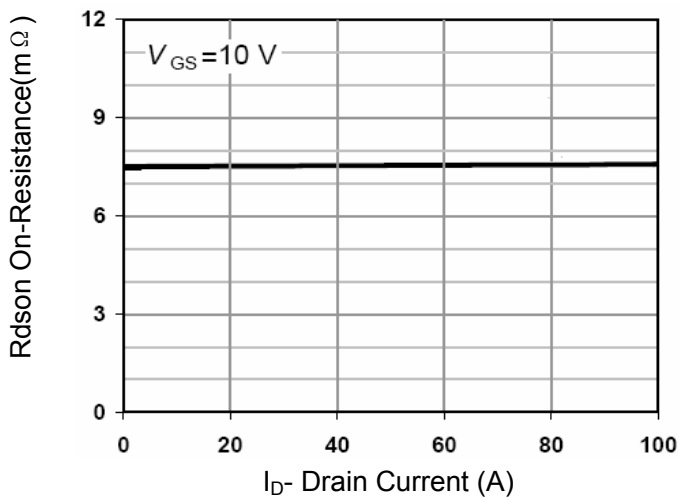


Figure 3 $R_{DS(on)}$ - Drain Current

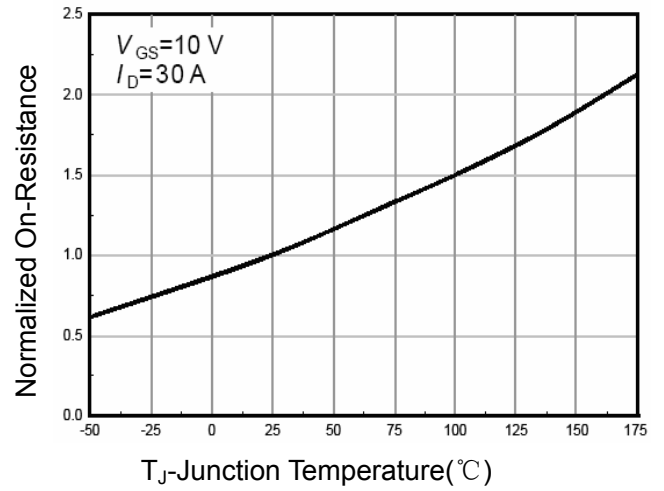


Figure 4 $R_{DS(on)}$ -Junction Temperature

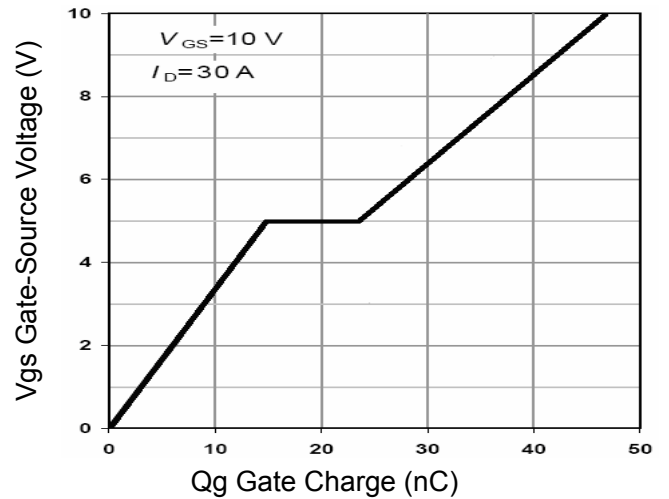


Figure 5 Gate Charge

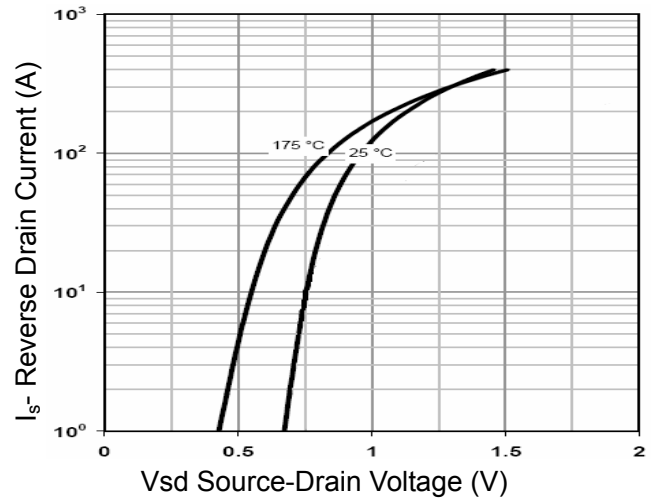


Figure 6 Source- Drain Diode Forward

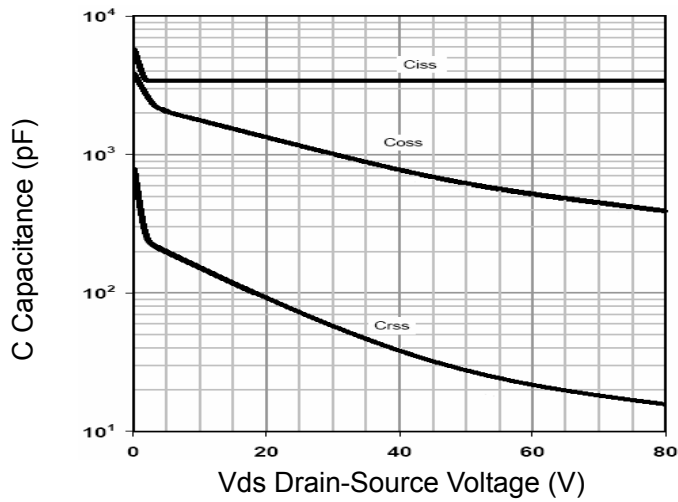


Figure 7 Capacitance vs Vds

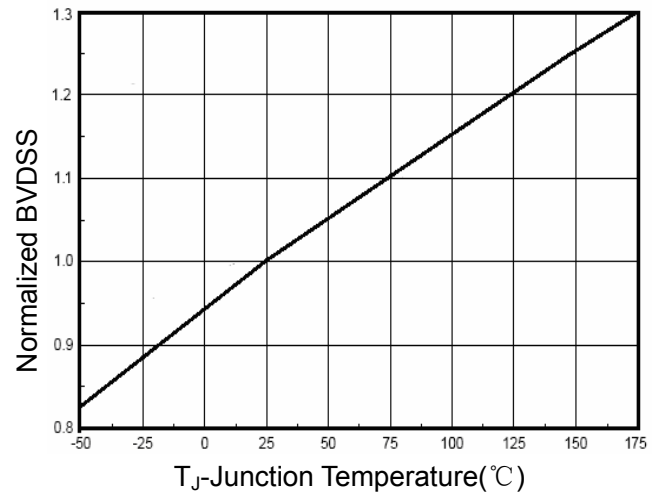


Figure 9 BV_{DSS} vs Junction Temperature

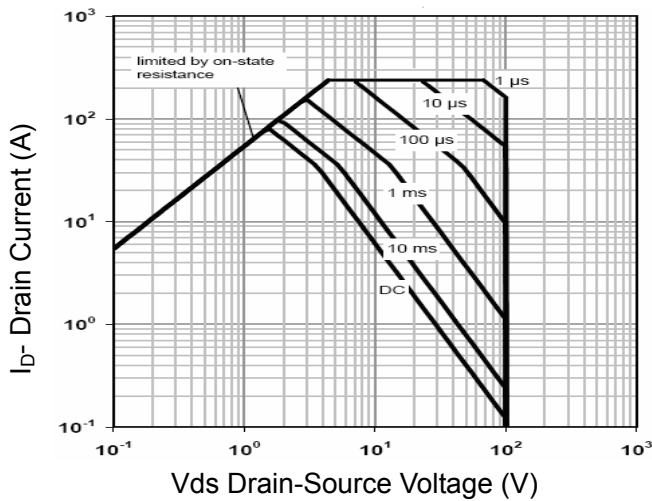


Figure 8 Safe Operation Area

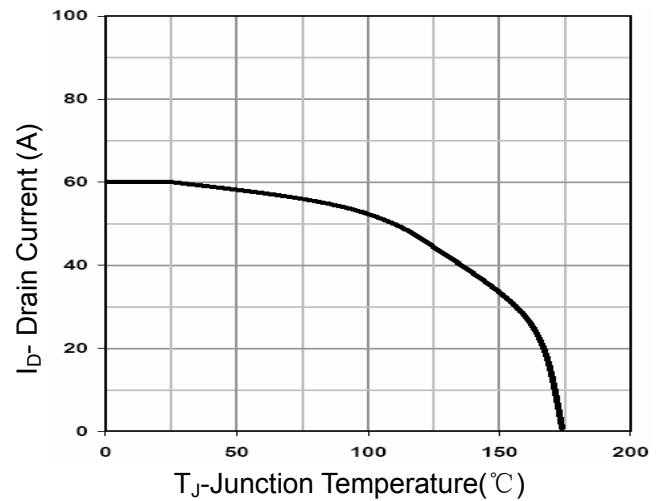


Figure 10 Current De-rating

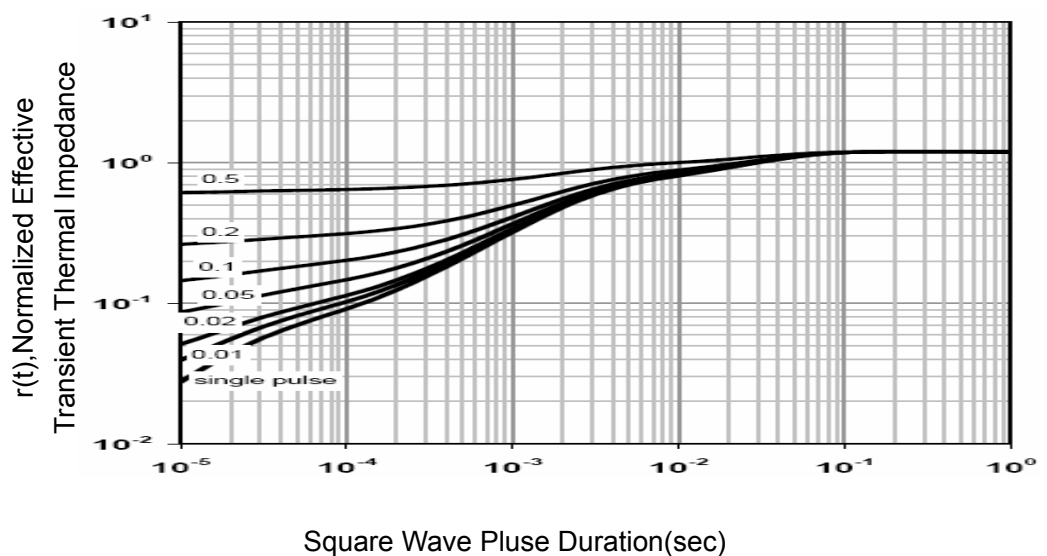
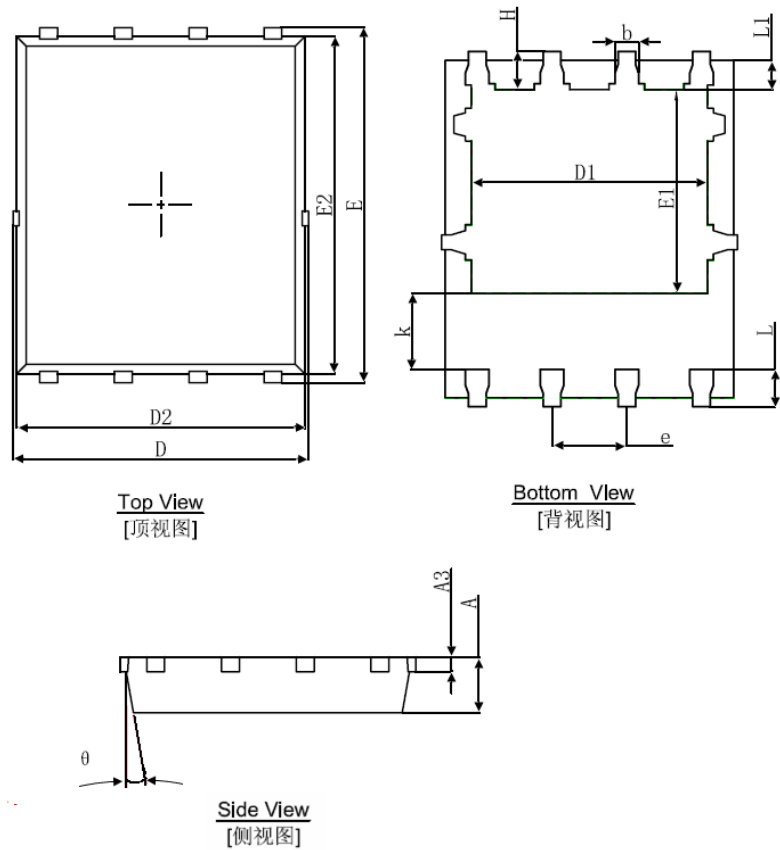


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°		8°	