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HMS3N70R2

700V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)}$ X Q_g)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

Application

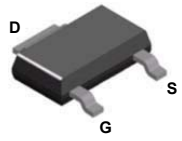
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV Power & LED Lighting Power

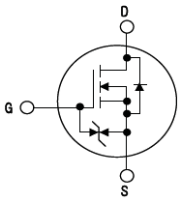
Key Parameters

Parameter	Value	Unit
BV_{DSS} @$T_{j,max}$	750	V
I_D	3	A
$R_{DS(on),\ max}$	1.5	Ω
$Qg_{,\ Typ}$	5.5	nC

Package & Internal Circuit

SOT-223-2L





Absolute Maximum Ratings

T_J=25℃ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	700	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current – Continuous (T_C = 25℃)	3.0 *	A
	Drain Current – Continuous (T_C = 100℃)	2.1 *	A
I_{DM}	Drain Current – Pulsed (Note 1)	9.0 *	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	43	mJ
dv/dt	MOSFET dv/dt ruggedness, V_{DS}=0…560V	50	V/ns
dv/dt	Reverse diode dv/dt, V_{DS}=0…560V, I_{DS}≤I_D	15	V/ns
P_D	Power Dissipation (T_C = 25℃)	5	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2500	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JS}$	Junction-to-Solder point	--	25	℃/W
$R_{\theta JA}$	Junction-to-Ambient	--	60	

Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 60 μA	2.5	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.1 A	--	--	1.5	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	700	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 700 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 700 V, T_J = 150℃	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	--	--	±1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1.0 MHz	--	245	--	pF
C_{oss}	Output Capacitance		--	13	--	pF
C_{rss}	Reverse Transfer Capacitance		--	1.7	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 350 V, I_D = 1.5 A, R_G = 25 Ω	--	20	--	ns
t_r	Turn-On Rise Time		--	18	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	50	--	ns
t_f	Turn-Off Fall Time		--	20	--	ns
Q_g	Total Gate Charge	V_{DS} = 560 V, I_D = 1.5 A V_{GS} = 10 V	--	5.5	--	nC
Q_{gs}	Gate-Source Charge		--	1.1	--	nC
Q_{gd}	Gate-Drain Charge		--	2.2	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	3.0	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	9.0	
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 3.0 A, V_{GS} = 0 V	--	--	1.3	V
trr	Reverse Recovery Time	I_S = 1.5 A, V_{GS} = 0 V di_F/dt = 100 A/μs	--	135	--	ns
Qrr	Reverse Recovery Charge		--	0.6	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=1A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

Typical Characteristics

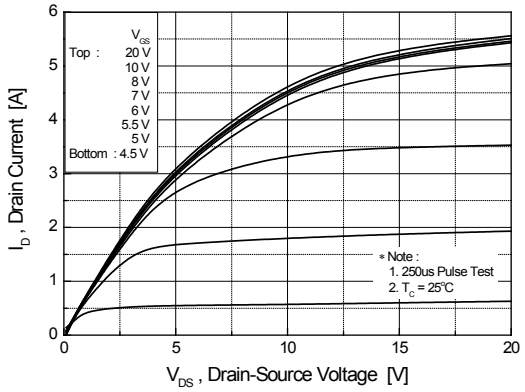


Figure 1. On Region Characteristics

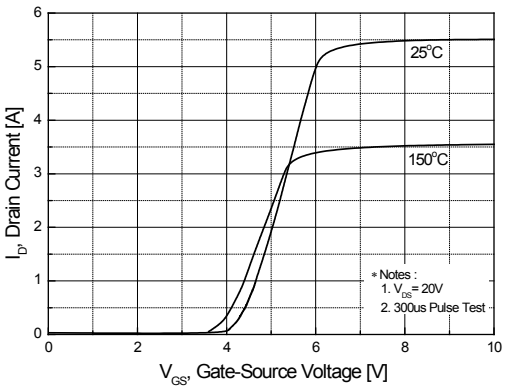


Figure 2. Transfer Characteristics

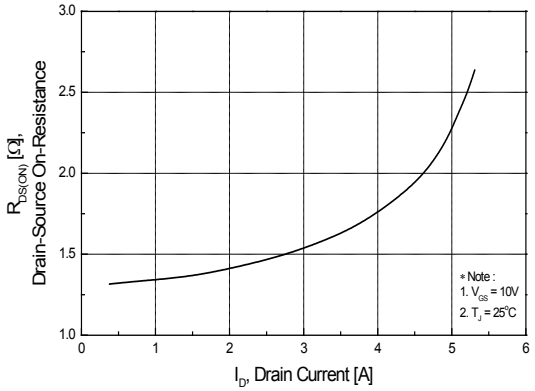


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

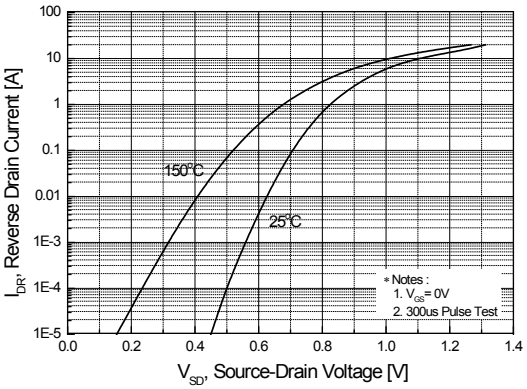


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

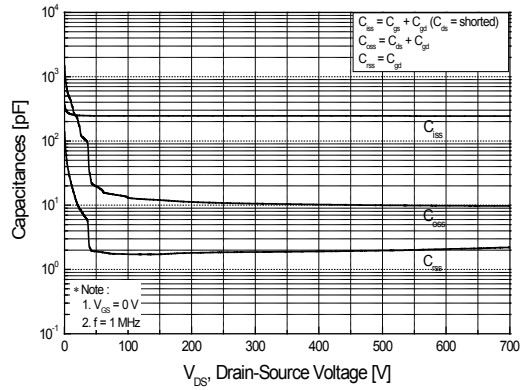


Figure 5. Capacitance Characteristics

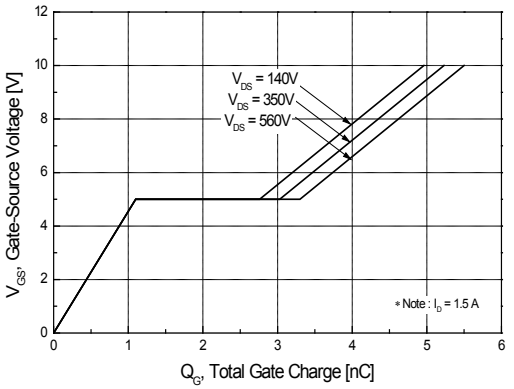


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

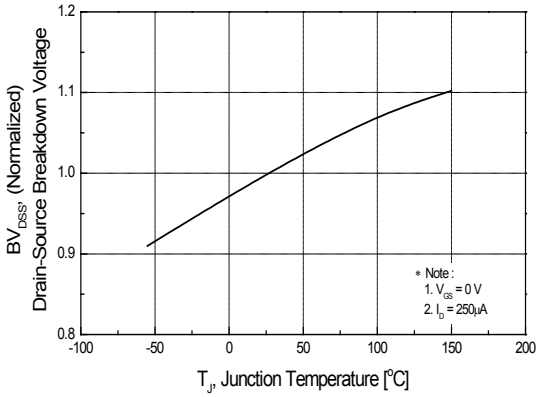


Figure 7. Breakdown Voltage Variation vs Temperature

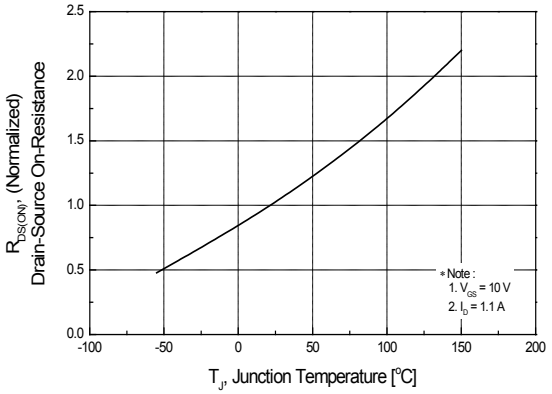


Figure 8. On-Resistance Variation vs Temperature

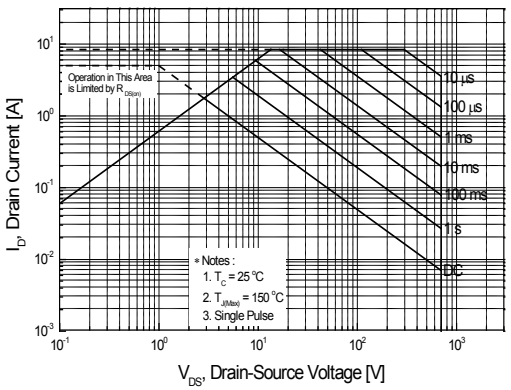


Figure 9. Maximum Safe Operating Area

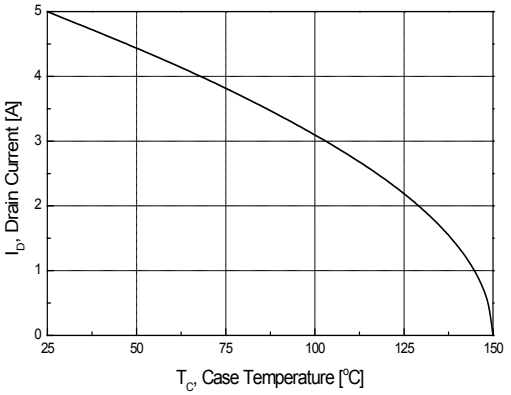


Figure 10. Maximum Drain Current vs Case Temperature

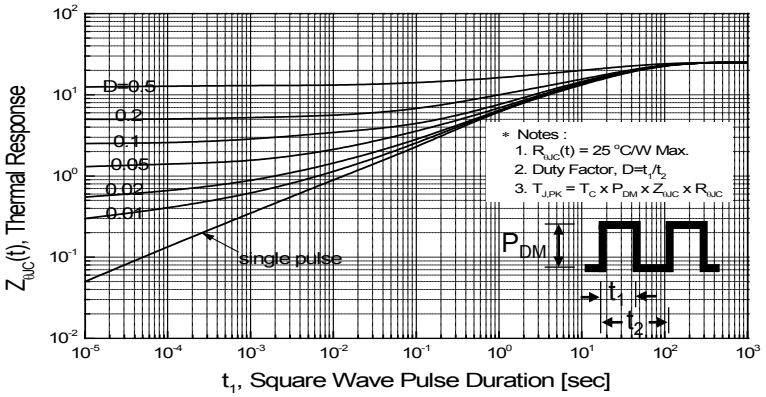


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

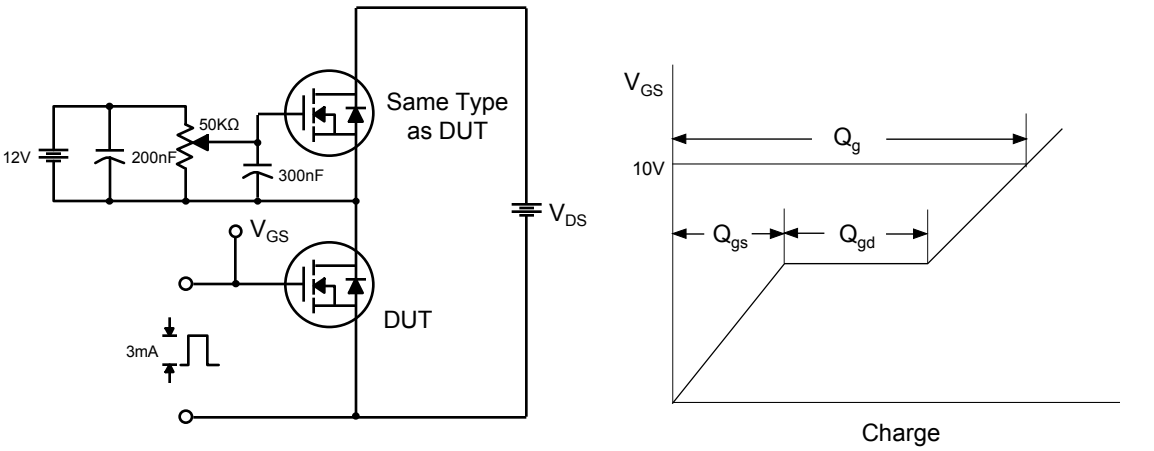


Fig 13. Resistive Switching Test Circuit & Waveforms

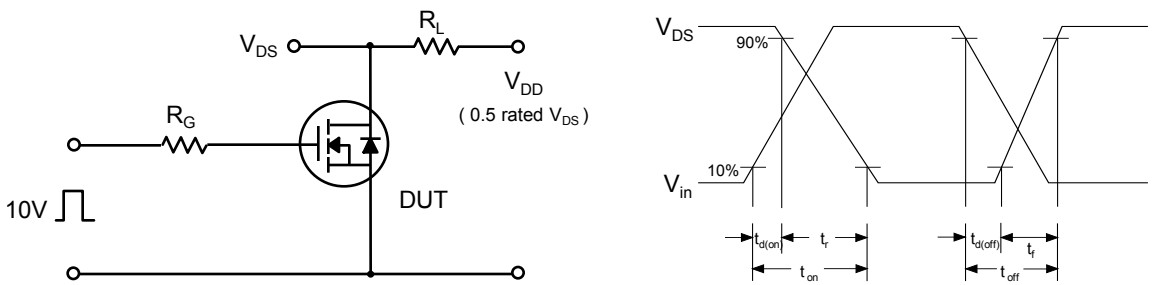


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

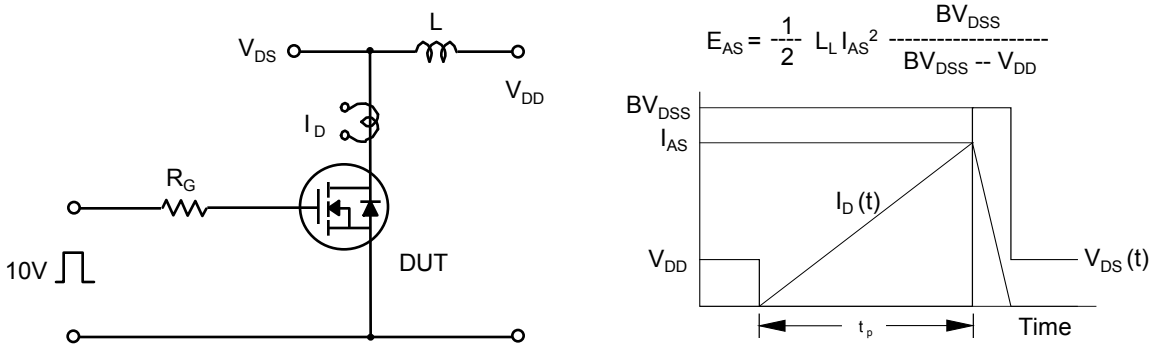
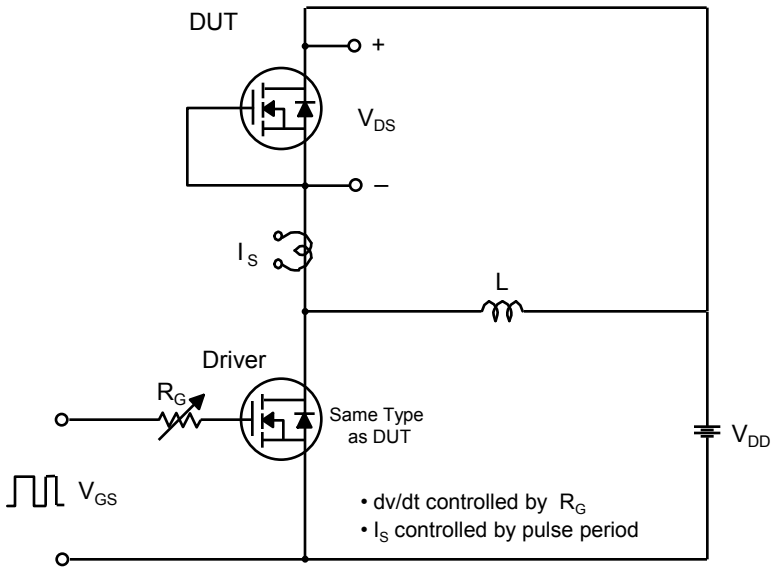
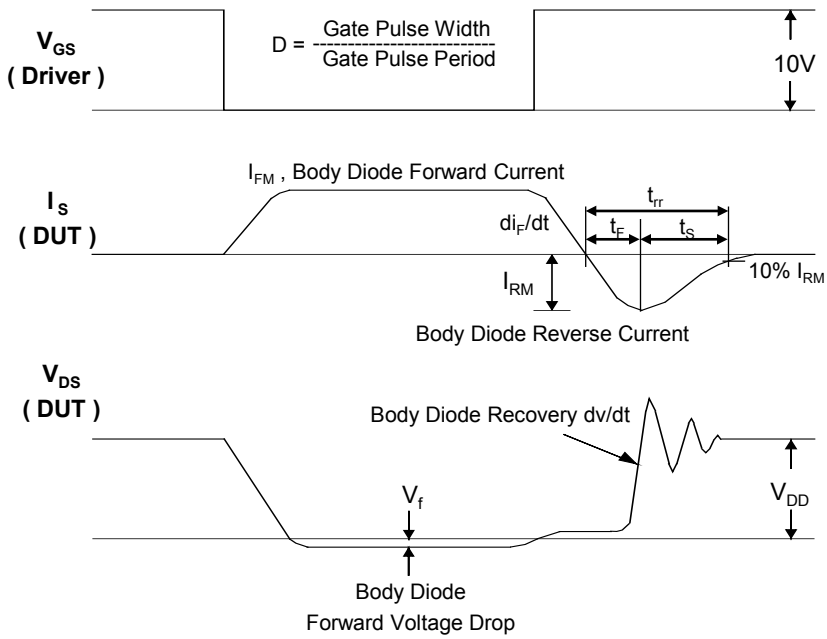


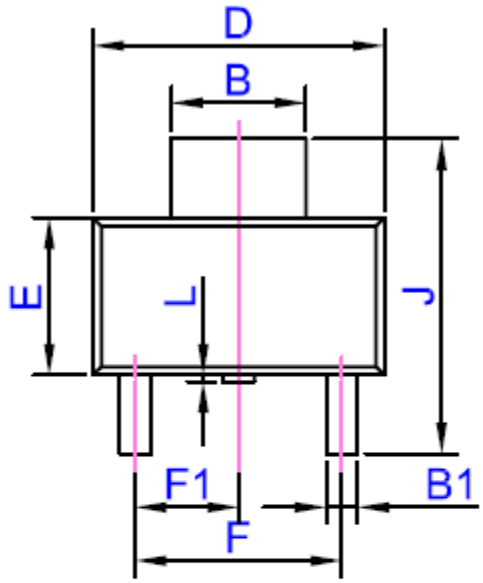
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

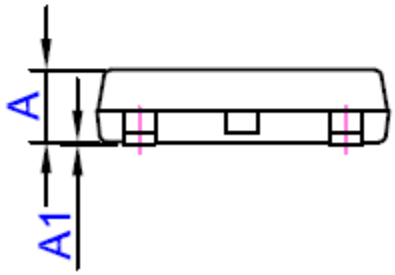


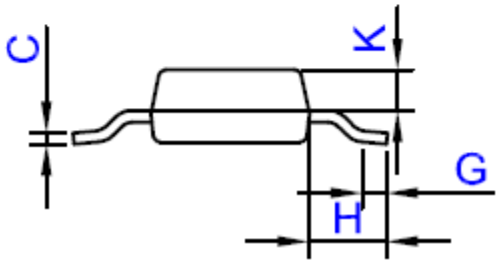


Package Dimension

SOT-223-2L







Ref	Dimensions					
	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.5	1.6	1.8	0.059	0.063	0.071
A1	0.01	0.06	0.10	0.001	0.002	0.004
B	2.9	3.0	3.1	0.114	0.118	0.122
B1	0.6	0.7	0.8	0.024	0.028	0.031
C	0.22	0.254	0.32	0.009	0.010	0.013
D	6.3	6.5	6.7	0.248	0.256	0.264
E	3.3	3.5	3.7	0.130	0.138	0.146
F		4.6			0.181	
F1		2.3			0.091	
G	0.7	0.9	1.1	0.028	0.035	0.043
H	1.5	1.75	2.0	0.059	0.069	0.079
J	6.7	7.0	7.3	0.264	0.276	0.287
K		0.9			0.035	
L	0	0.1	0.2	0	0.004	0.008