

N-Channel Super Junction Power MOSFET

General Description

The series of devices use advanced super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

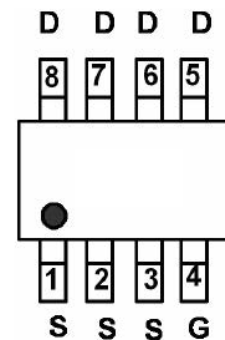
Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)

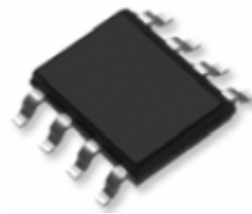
V_{DS}	650	V
$R_{DS(ON) MAX}$	12	Ω
I_D	1	A



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
HMSN65S	SOP8	HMSN65S



SOP-8 top view

Table 1. Absolute Maximum Ratings ($T_c=25^\circ\text{C}$)

Parameter	Symbol	HMS15N65	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	650	V
Gate-Source Voltage ($V_{DS}=0V$)	V_{GS}	± 30	V
Continuous Drain Current at $T_c=25^\circ\text{C}$	$I_{D(DC)}$	1	A
Continuous Drain Current at $T_c=100^\circ\text{C}$	$I_{D(DC)}$	0.7	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	3	A
Maximum Power Dissipation($T_c=25^\circ\text{C}$)	P_D	145	W
Derate above 25°C		1.6	W/ $^\circ\text{C}$
Single pulse avalanche energy (Note 2)	E_{AS}	690	mJ
Avalanche current (Note 1)	I_{AR}	7	A
Repetitive Avalanche energy, t_{AR} limited by T_{jmax} (Note 1)	E_{AR}	1	mJ

Parameter	Symbol	HMS15N65A	Unit
Drain Source voltage slope, $V_{DS} \leq 480V$,	dv/dt	50	V/ns
Reverse diode dv/dt, $V_{DS} \leq 480V, I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+150	°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	HMS15N65A	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	0.62	°C /W
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62.5	°C /W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V		0.05	1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V			100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±30V,V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2.0		4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10.5A			12	Ω
Dynamic Characteristics						
Forward Transconductance	g _{FS}	V _{DS} = 20V, I _D = 10.5A		17.5		S
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V, F=1.0MHz		1950		PF
Output Capacitance	C _{oss}			150		PF
Reverse Transfer Capacitance	C _{rss}			5		PF
Total Gate Charge	Q _g	V _{DS} =480V,I _D =1A, V _{GS} =10V		45	70	nC
Gate-Source Charge	Q _{gs}			9		nC
Gate-Drain Charge	Q _{gd}			18		nC
Intrinsic gate resistance	R _G	f = 1 MHz open drain		1		Ω
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =380V,I _D =11A, R _G =4Ω,V _{GS} =10V		11		nS
Turn-on Rise Time	t _r			6		nS
Turn-Off Delay Time	t _{d(off)}			61	100	nS
Turn-Off Fall Time	t _f			4.5	12	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _C =25℃			1	A
Pulsed Source-drain current(Body Diode)	I _{SDM}				3	A
Forward on voltage	V _{SD}	Tj=25℃,I _{SD} =1A,V _{GS} =0V		0.9	1.3	V
Reverse Recovery Time	t _{rr}	Tj=25℃,I _F =1A,di/dt=100A/μs		310		nS
Reverse Recovery Charge	Q _{rr}			5		uC
Peak Reverse Recovery Current	I _{rrm}			1		A

Notes 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

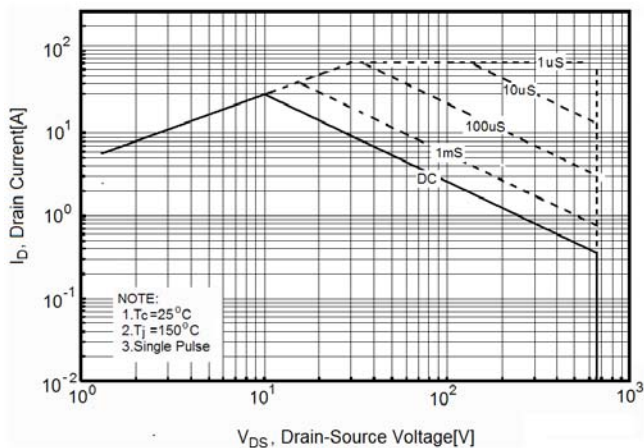


Figure3. Source-Drain Diode Forward Voltage

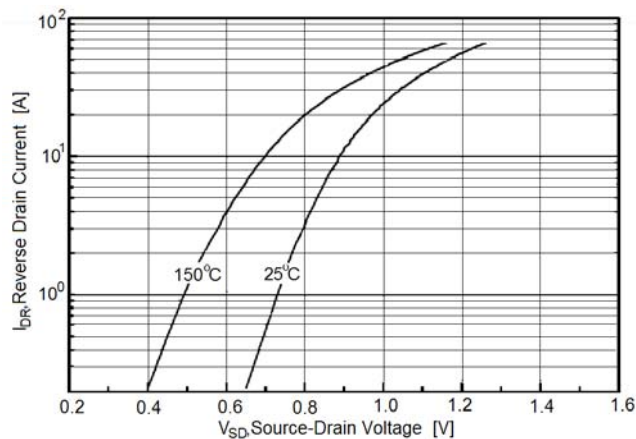


Figure4. Output characteristics

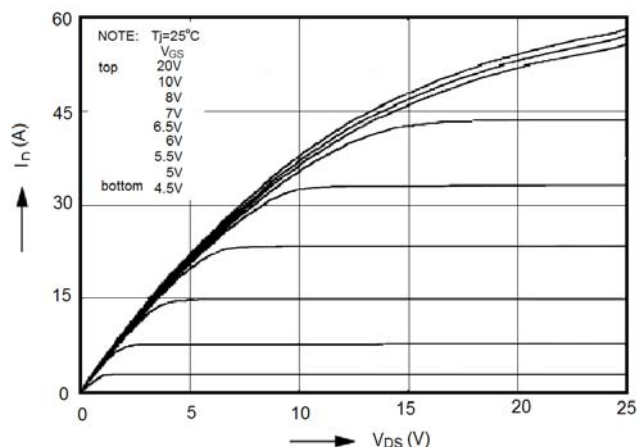


Figure5. Transfer characteristics

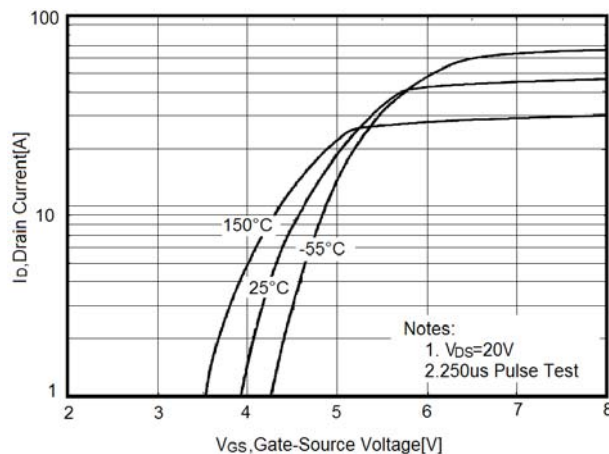


Figure6. Static drain-source on resistance

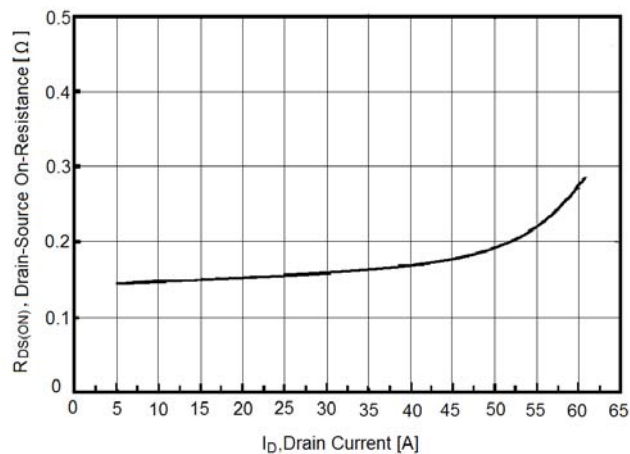


Figure7. $R_{DS(ON)}$ vs Junction Temperature

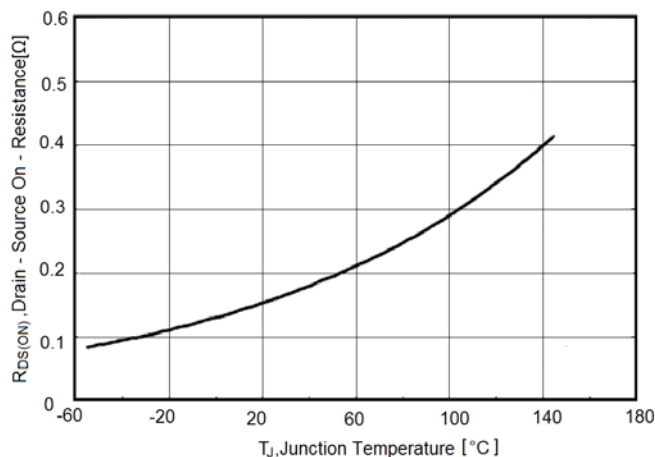


Figure8. BV_{DSS} vs Junction Temperature

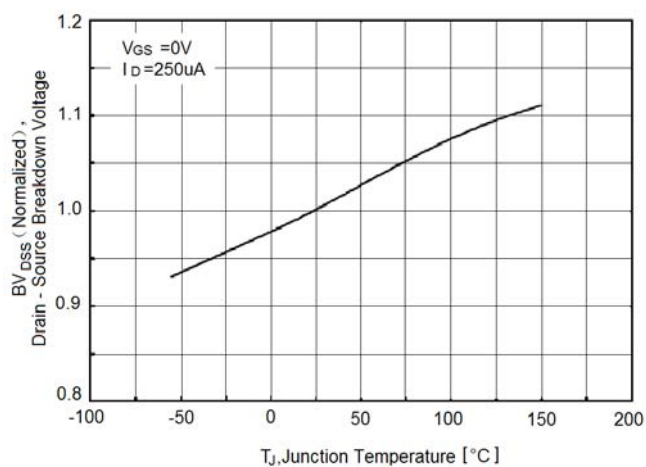


Figure9. Maximum I_D vs Junction Temperature

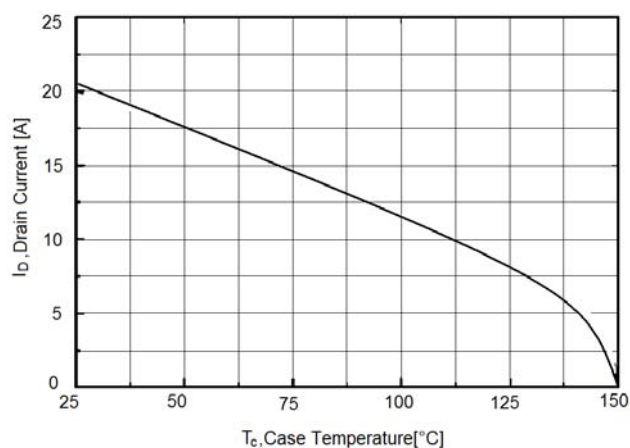


Figure10. Gate charge waveforms

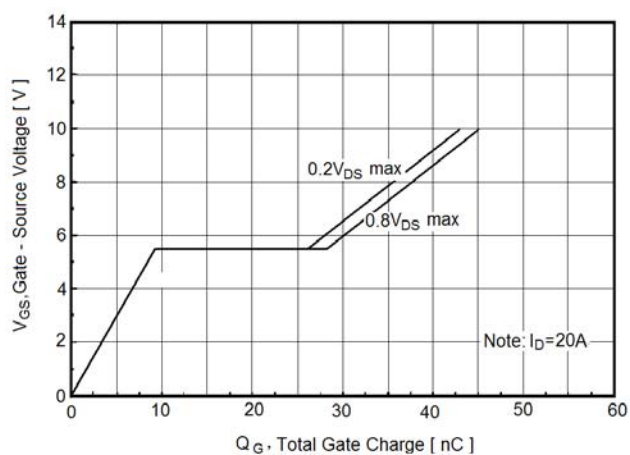


Figure11. Capacitance

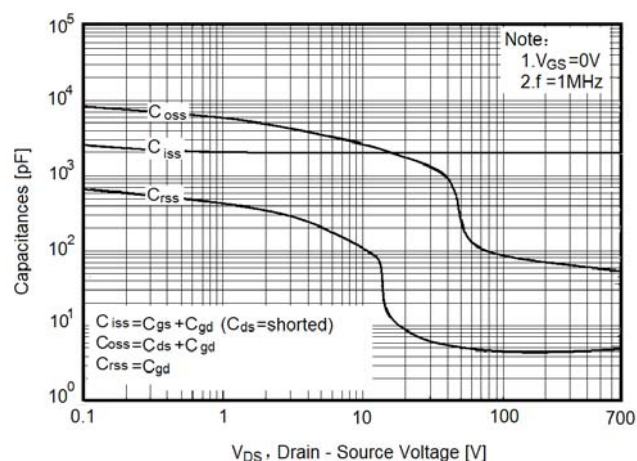
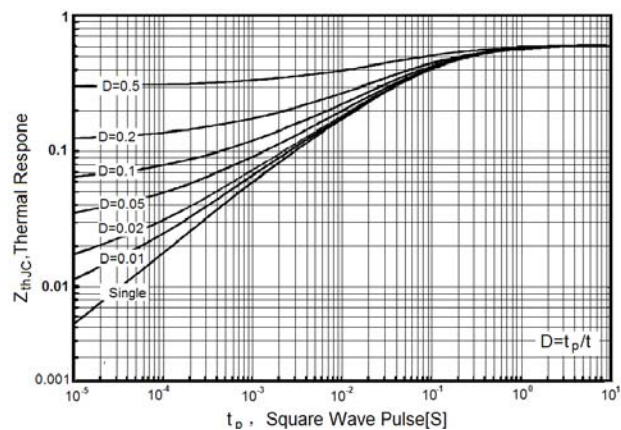
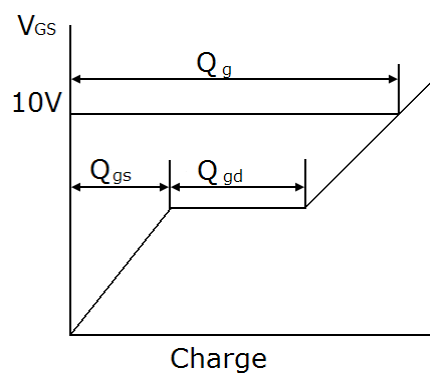
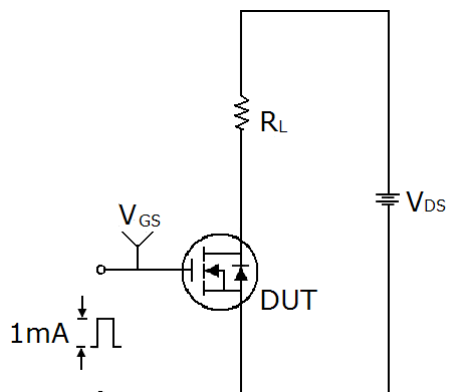


Figure12. Transient Thermal Impedance

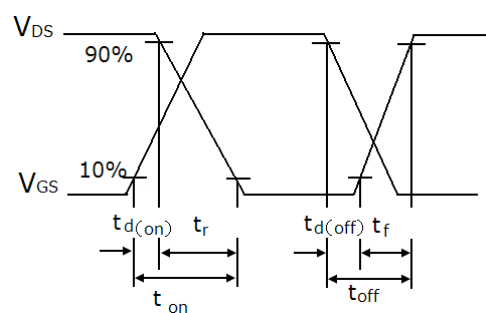
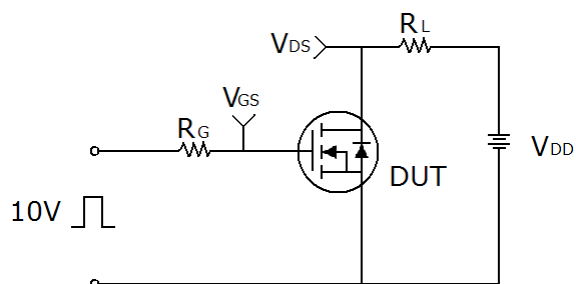


Test circuit

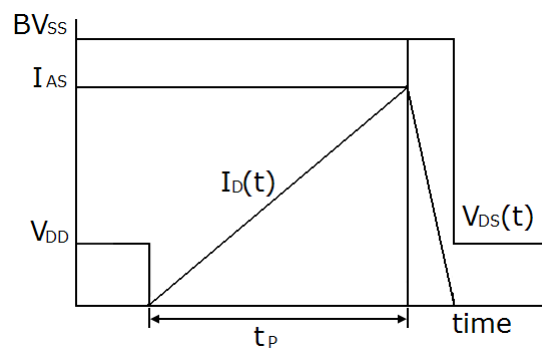
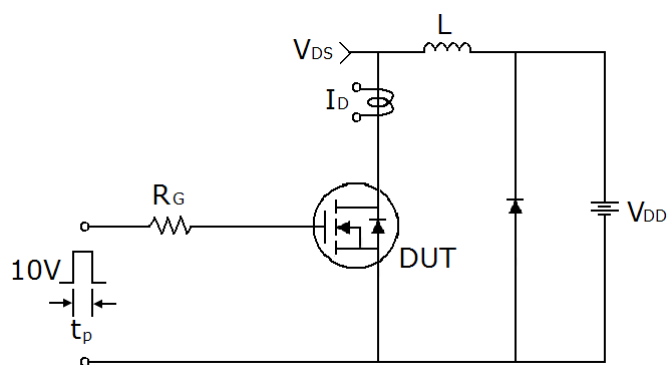
1) Gate charge test circuit & Waveform



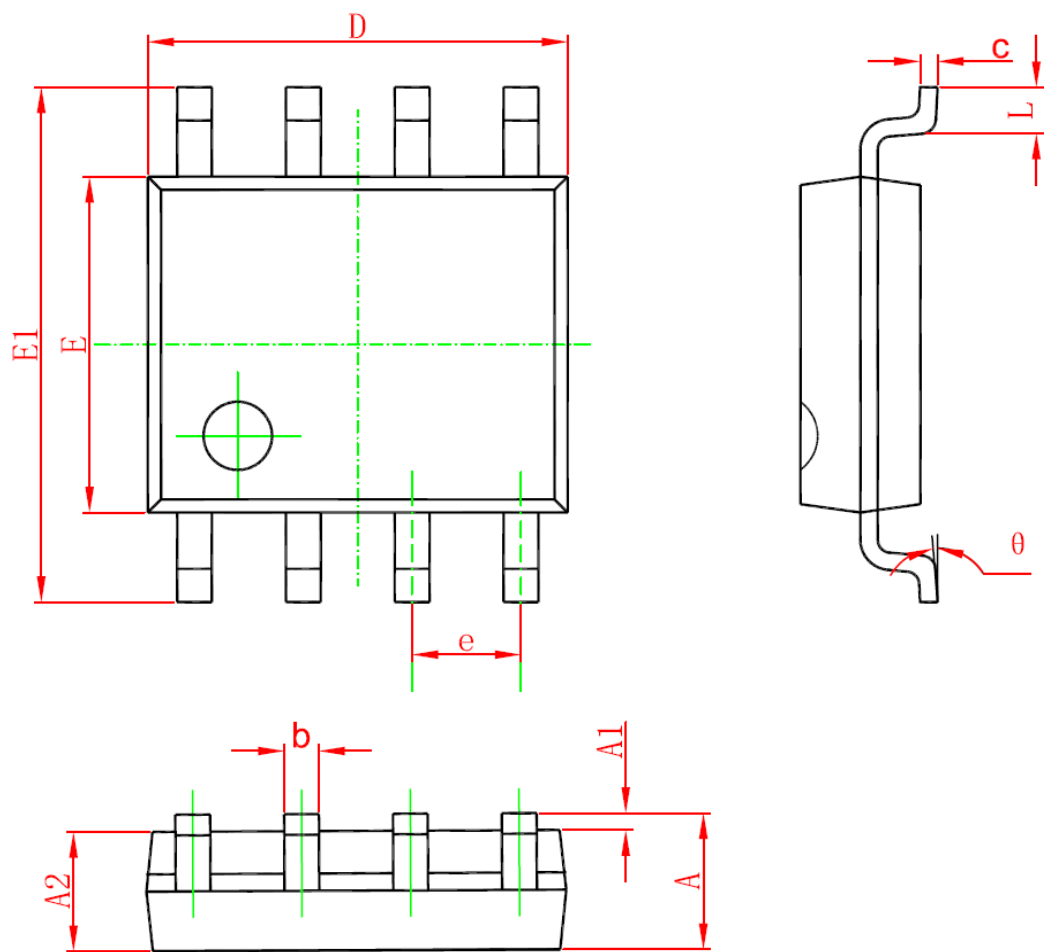
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms



SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°