

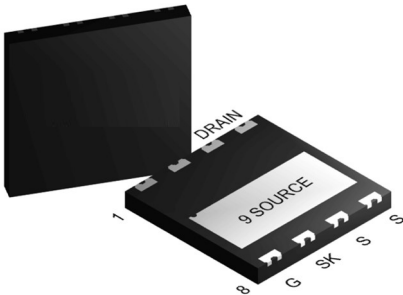
HMN10N65D

General description

650V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead Package (DFN) with 8 mm × 8 mm size

Features

- Enhancement-mode transistor - normally-OFF power switch
- Ultra-high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High-density power conversion
- High-efficiency power conversion

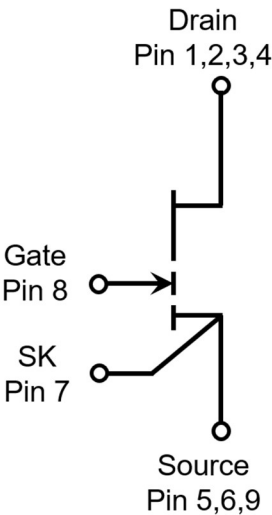


Table 1 Key Performance Parameters at T_J = 25 °C

Parameters	Values	Units
V _{DS, max}	650	V
R _{DS(on), max}	200	mΩ
Q _{G, typ}	2.3	nC
I _{DS, Pulse}	18	A
Q _{OSS @ 400 V}	22	nC
Q _{rr}	0	nC

Gate	8
Drain	1, 2, 3, 4
Kelvin Source	7
Source	5, 6, 9

Table 2 Ordering Information

Type/Ordering Code	Package	Marking
HMN10N65D	DFN 8x8, 2500 pcs/reel	HMN10N65D YXWX

1 Maximum ratings

at $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum rating

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, \max}$	-	-	650	V	$V_{GS} = 0\text{ V}$, $I_D = 10\text{ }\mu\text{A}$
Drain-source voltage transient ¹	$V_{DS, \text{transient}}$	-	-	750	V	$V_{GS} = 0\text{ V}$, $V_{DS} = 750\text{ V}$
Continuous current, drain-source	I_D	-	-	10	A	$T_c = 25\text{ }^{\circ}\text{C}$
Pulsed current, drain-source ²	$I_{D, \text{pulse}}$	-	-	18	A	$T_c = 25\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$
Pulsed current, drain-source ²	$I_{D, \text{pulse}}$	-	-	10	A	$T_c = 125\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$
Gate-source voltage, continuous ³	V_{GS}	-1.4	-	+7	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Gate-source voltage, pulsed	$V_{GS, \text{pulse}}$	-	-	+10	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $t_{\text{Pulse}} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	-	-	75	W	$T_c = 25\text{ }^{\circ}\text{C}$
Operating temperature	T_j	-55	-	+150	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	-55	-	+150	$^{\circ}\text{C}$	

1. $V_{DS, \text{transient}}$ is intended for surge rating during non-repetitive events, $t_{\text{Pulse}} < 1\text{ }\mu\text{s}$.

2. Pulse width = $10\text{ }\mu\text{s}$.

3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1.65	$^{\circ}\text{C/W}$	
Reflow soldering temperature	T_{sold}	-	-	260	$^{\circ}\text{C}$	MSL3

3 Electrical characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.

Table 5 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.6	2.5	V	$I_D = 11\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	1.6	-		$I_D = 11\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 125\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	-	0.4	20	μA	$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	4	-		$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	200	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	160	200	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 3\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	330	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 3\text{ A}$; $T_j = 125\text{ }^{\circ}\text{C}$
Gate resistance	R_G	-	3.5	-	Ω	$f = 5\text{ MHz}$; open drain

Table 6 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	83	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	27	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Reverse transfer capacitance	C_{rss}	-	0.4	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	35	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	54	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	22	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	$V_{DS} = 400\text{ V}$; $I_D = 6\text{ A}$; $L = 318\text{ }\mu\text{H}$; $V_{GS} = 6\text{ V}$; $R_{on} = 10\text{ }\Omega$; $R_{off} = 2\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	4	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	6	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

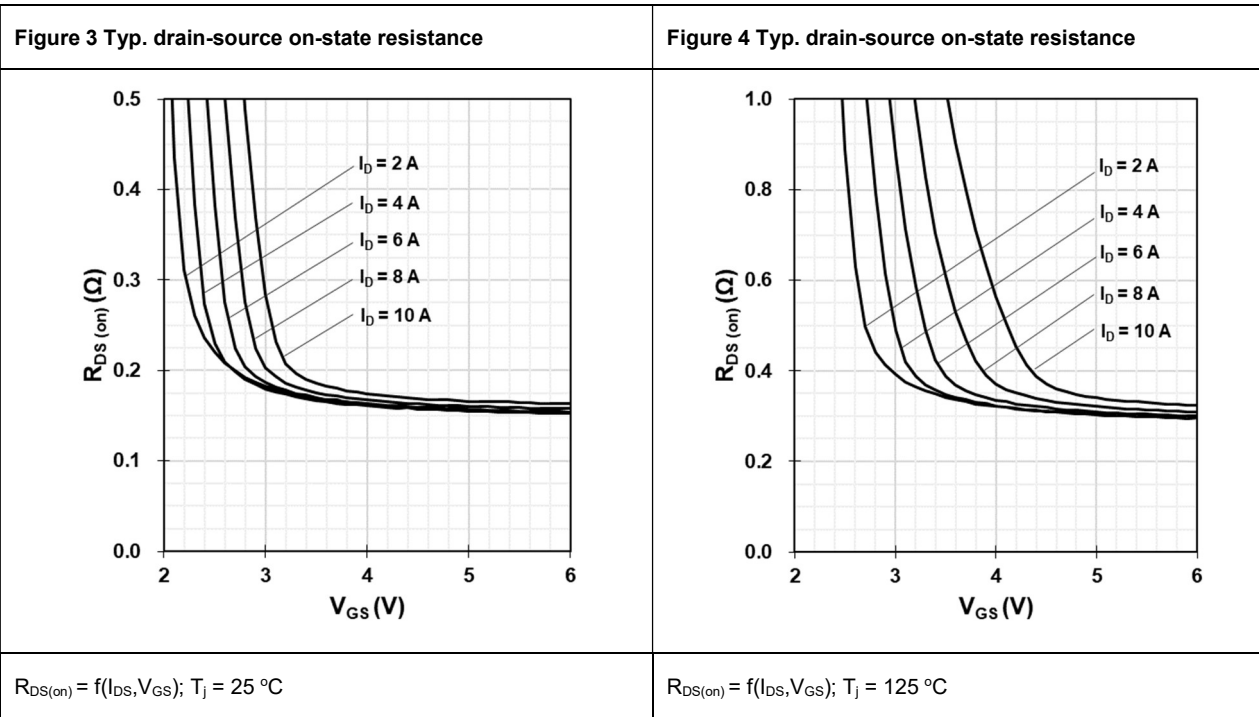
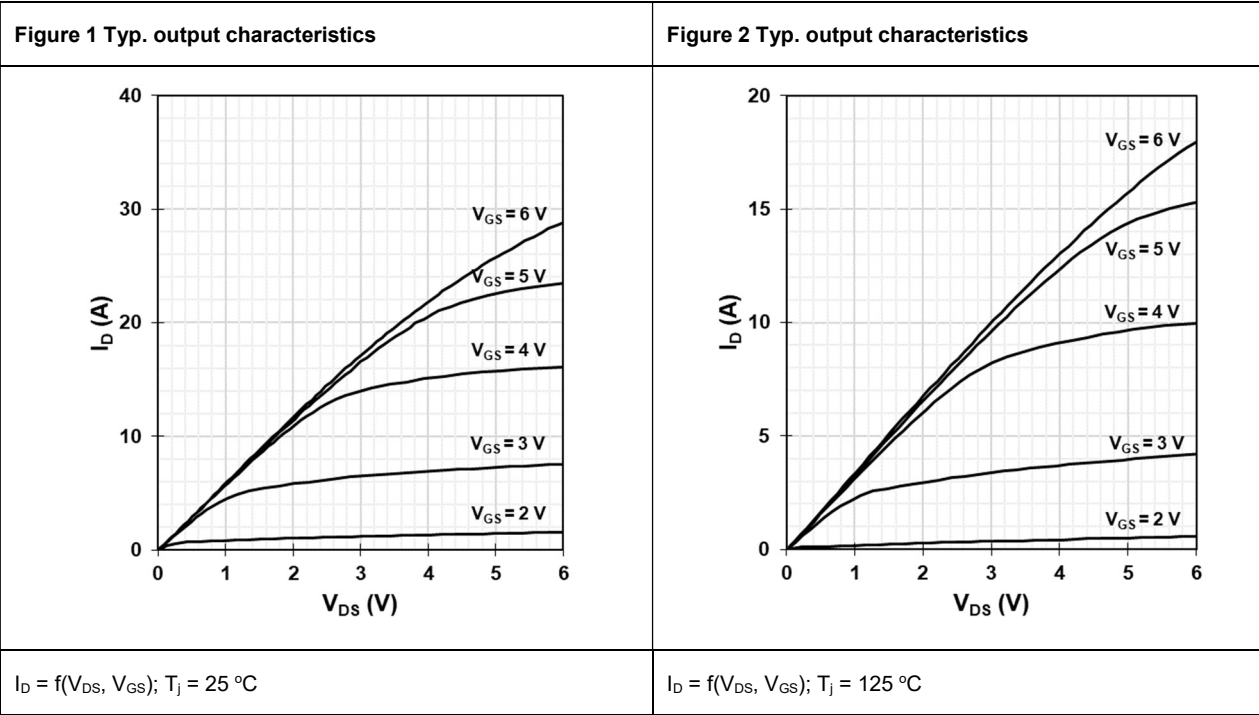
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2.3	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V};$ $I_D = 3 \text{ A}$
Gate-source charge	Q_{GS}	-	0.2	-	nC	
Gate-drain charge	Q_{GD}	-	0.9	-	nC	
Gate plateau voltage	V_{Plat}	-	2.4	-	V	$V_{DS} = 400 \text{ V}; I_D = 3 \text{ A}$

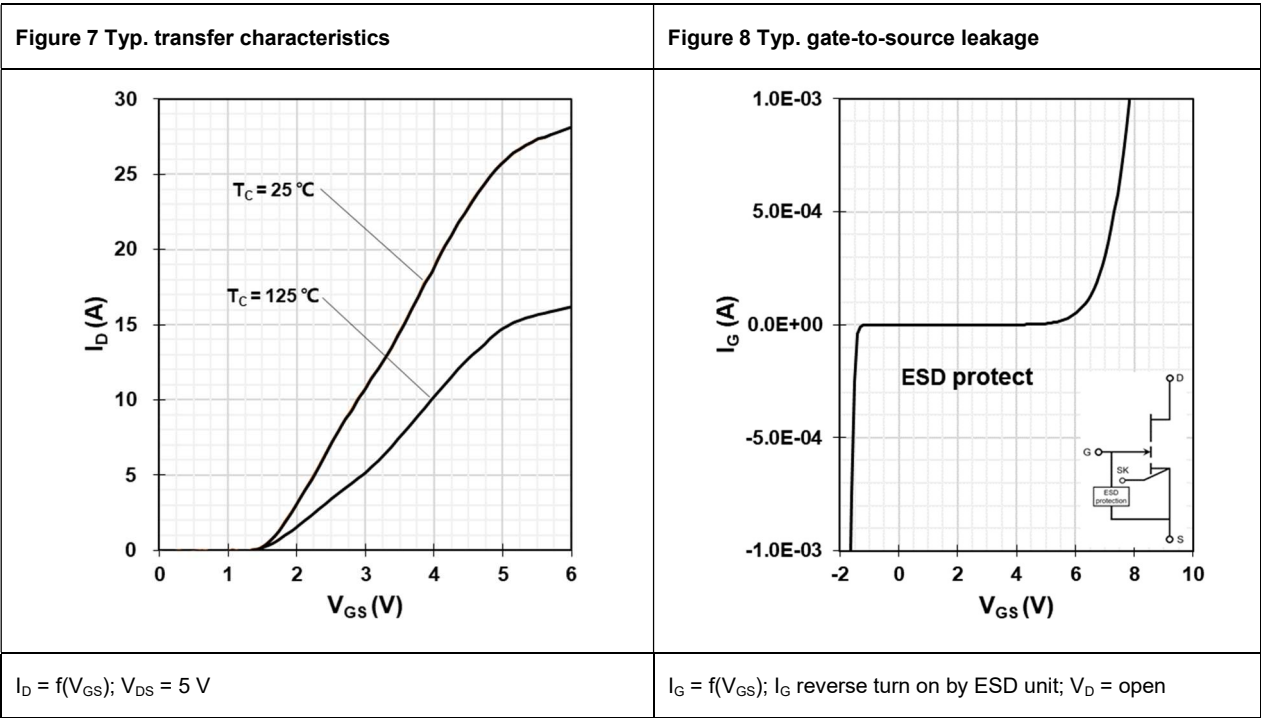
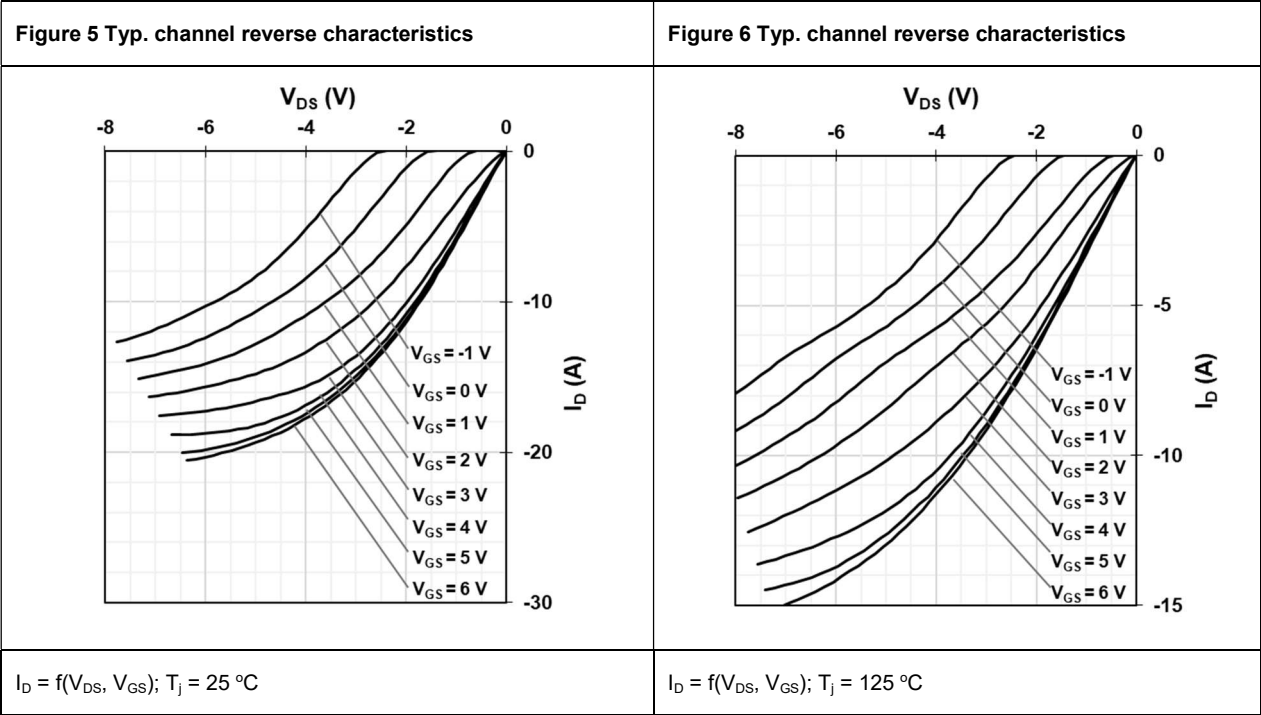
Table 8 Reverse conduction characteristics

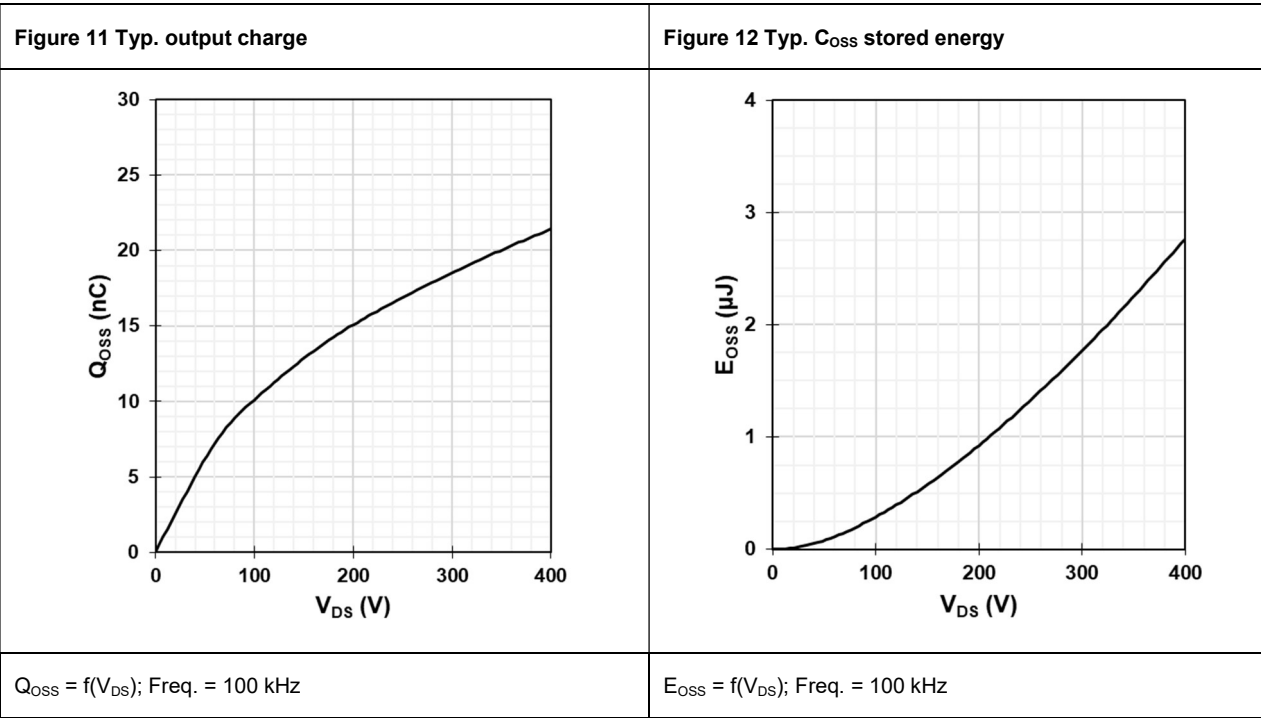
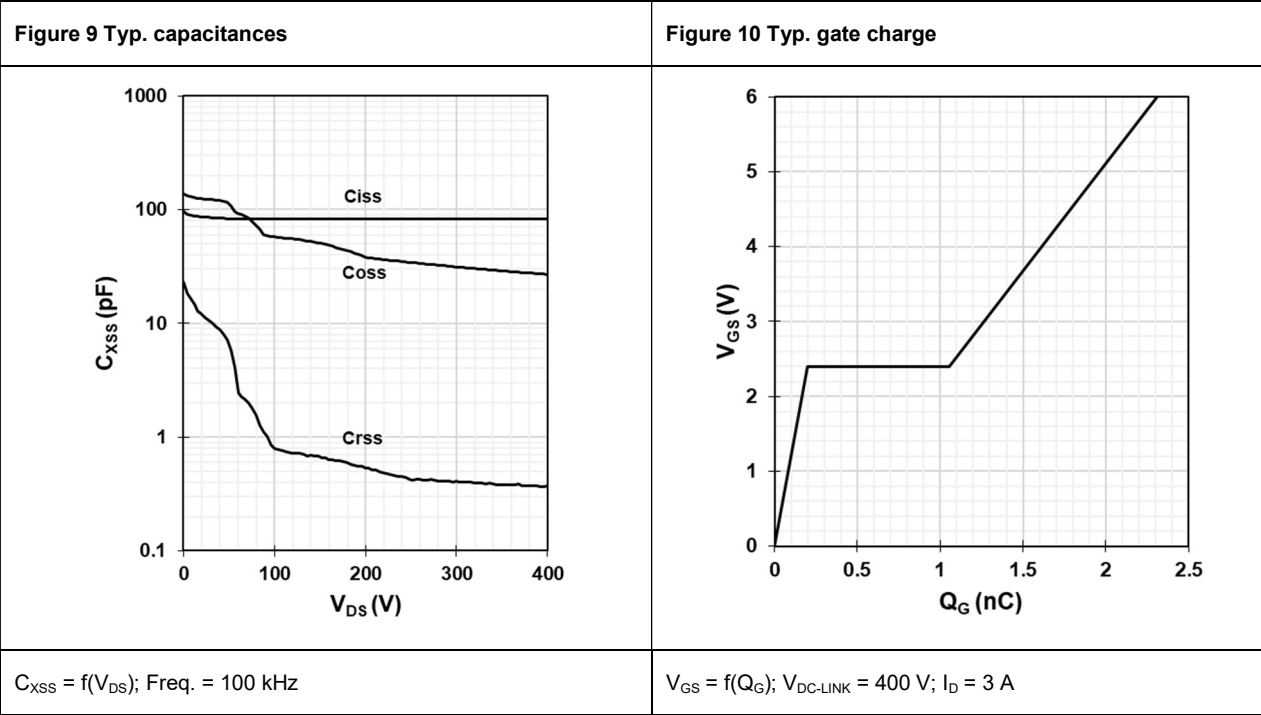
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	2.5	-	V	$V_{GS} = 0 \text{ V}; I_{SD} = 3 \text{ A}$
Pulsed current, reverse	$I_{S, pulse}$	-	20	-	A	$V_{GS} = 6 \text{ V}$
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_{SD} = 3 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

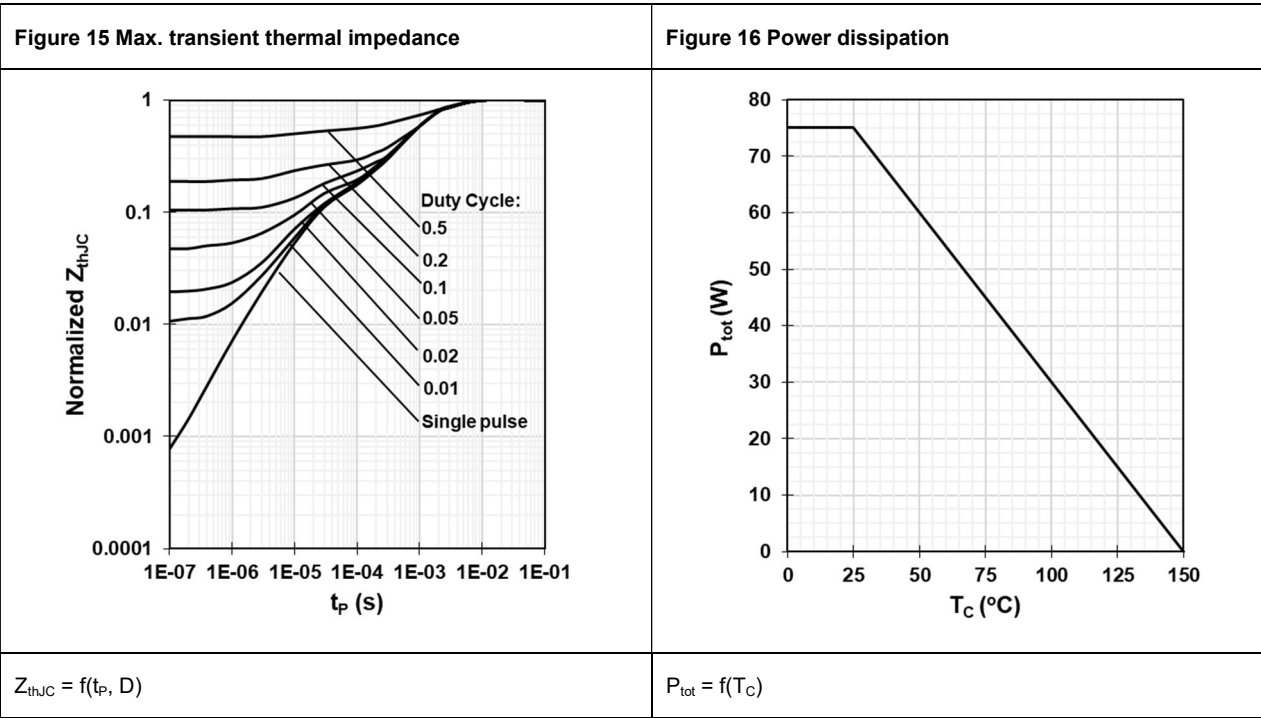
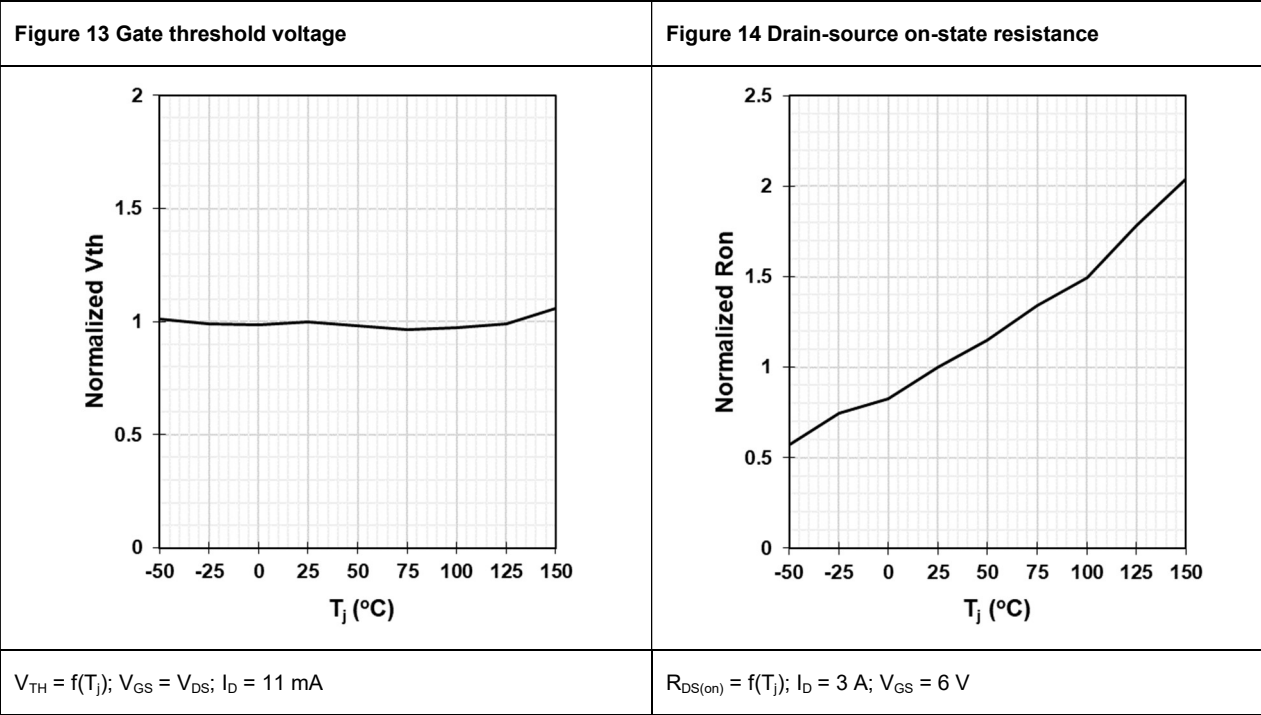
4 Electrical characteristics diagrams

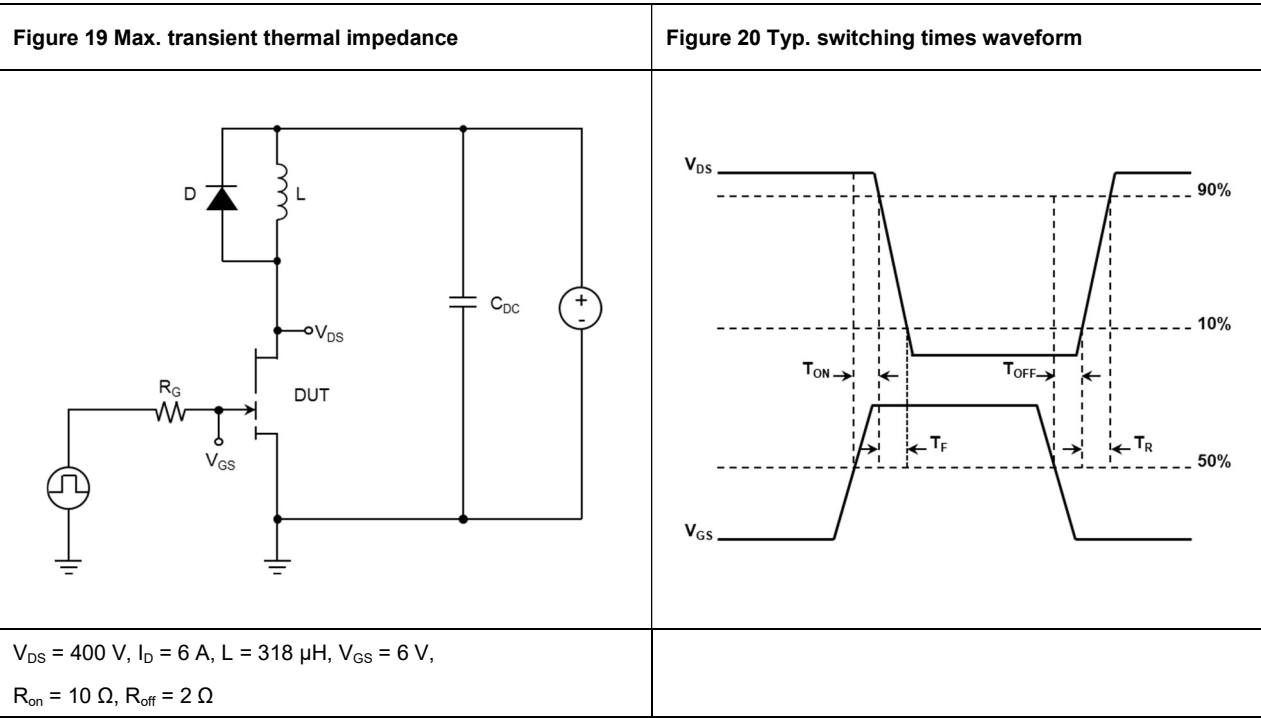
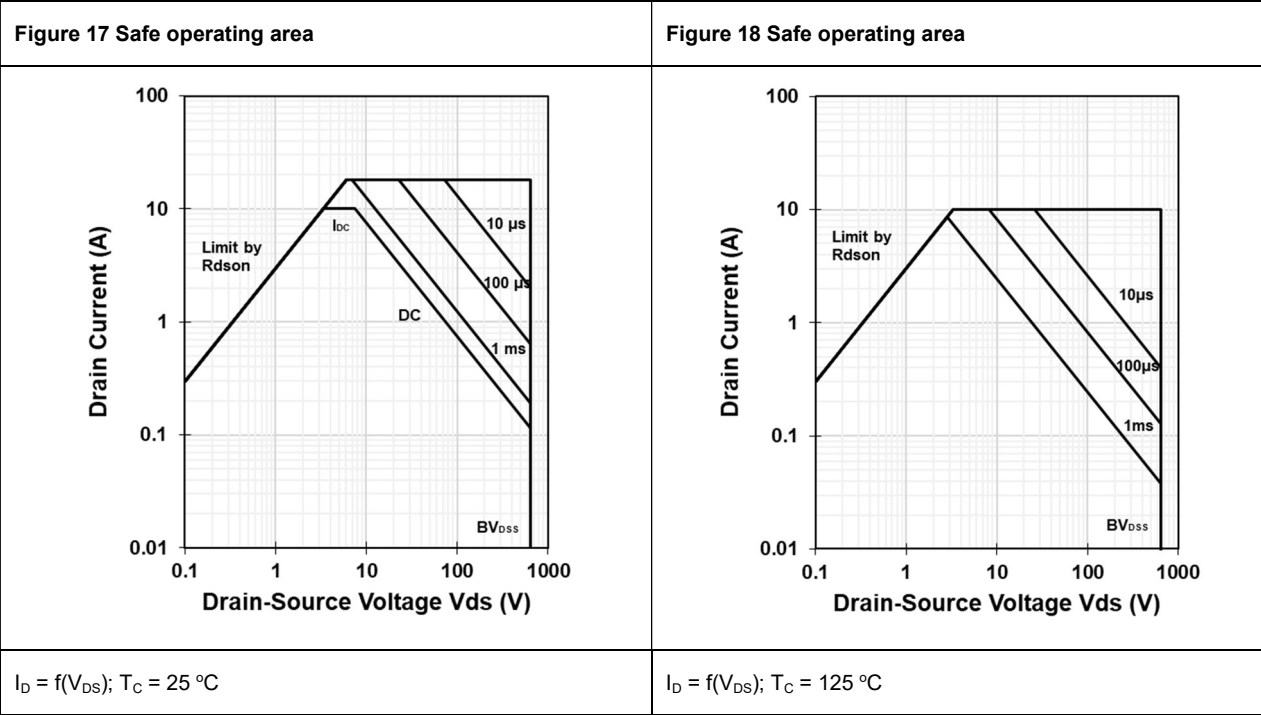
at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.



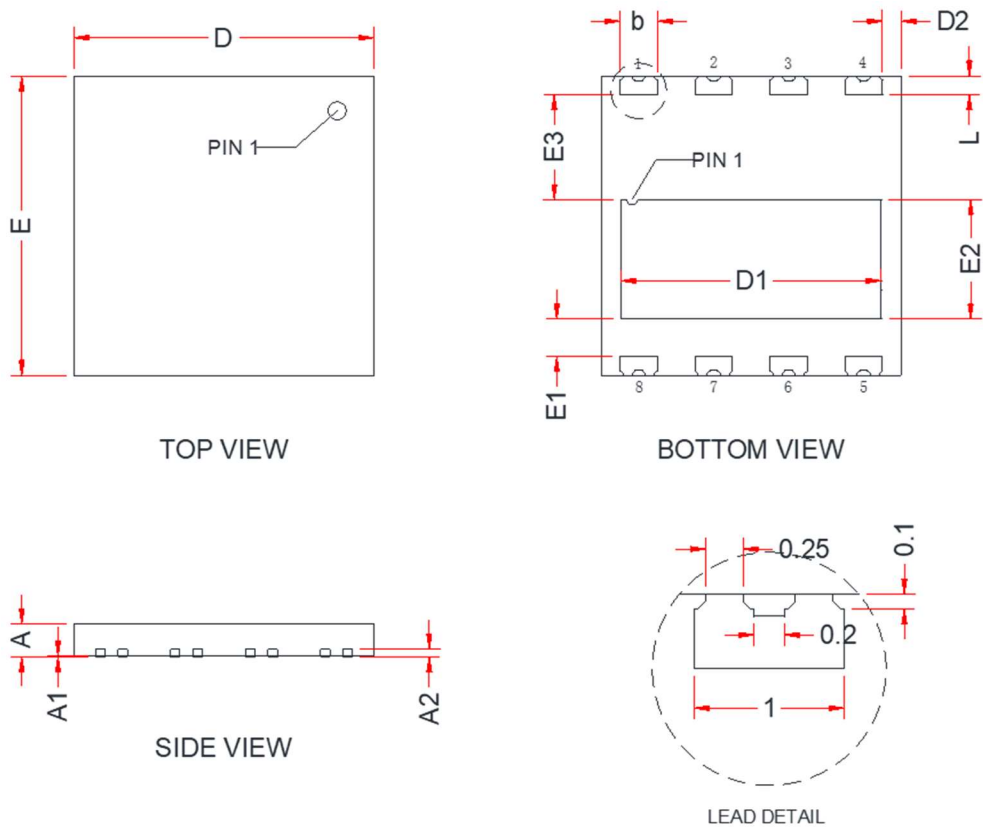








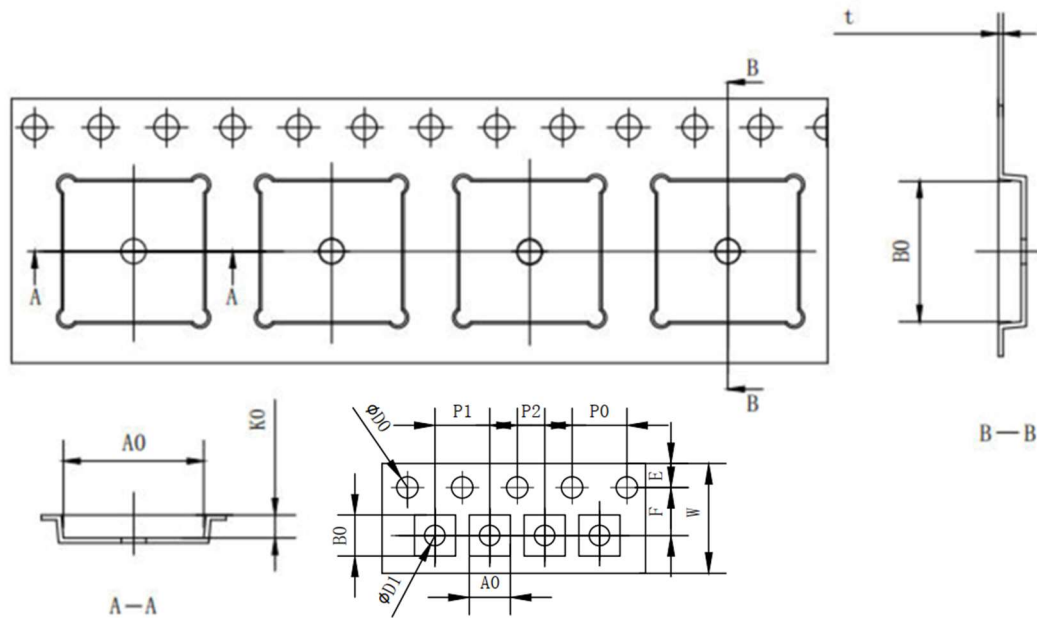
5 Package outlines



Row	Description	Example
Row 1	Device name	HMN10N65D
Row 2	Year & Week	YXWX

	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.95	1.00	1.05
D	8.00BSC		
D1	6.84	6.94	7.04
D2	0.40	0.50	0.60
E	8.00BSC		
E1	0.90	1.00	1.10
E2	3.10	3.20	3.30
E3	2.70	2.80	2.90
e	2.00BSC		
L	0.40	0.50	0.60

6 Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	12.00±0.10
F	7.50±0.10	A0	8.30±0.10
D0	1.50±0.10	B0	8.30±0.10
D1	1.50±0.10	K0	1.10±0.10
P0	4.00±0.10	T	0.30±0.05
P2	2.00±0.10		

