


32Mbyte(8Mx36) 72-pin FP with Parity MODE 2K Ref. SIMM Design 5V
Part No. HMD8M36M18, HMD8M36M18G

GENERAL DESCRIPTION

The HMD8M36M18G is a 8M x 36bit dynamic RAM high density memory module. The module consists of sixteen CMOS 4M x 4bit DRAM in 24-pin SOJ packages and two CMOS 4Mx 4bit Quad-CAS DRAM in 28pin SOJ packages mounted on a 72-pin, double-sided, FR-4-printed circuit board. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM components. The module is a single In-line Memory Module with edge connections and is intended for mounting in to 72-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

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FEATURES

w Part Identification

HMD8M36M18---- 2048 Cycles/32ms Ref. Solder Lead

HMD8M36M18G-- 2048 Cycles/32ms Ref. Gold Lead

w Access times : 50, 60ns

w High-density 32MByte design

w Single + 5V $\pm 0.5V$ power supply

w JEDEC standard PDpin and pinout

w Fast Page with Parity mode operation

w /CAS-before-/RAS refresh capability

w /RAS-only and Hidden refresh capability

w TTL compatible inputs and outputs

w FR4-PCB design

OPTIONS

w Timing

50ns access -5

60ns access -6

w Packages

72-pin SIMM M

MARKING

PRESENCE DETECT PINS(Optional)

Pin	50ns	60ns
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC
5	50ns	13ns	90ns
6	60ns	15ns	110ns

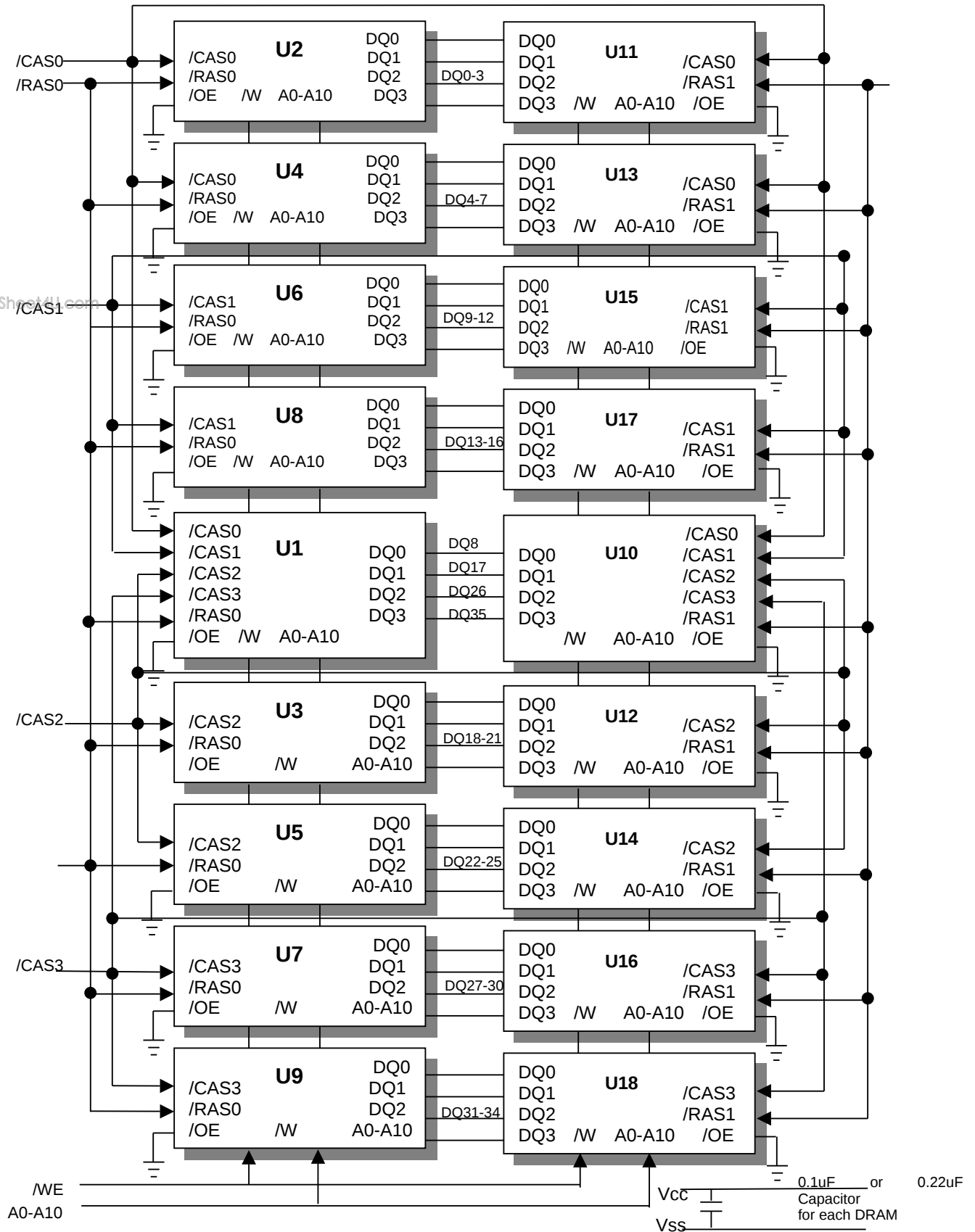
PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	/CAS0	58	DQ31
5	DQ19	23	DQ23	41	/CAS2	59	Vcc
6	DQ2	24	DQ6	42	/CAS3	60	DQ32
7	DQ20	25	DQ24	43	/CAS1	61	DQ14
8	DQ3	26	DQ7	44	/RAS0	62	DQ33
9	DQ21	27	DQ25	45	/RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	/WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

**SIMM
TOP VIEW**

Note: A11 is used for only 4K Ref.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	V_{IN_OUT}	-1V to 7.0V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 7.0V
Power Dissipation	P_D	18W
Storage Temperature	T_{STG}	-55°C to 150°C
Short Circuit Output Current	I_{OS}	50mA

Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 ° C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

SYMBOL	SPEED	MIN	MAX	UNITS
I_{CC1}	-5	-	1008	mA
	-6	-	918	mA
I_{CC2}	Don't care	-	36	mA
I_{CC3}	-5	-	1008	mA
	-6	-	918	mA
I_{CC4}	-5	-	828	mA
	-6	-	738	mA
I_{CC5}	Don't care	-	18	mA
I_{CC6}	-5	-	1008	mA
	-6	-	918	mA
$I_{IL(L)}$		-90	90	μA
$I_{OL(L)}$		-10	10	μA
V_{OH}		2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS= V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS= V_{IH} , /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS= V_{IL} , /CAS, Address cycling @ $t_{PC}=\min$)

I_{CC5} : Standby Current (/RAS=/CAS= $V_{CC}-0.2V$)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @ $t_{RC}=\min$)

I_{IL} : Input Leakage Current (Any input $0V \leq V_{IN} \leq 6.5V$, all other pins not under test = $0V$)

I_{OL} : Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)

V_{OH} : Output High Voltage Level ($I_{OH} = -5mA$)

V_{OL} : Output Low Voltage Level ($I_{OL} = 4.2mA$)

* **NOTE:** I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , address can be changed maximum once while /RAS= V_{IL} . In I_{CC4} , address can be changed maximum once within one page mode cycle.

CAPACITANCE ($T_A=25^{\circ}C$, $V_{CC} = 5V$, $f = 1MHz$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance [A0-A11(A10)]	C_{IN1}	-	110	pF
Input Capacitance (/W)	C_{IN2}	-	130	pF
Input Capacitance (/RAS0)	C_{IN3}	-	80	pF
Input Capacitance (/CAS0-/CAS3)	C_{IN4}	-	40	pF
Input/Output Capacitance (DQ0-31)	C_{DO1}	-	25	pF

AC CHARACTERISTICS ($0^{\circ}C \leq T_A \leq 70^{\circ}C$, $V_{CC} = 5V \pm 10\%$, See notes 1,2.)

STANDARD OPERATION	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	90		110		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		13		15	ns
Access time from column address	t_{AA}		25		30	ns
/CAS to output in Low-Z	t_{CLZ}	3		3		ns
Output buffer turn-off delay	t_{OFF}	3	13	3	13	ns
Transition time (rise and fall)	t_T	2	50	2	50	ns
/RAS precharge time	t_{RP}	30		40		ns
/RAS pulse width	t_{RAS}	50	10K	60	10K	ns
/RAS hold time	t_{RSH}	13		15		ns
/CAS hold time	t_{CSH}	50		60		ns
/CAS pulse width	t_{CAS}	13	10K	15	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	37	20	45	ns
/RAS to column address delay time	t_{RAD}	15	25	15	30	ns
/CAS to /RAS precharge time	t_{CRP}	5		5		ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns

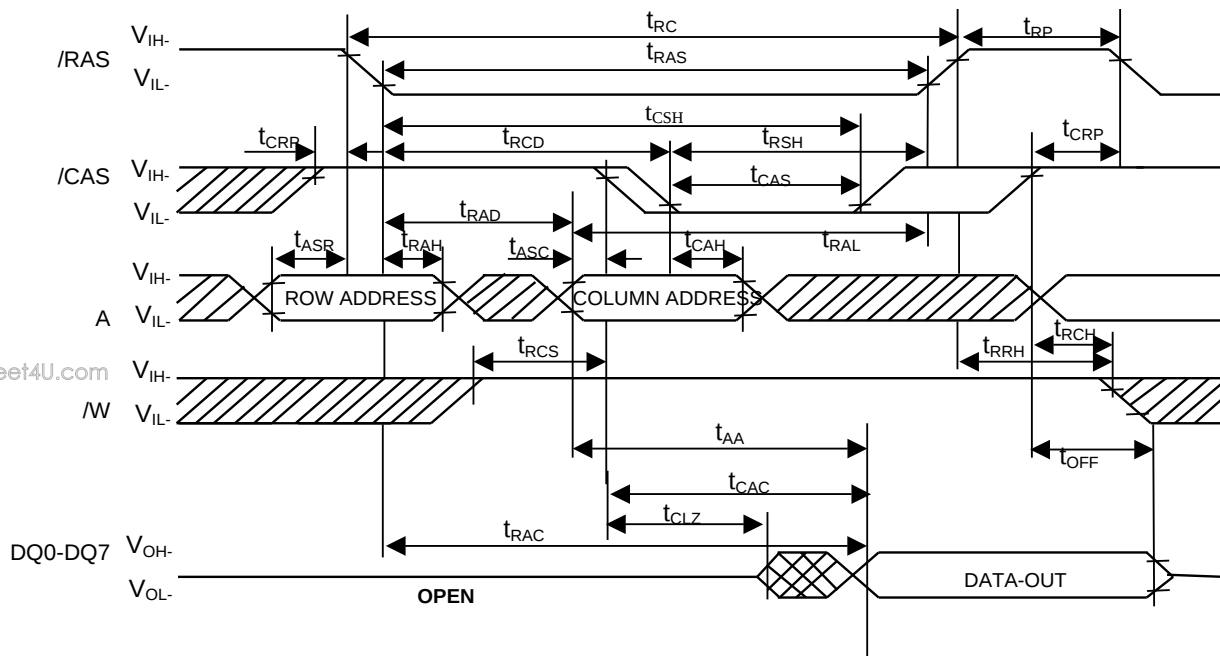
Column address set-up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	10		10		ns
Column Address to /RAS lead time	t_{RAL}	25		30		ns
Read command set-up time	t_{RCS}	0		0		ns
Read command hold referenced to /CAS	t_{RCH}	0		0		ns
Read command hold referenced to /RAS	t_{RRH}	0		0		ns
Write command hold time	t_{WCH}	10		10		ns
Write command hold referenced to /RAS	t_{WCR}	50		55		ns
Write command pulse width	t_{WP}	10		10		ns
Write command to /RAS lead time	t_{RWL}	13		15		ns
Write command to /CAS lead time	t_{CWL}	13		15		ns
Data-in set-up time	t_{DS}	0		0		ns
Data-in hold time	t_{DH}	10		15		ns
Refresh period	t_{REF}		64		64	ns
Write command set-up time	t_{WCS}	0		0		ns
/CAS setup time (C-B-R refresh)	t_{CSR}	5		5		ns
/CAS hold time (C-B-R refresh)	t_{CHR}	10		10		ns
/RAS precharge to /CAS hold time	t_{RPC}	5		5		ns
Access time from /CAS precharge	t_{CPA}		30		35	ns
/CAS precharge time (Fast page)	t_{CP}	10		10		ns
/RAS pulse width (Fast page)	t_{RASP}	50	200K	60	200K	ns
/W to /RAS precharge time (C-B-R refresh)	t_{WRP}	10		10		ns
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10		10		ns

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameter.
They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA} .

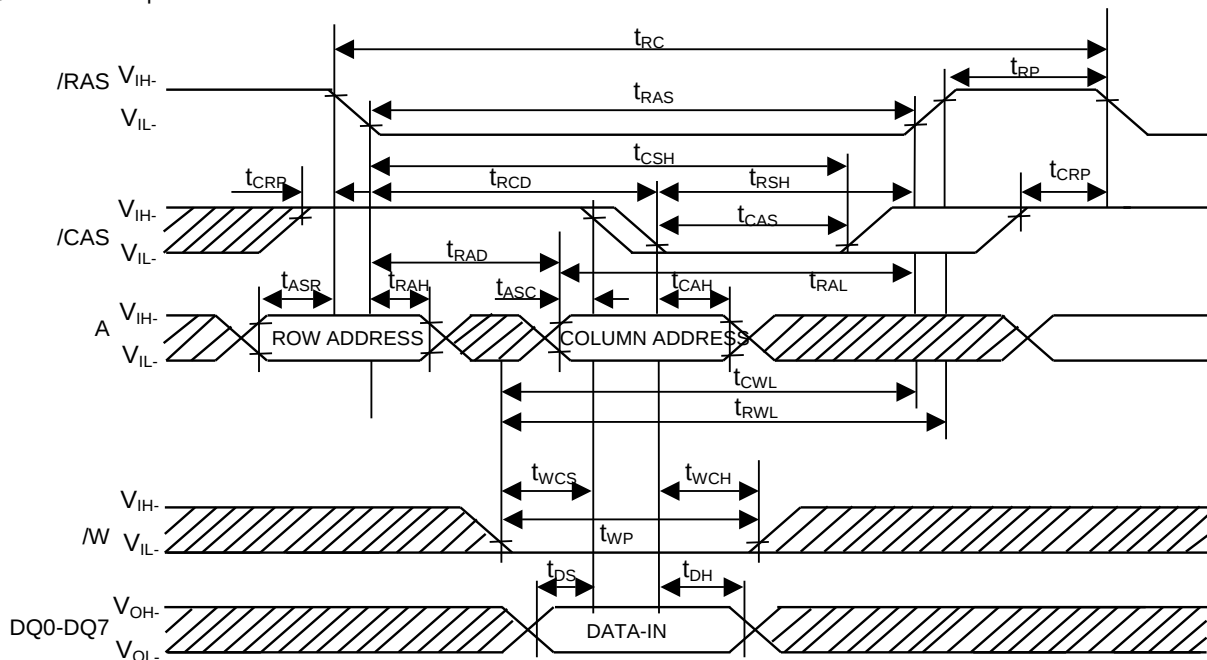
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE (EARLY WRITE)

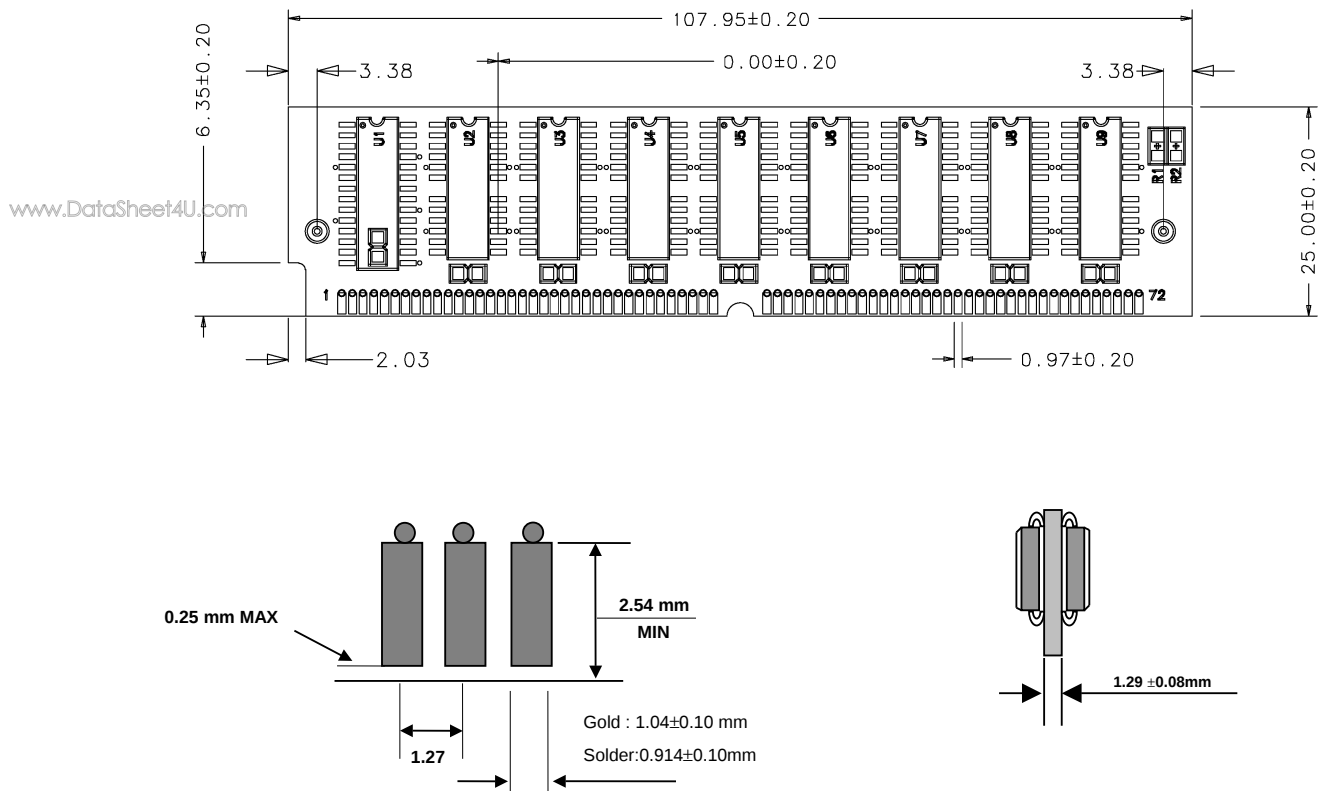
NOTE : Dout = Open



PACKAGING INFORMATION

SIMM Design

(Front)



ORDERING INFORMATION

Part Number	Density	Org.	Package	Vcc	SPEED
HMD8M36M18G-5	32MByte	8MX 36bit	72 Pin-SIMM	5.0V	50ns
HMD8M36M18G-6	32MByte	8MX 36bit	72 Pin-SIMM	5.0V	60ns