16Mbyte(4Mx32) Fast Page Mode, 4K Refresh 72Pin SIMM

Part No. HMD4M32M8GL

GENERAL DESCRIPTION

The HMD4M32M8GL is a 4M x 32bit dynamic RAM high-density memory module. The module consists of eight CMOS 4M x 4bit DRAMs in 24-pin SOJ packages mounted on a 72-pin, double-sided, FR-4-printed circuit board. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM components. The module is a single In-line Memory Module with edge connections and is intended for mounting in to 72-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Part Identification
  HMD4M32M8GL- 4,096 Cycles/64ms Ref . Gold
- Access times : 50, 60ns
- High-density 16MByte design
- Single + 5V ±0.5V power supply
- JEDEC standard pinout
- FP(Fast Page) mode operation
- TTL compatible inputs and outputs
- FR4-PCB design

OPTIONS MARKING

- Timing
  - 50ns access -5
  - 60ns access -6
- Packages
  - 72-pin SIMM M

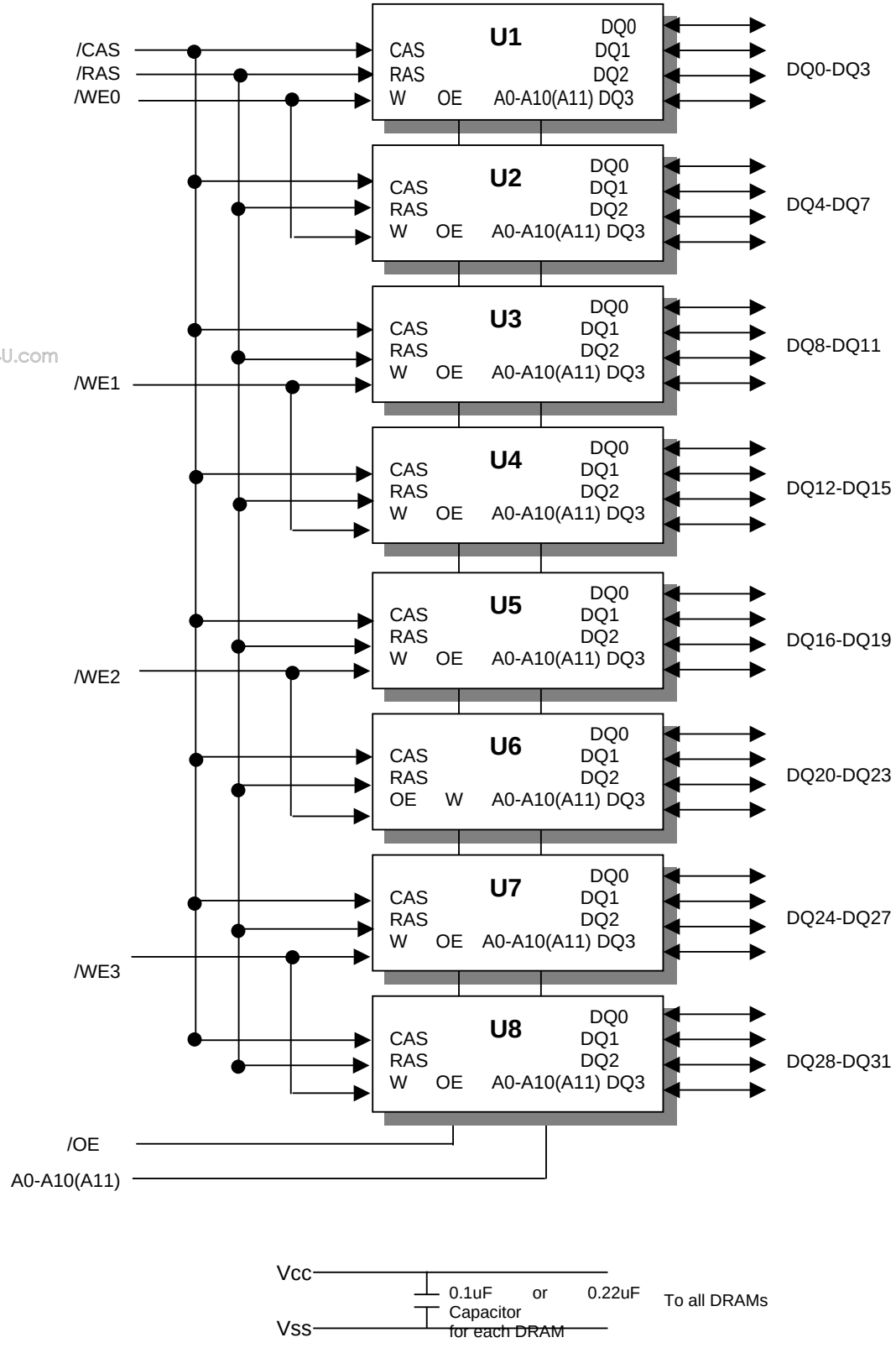
PIN CONFIGURATION DESCRIPTION

Pin Name	FUNCTION
A0 – A11	Address Input(4K Ref.)
A0 – A10	Address Input(2K Ref.)
DQ0-31	Data In/Out
/WE0-/WE3	Read/Write Input
/OE	Data Output Enable
/CAS	Column Address Strobe
/RAS	Row Address Strobe
BD_{IN}	Board Insertion Signal
SIZE	Size Indentification
Vcc/ Vss	Power and Ground
NC	No Connection

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ22	49	DQ8
2	DQ0	26	DQ7	50	DQ24
3	DQ16	27	DQ23	51	DQ9
4	DQ1	28	A8	52	DQ25
5	DQ17	29	A10	53	DQ10
6	DQ2	30	Vcc	54	DQ26
7	DQ18	31	/WE2	55	DQ11
8	DQ3	32	NC	56	DQ27
9	DQ19	33	Vss	57	DQ12
10	Vcc	34	/RAS	58	DQ28
11	/WE0	35	Vcc	59	/WE3
12	A0	36	NC	60	DQ29
13	A1	37	NC	61	DQ13
14	A2	38	/OE0	62	DQ30
15	A3	39	Vss	63	DQ14
16	A4	40	/CAS	64	DQ31
17	A5	41	Vcc	65	DQ15
18	A6	42	NC	66	Vss
19	A7	43	NC	67	NC
20	DQ4	44	NC	68	NC
21	DQ20	45	A9	69	BD_{IN}
22	DQ5	46	A11	70	NC
23	DQ21	47	/WE1	71	SIZE
24	DQ6	48	Vcc	72	Vss

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 7.0V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 7.0V
Power Dissipation	P_D	8W
Storage Temperature	T_{STG}	-55°C to 150°C
Short Circuit Output Current	I_{OS}	50mA

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

SYMBOL	SPEED	MIN	MAX	UNITS
I_{CC1}	-5	-	720	mA
	-6	-	640	mA
I_{CC2}		-	16	mA
I_{CC3}	-5	-	720	mA
	-6	-	640	mA
I_{CC4}	-5	-	640	mA
	-6	-	560	mA
I_{CC5}		-	8	mA
I_{CC6}	-5	-	720	mA
	-6	-	640	mA
$I_{I(L)}$		-40	40	µA
$I_{O(L)}$		-40	40	µA
V_{OH}		2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS=V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS=V_{IH}, /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS=V_{IL}, /CAS, Address cycling @t_{PC}=min)

I_{CC5} : Standby Current (/RAS=/CAS=Vcc-0.2V)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @t_{RC}=min)

I_{IL} : Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)

I_{OL} : Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V

V_{OH} : Output High Voltage Level (I_{OH}= -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE**: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address cad be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25°C, Vcc = 5V, f = 1Mz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A11)	C_{IN1}	-	40	pF
Input Capacitance (/WE0-/WE3)	C_{IN2}	-	49	pF
Input Capacitance (/RAS)	C_{IN3}	-	49	pF
Input Capacitance (/CAS)	C_{IN4}	-	49	pF
Input/Output Capacitance (DQ0-31)	C_{DQ1}	-	49	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

STANDARD OPERATION	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	90		110		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		13		15	ns
Access time from column address	t_{AA}		25		30	ns
/CAS to output in Low-Z	t_{CLZ}	0		0		ns
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns
Transition time (rise and fall)	t_T	3	50	3	50	ns
/RAS precharge time	t_{RP}	30		40		ns
/RAS pulse width	t_{RAS}	50	10K	60	10K	ns
/RAS hold time	t_{RSH}	13		15		ns
/CAS hold time	t_{CSH}	50		60		ns
/CAS pulse width	t_{CAS}	13	10K	15	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	37	20	45	ns
/RAS to column address delay time	t_{RAD}	15	25	15	30	ns
/CAS to /RAS precharge time	t_{CRP}	5		5		ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns
Column address set-up time	t_{ASC}	0		0		ns

Column address hold time	t_{CAH}	10	10	ns
Column address hold referenced to /RAS	t_{AR}	40	45	ns
Column Address to /RAS lead time	t_{RAL}	25	30	ns
Read command set-up time	t_{RCS}	0	0	ns
Read command hold referenced to /CAS	t_{RCH}	0	0	ns
Read command hold referenced to /RAS	t_{RRH}	0	0	ns
Write command hold time	t_{WCH}	10	10	ns
Write command hold referenced to /RAS	t_{WCR}	40	45	ns
Write command pulse width	t_{WP}	10	10	ns
Write command to /RAS lead time	t_{RWL}	15	15	ns
Write command to /CAS lead time	t_{CWL}	13	15	ns
Data-in set-up time	t_{DS}	0	0	ns
Data-in hold time	t_{DH}	10	15	ns
Data-in hold referenced to /RAS	t_{DHR}	40	45	ns
Refresh period 2K Ref.	t_{REF}	32	32	ns
Write command set-up time	t_{WCS}	0	0	ns
/CAS setup time (C-B-R refresh)	t_{CSR}	5	5	ns
/CAS hold time (C-B-R refresh)	t_{CHR}	10	10	ns
/RAS precharge to /CAS hold time	t_{RPC}	5	5	ns
Access time from /CAS precharge	t_{CPA}	30	35	ns
Fast page mode cycle time	t_{PC}	35	40	ns
/CAS precharge time (Fast page)	t_{CP}	10	10	ns
/RAS pulse width (Fast page)	t_{RASP}	50 200K	60 200K	ns
/W to /RAS precharge time (C-B-R refresh)	t_{WRP}	10	10	ns
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10	10	ns
/CAS precharge(C-B-R counter test)	t_{CPT}	20	20	ns

NOTES

1.An initial pause of 200μs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.

2.$V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.

3.Measured with a load equivalent to 2TTL loads and 100pF

4.Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

5.Assumes that $t_{RCD} \geq t_{RCD(max)}$

6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$

7.This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter.

They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write

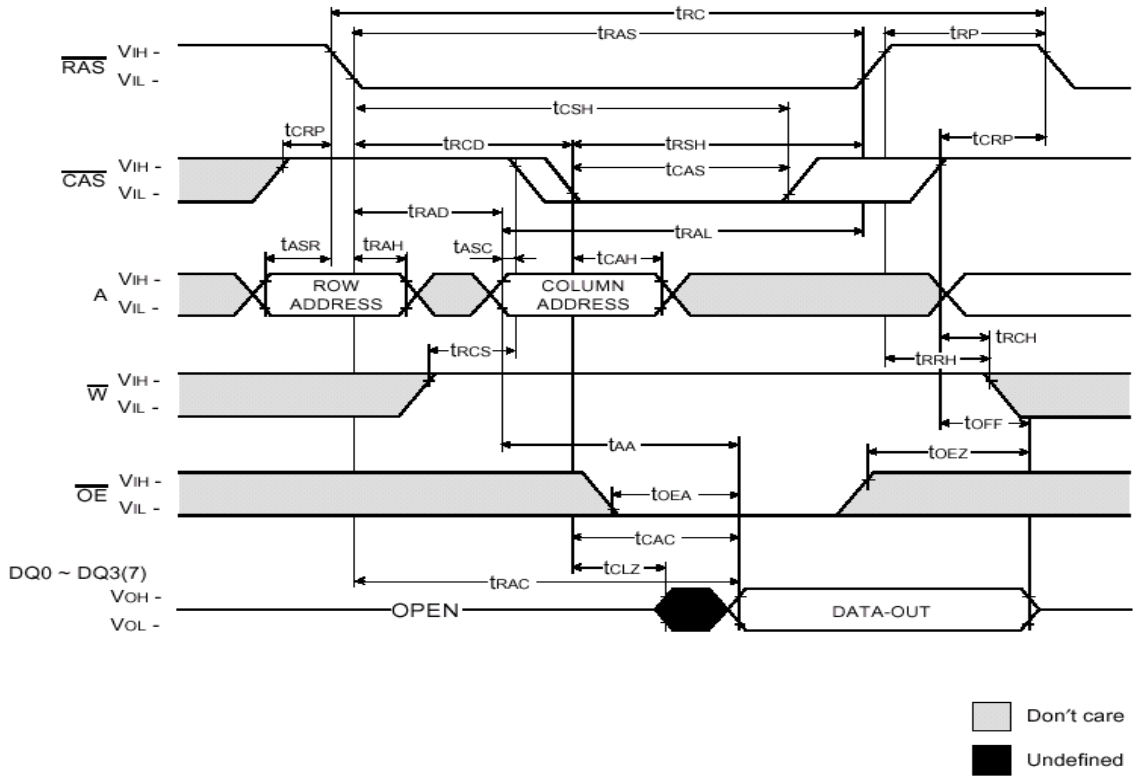
cycle and the data out pin will remain high impedance for the duration of the cycle.

9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by t_{AA}.

TIMING DIAGRAM

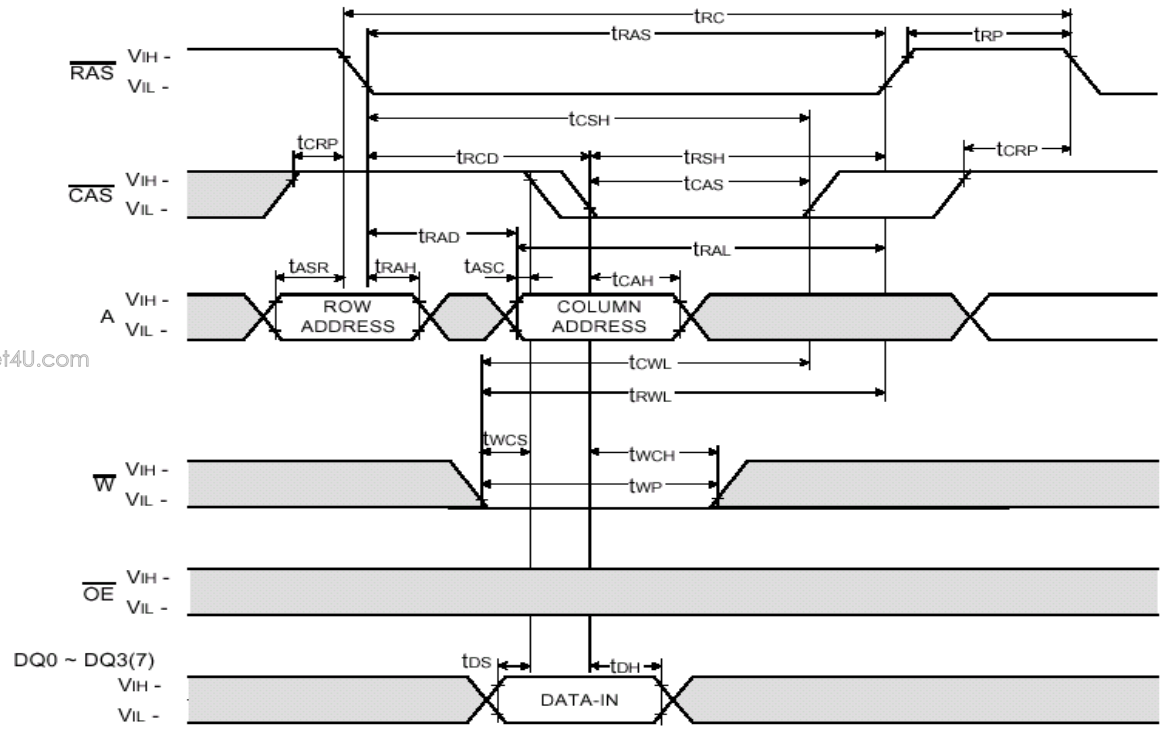
Please refer to attached timing diagram chart (I)

READ CYCLE



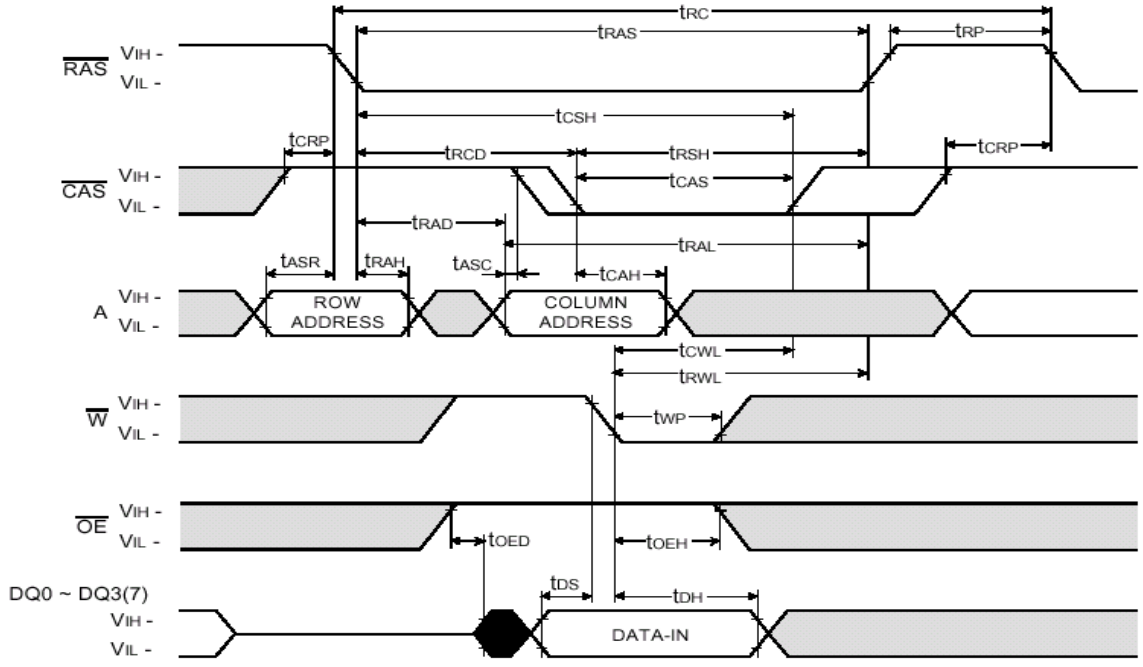
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

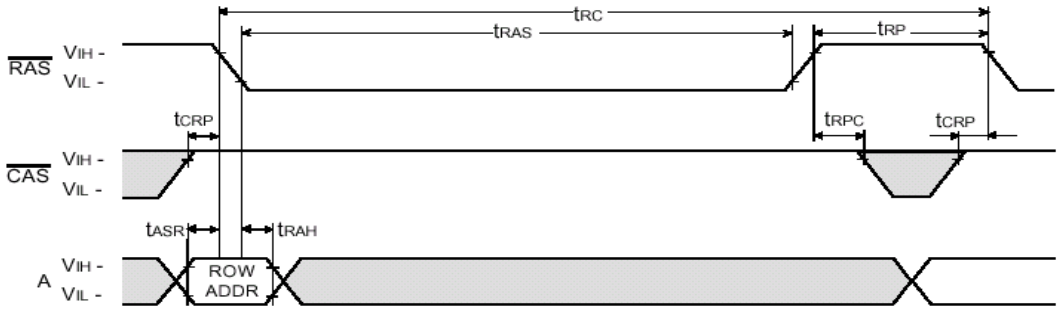
NOTE : DOUT = OPEN



$\overline{RAS}$ - ONLY REFRESH CYCLE

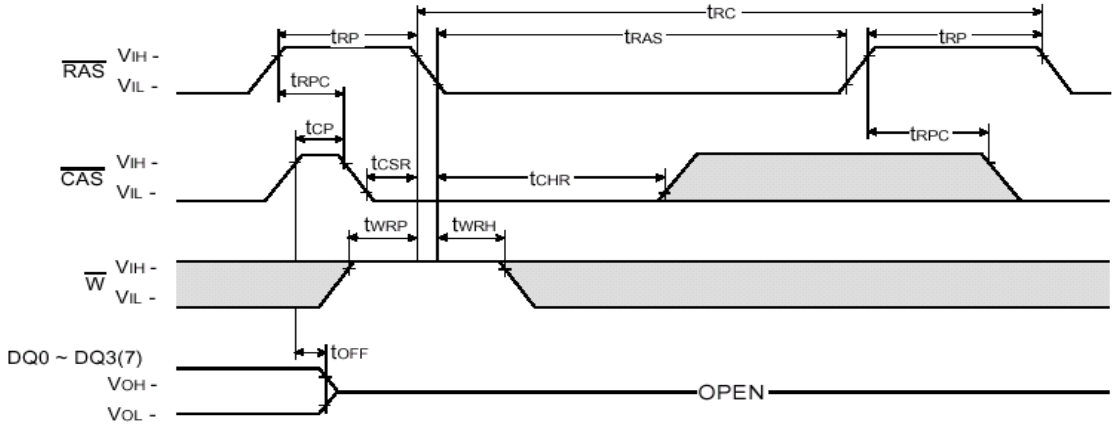
NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

DOUT = OPEN



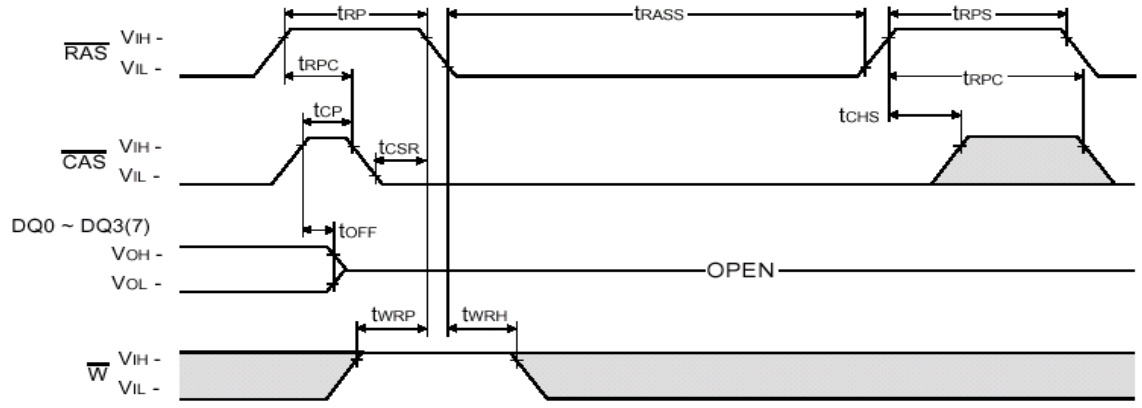
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



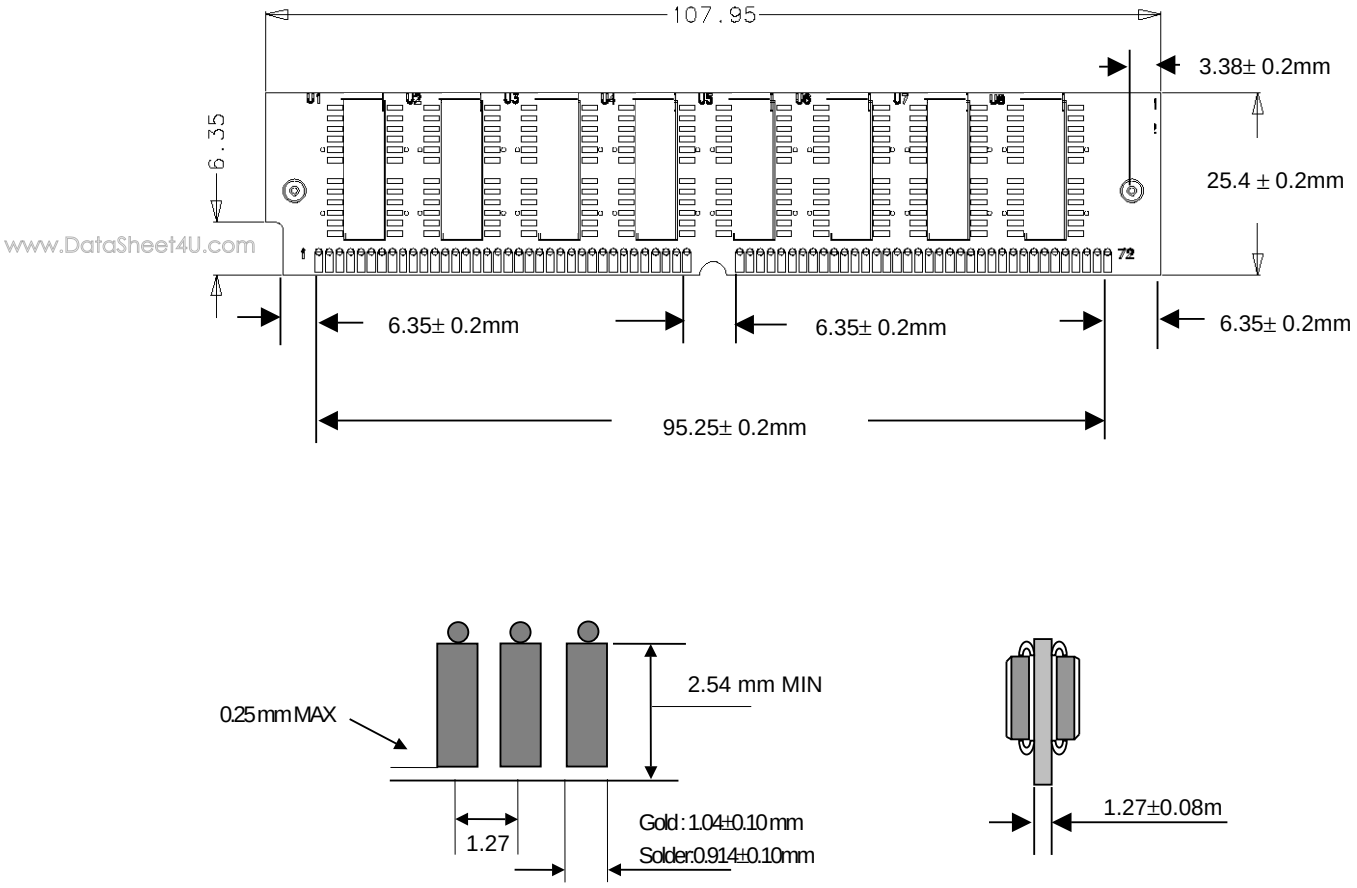
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



PACKAGING INFORMATION

SIMM Design



ORDERING INFORMATION

Part Number	Density	Org.	Package	Refresh Cycle	Vcc	SPEED
HMD4M32M8GL-5	16MByte	4MX 32bit	72 Pin-SIMM	4K Cycles 64ms Ref.	5.0V	50ns
HMD4M32M8GL-6	16MByte	4MX 32bit	72 Pin-SIMM	4K Cycles 64ms Ref.	5.0V	60ns