HMCS412 Series/ HMCS414 Series/ HMCS424 Series

Description

The HMCS412/414/424 Series are HMCS400 Series CMOS 4-bit single-chip microcomputers. Each device incorporates a ROM, RAM, I/O, serial interface, and timer/counter, including high-voltage I/O pins with high-current output pins to directly drive a fluorescent display.

Features

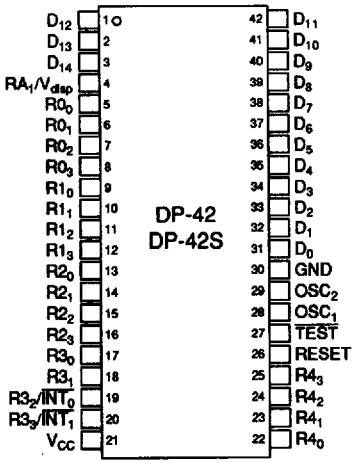
- 2048-word × 10-bit ROM (HMCS412)
  4096-word × 10-bit ROM (HMCS414/424)
- 160-digit × 4-bit RAM (HMCS412/414)
  256-digit × 4-bit RAM (HMCS424)
- 36 I/O pins including 24 high-voltage I/O pins (40 V max.)
- Timer/counters
  — 8-bit × 1 (HMCS412/414)
  — 8-bit × 2 (HMCS424)
- Clock-synchronous 8-bit serial interface (HMCS424 only)
- Five interrupt sources
  — Two by external sources (HMCS412, 414)
  — One by internal source (HMCS412, 414)
  — Two by external sources (HMCS424)
  — Three by internal sources (HMCS424)
- Subroutine stack up to 16 levels including interrupts
- Low-power dissipation modes
  — Standby mode
  — Stop mode
- On-chip oscillator
  — Crystal or ceramic oscillator
  — Resistor (HMCS412C/414C)
  — External clock input
    C-type: 5-V operation version
    CL-type: 3-V operation version
    AC-type: high speed operation version
- Package
  — Standard 42-pin dual-inline plastic package (DP-42)
  — 42-pin shrink dual-inline plastic package (DP-42S)
  — 44-pin flat plastic package (FP-44A)

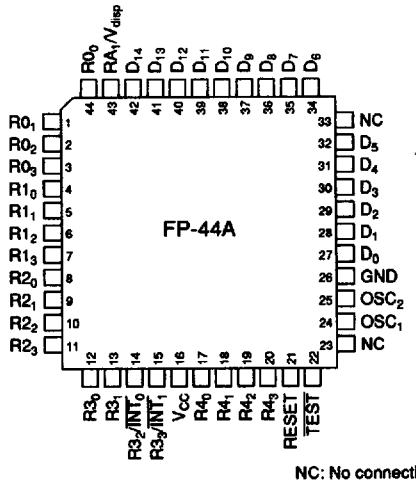
Ordering Information

Series	Product Name	Model Name	Package
HMCS412	HMCS412C	HD614121P	DP-42
		HD614121S	DP-42S
		HD614121H	FP-44A
	HMCS412CL	HD614126P	DP-42
		HD614126S	DP-42S
		HD614126H	FP-44A
	HMCS412AC	HD614129P	DP-42
		HD614129S	DP-42S
		HD614129H	FP-44A
HMCS414	HMCS414C	HD614141P	DP-42
		HD614141S	DP-42S
		HD614141H	FP-44A
	HMCS414CL	HD614146P	DP-42
		HD614146S	DP-42S
		HD614146H	FP-44A
	HMCS414AC	HD614149P	DP-42
		HD614149S	DP-42S
		HD614149H	FP-44A
HMCS424	HMCS424C	HD404240P	DP-42
		HD404240S	DP-42S
		HD404240H	FP-44A
	HMCS424CL	HD40L4240P	DP-42
		HD40L4240S	DP-42S
		HD40L4240H	FP-44A
	HMCS424AC	HD40A4240P	DP-42
		HD40A4240S	DP-42S
		HD40A4240H	FP-44A

Pin Arrangement

HMCS412, HMCS414

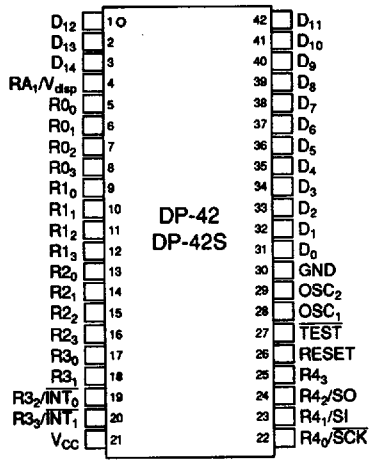


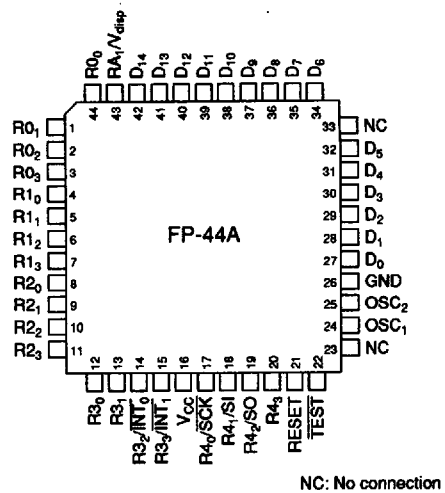


NC: No connection

Top view

HMCS424





NC: No connection

Top view

Pin Functions

GND, V_{CC}, V_{disp} (Power): GND, V_{CC} and V_{disp} are the power supply pins for the MCU. Connect GND to ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA_1) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC} – 40 V). For details, see the Input/Output section.

$\overline{\text{TEST}}$ (Test): $\overline{\text{TEST}}$ is for test purposes only. Connect it to V_{CC}.

RESET (Reset): RESET resets the MCU. For details, see the Reset section.

OSC_1, OSC_2 (Oscillator Connections): OSC_1 and OSC_2 are input pins for the internal oscillator circuit. They can be connected to a crystal, ceramic, or external oscillator circuit. For details, see the Internal Oscillator Circuit section.

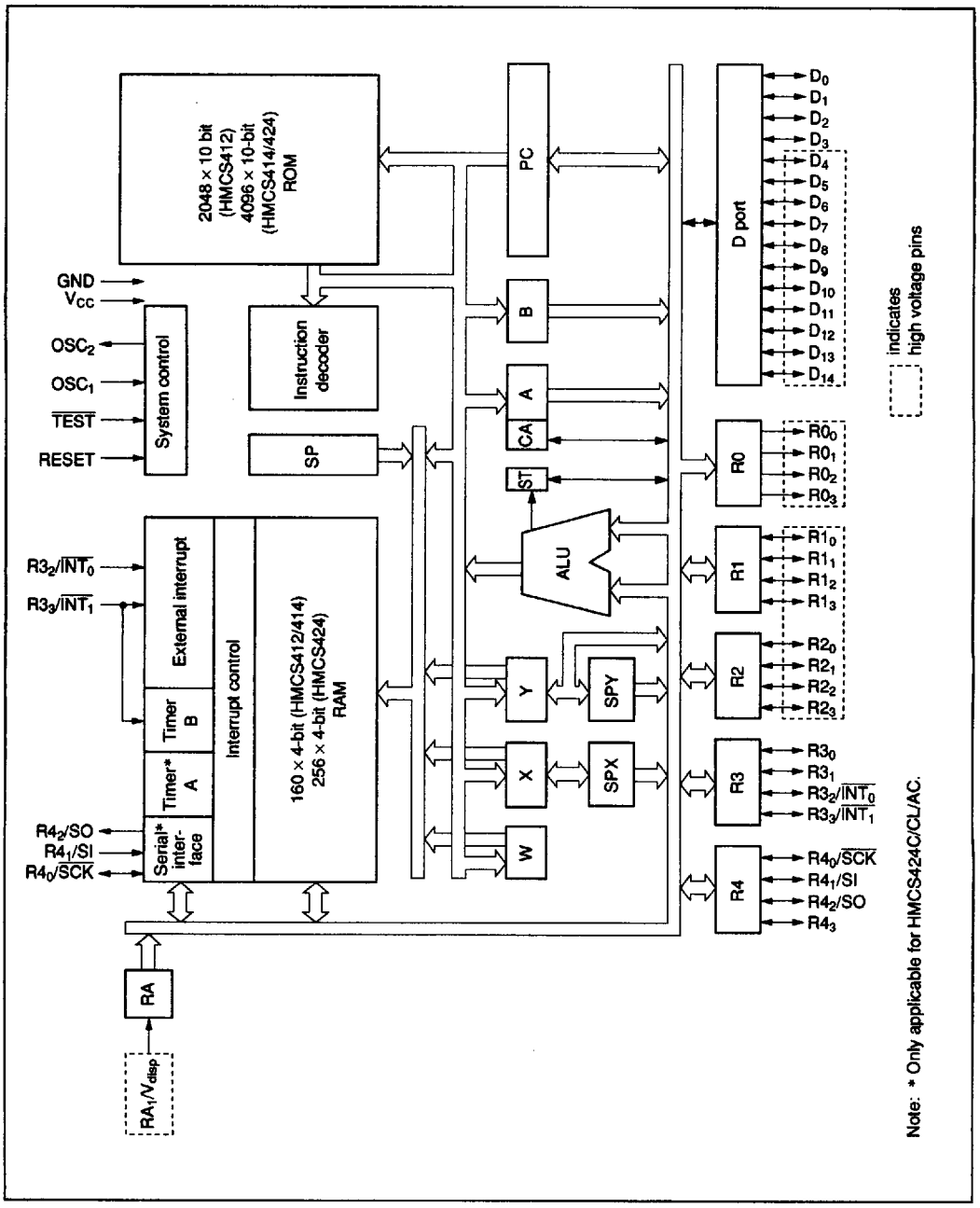
D_0 to D_{14} (D Port): The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D_0 to D_3 are standard and D_4 to D_{14} are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

$R0_0$ to $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, RA_1 (R Ports): R0 to R4 are 4-bit ports. RA is a 1-bit port. R0 is an output port, RA is an input port, and R1 to R4 are I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 and R4 are standard ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$ and $R3_3$ are multiplexed with $\overline{\text{INT}_0}$ and $\overline{\text{INT}_1}$. For HMCS424C/CL/AC, pins $R4_0$, $R4_1$, and $R4_2$ are multiplexed with $\overline{\text{SCK}}$, SI, and SO, respectively. For details, see the Input/Output section.

$\overline{\text{INT}_0}$, $\overline{\text{INT}_1}$ (Interrupts): $\overline{\text{INT}_0}$ and $\overline{\text{INT}_1}$ are external interrupts for the MCU. $\overline{\text{INT}_1}$ can be used as an external event input pin for timer B. $\overline{\text{INT}_0}$ and $\overline{\text{INT}_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupt section.

$\overline{\text{SCK}}$, SI, SO: Only applicable to the HMCS424C/CL/AC. The transmit clock I/O pin ($\overline{\text{SCK}}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{\text{SCK}}$, SI, and SO are multiplexed with $R4_0$, $R4_1$, and $R4_2$, respectively. For details, see the Serial Interface section.

Block Diagram



Memory Map

ROM Memory Map

The MCU contains the following ROM size shown in table 1. The ROM is described in the following paragraphs with the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F can be used for JMPL instructions to branch to the starting address of the initialization program and the interrupt programs. After reset or an interrupt, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F can be used for subroutines. The CAL instruction branches to these subroutines.

Pattern Area
$0000 to $07FF (HMCS412C/CL/AC); $0000 to $0FFF (HMCS414C/CL/AC, HMCS424C/CL/AC): These locations can be used for ROM data. The P instruction allows reference to the ROM data as a pattern.

Program Area
$0000 to $07FF (HMCS412C/CL/AC); $0000 to $0FFF (HMCS414C/CL/AC, HMCS424C/CL/AC): These locations can be used for program code.

Table 1 ROM Size

Series Name	ROM Size
HMCS412C/CL/AC	2048-word × 10-bit
HMCS414C/CL/AC	4096-word × 10-bit
HMCS424C/CL/AC	

Table 2 RAM Size

Series Name	RAM Size
HMCS412C/CL/AC	160-digit × 4-bit
HMCS414C/CL/AC	
HMCS424C/CL/AC	256-digit × 4-bit

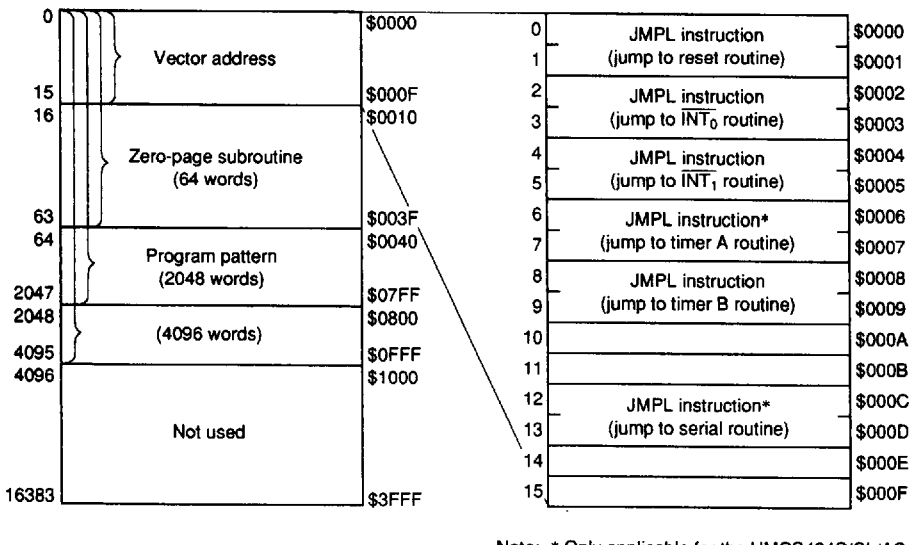


Figure 1 ROM Memory Map

RAM Memory Map

The MCU also contains the following RAM size shown in table 2 as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counters. These registers are classified into three types: write-only, read-only, and read/write, as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area ($020 to $07F (HMCS412C/CL/AC, HMCS414C/CL/AC); $020 to $0DF (HMCS424C/CL/AC)): The 16 digits of $020 through $02F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL or CALL instruction) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status flag and carry flag are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

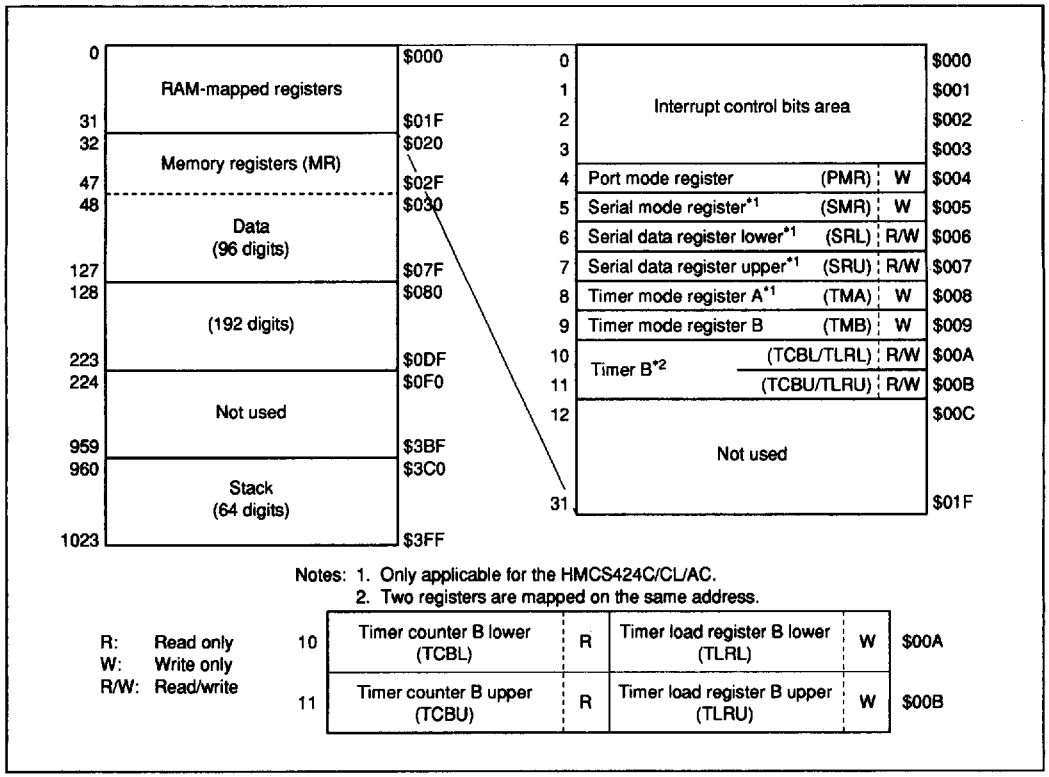


Figure 2 RAM Memory Map

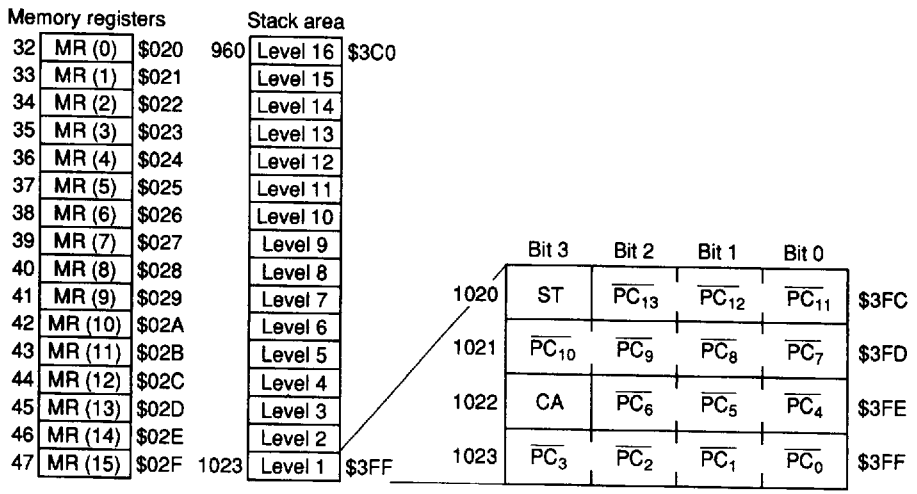
	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA* (IM of timer A)	IFTA* (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not used	Not used	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS* (IM of serial)	IFS* (IF of serial)	$003

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit of the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction. The value of the status flag becomes invalid when the RSP bit or the unusable bits are tested by the TM or TMD instruction.

* Only applicable for the HMCS424C/CL/AC.

Figure 3 Configuration of Interrupt Control Bits Area



PC_{13} to PC_0: Program counter
ST: Status flag
CA: Carry flag

Notes: 1. Since HMCS412C/CL/AC have 2 k ROM, $\overline{PC_{11}}$, $\overline{PC_{12}}$, and $\overline{PC_{13}}$ are not used.
2. Since HMCS414C/CL/AC and HMCS424C/CL/AC have 4 k ROM, $\overline{PC_{12}}$ and $\overline{PC_{13}}$ are not used.

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit write-only W register, and the 4-bit X and Y registers are used for indirect addressing of RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, the carry flag is pushed onto the stack. It is restored by the RTNI instruction, but not by the RTN instruction.

Status Flag (ST): The status flag (ST) holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instruction. The value of the status flag remains unchanged until the next arithmetic, compare, or bit test instruction is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction is executed or not. During an interrupt, the status flag is pushed onto the stack and restored back from the stack by the RTNI instruction, but not by the RTN instruction.

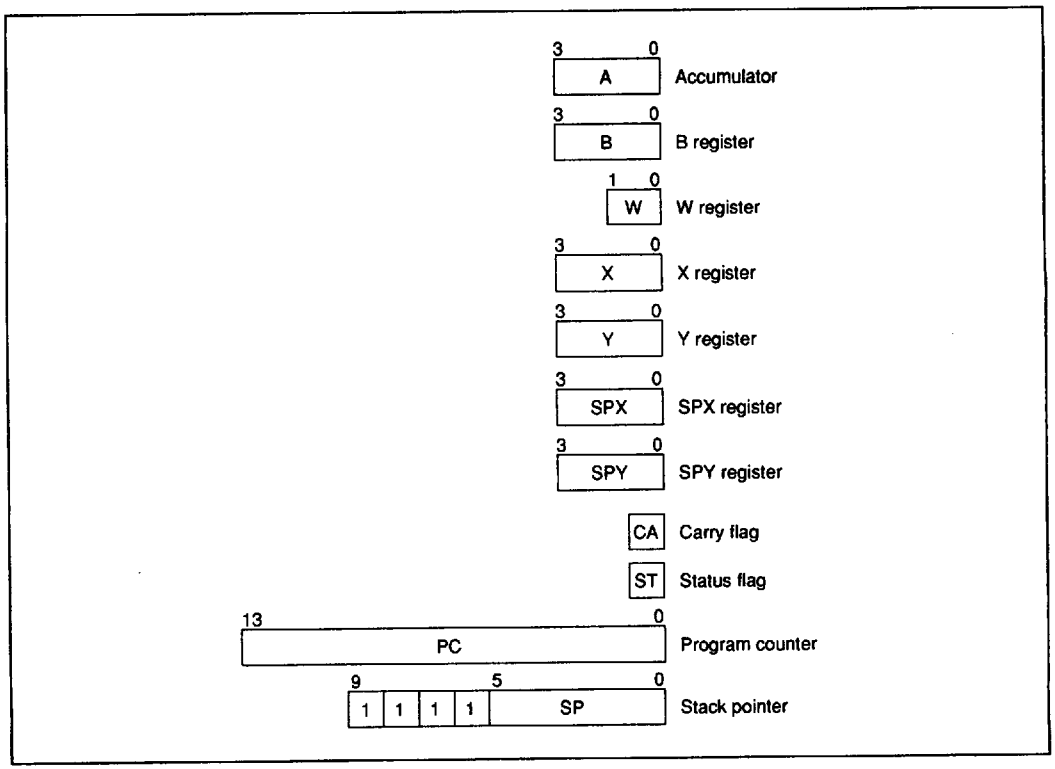


Figure 5 Registers and Flags

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to $3FF by either MCU reset or the RSP bit reset by the REM/REMD instruction.

Interrupts

Three interrupt sources are available on the MCU of HMCS412C/CL/AC and HMCS414C/CL/AC. They are two external requests ($\overline{INT_0}$, $\overline{INT_1}$) and one timer/counter (timer B). HMCS424C/CL/AC has five interrupt sources: the three sources stated above, timer A and serial interface (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Servicing: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 by MCU reset.

Table 3 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A*	3	$0006
Timer B*	4	$0008
Serial*	5	$000C

Note: * Only applicable for the HMCS424C/CL/AC.

Table 4 Interrupt Conditions

Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A*1	Timer B	Serial*1
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$*1	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$*1	*	*	*	*	1

Notes: * Don't care
*1 Only applicable for the HMCS424C/CL/AC.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

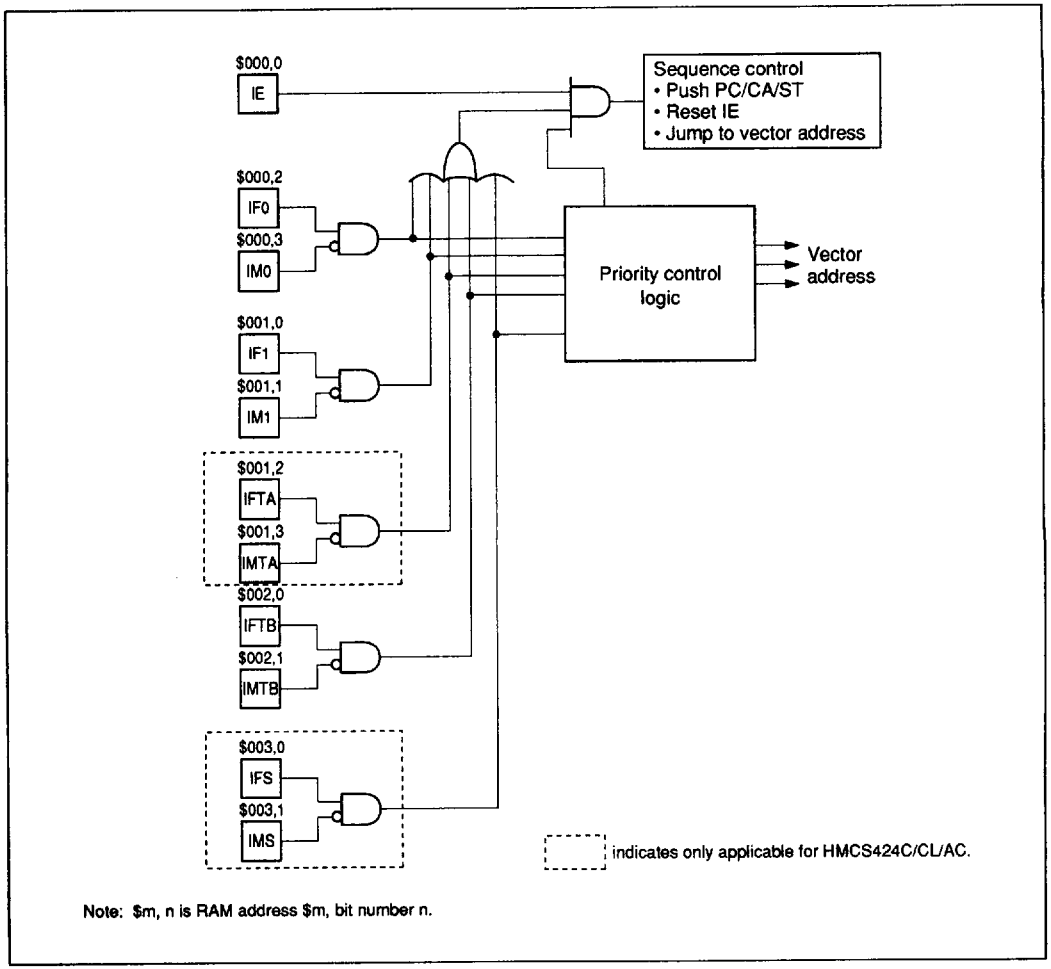


Figure 6 Interrupt Control Circuit Block diagram

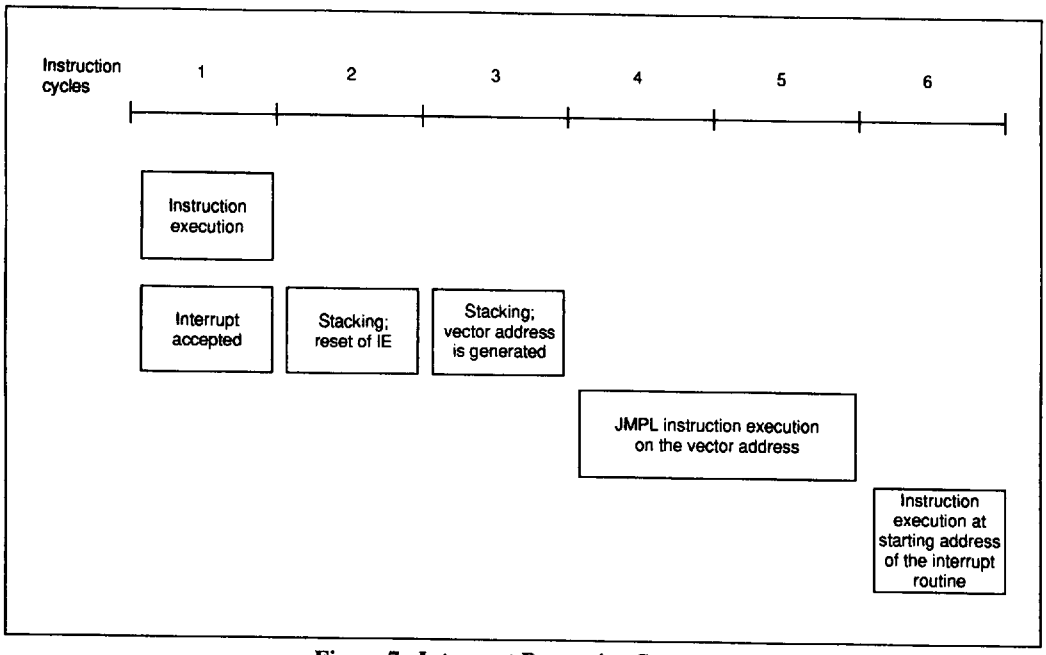


Figure 7 Interrupt Processing Sequence

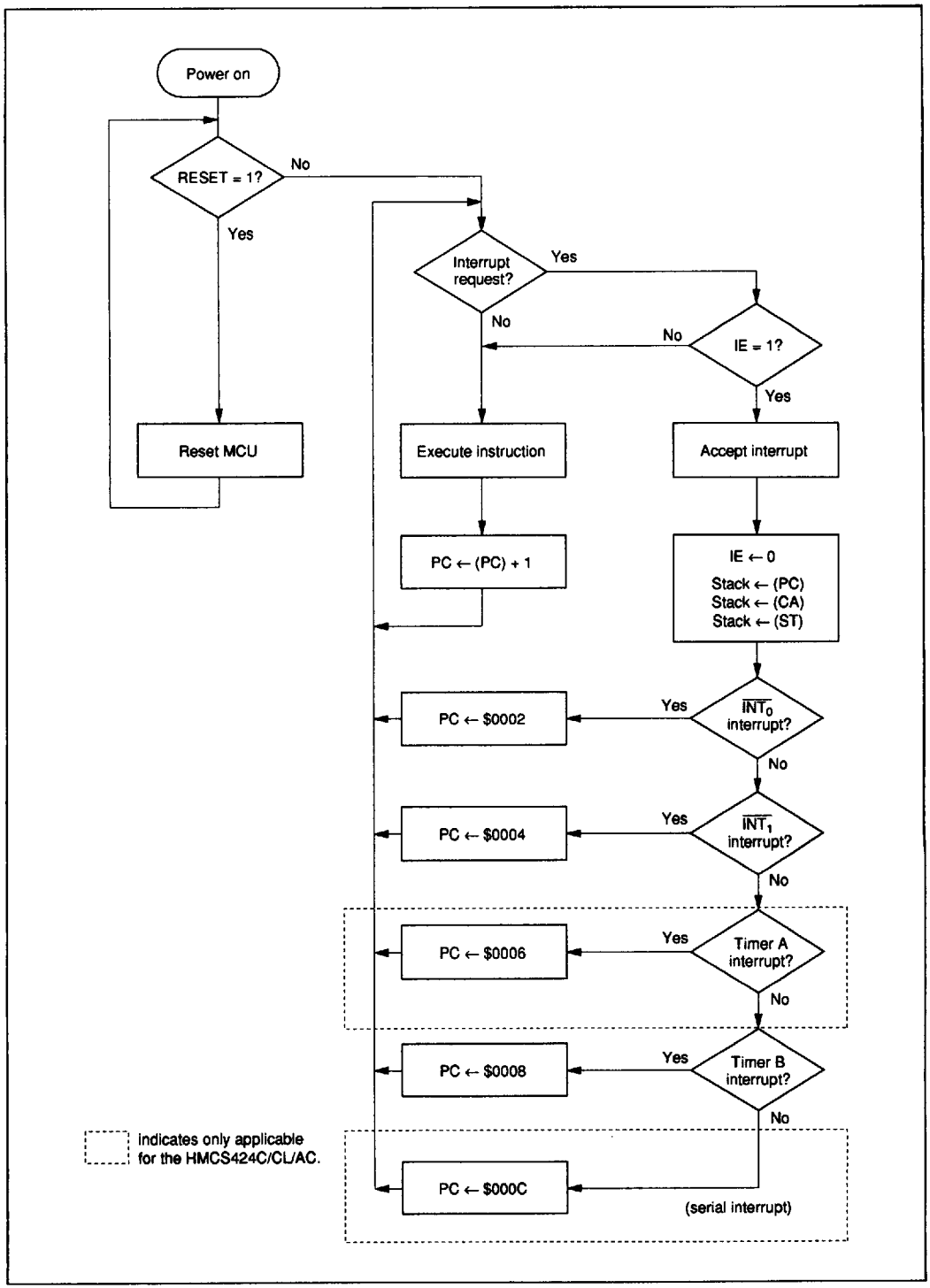


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 5. It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT_1}$ and $R3_2/\overline{INT_0}$ pins to be used as $\overline{INT_1}$ and $\overline{INT_0}$, respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs (table 6).

The $\overline{INT_1}$ input can be used as a clock signal input to timer B, in which timer B counts up at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as timer B external event input, the external interrupt mask (IM1) has to be set so that the $\overline{INT_1}$ interrupt request will not be accepted (table 7).

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$, and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The 4-bit write-only port mode register controls the $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, $R4_1$/SI, and $R4_2$/SO pins as shown in table 8. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 5 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 6 External Interrupt Request Flags

IF0, IF1	Interrupt Requests
0	No
1	Yes

Table 7 External Interrupt Masks

IM0, IM1	Interrupt Requests
0	Enabled
1	Disabled (masked)

Table 8 Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR1	$R4_1$/SI Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2$/SO Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

Note: PMR0 and PMR1 can be only used by the HMCS424C/CL/AC.

Serial Interface

Only applicable for the HMCS424C/CL/AC. The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register, the octal counter, and the multiplexer, as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to \$0. The counter starts to count at the falling edge of the transmit clock signals ($\overline{SCK}$) and increments by one at the rising edge of the $\overline{SCK}$. When the octal counter is reset to \$0 after eight transmit clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the $R4_0/\overline{SCK}$, prescaler divide ratio, and transmit clock source, as shown in table 9. The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying the transmit clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

The contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it is necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

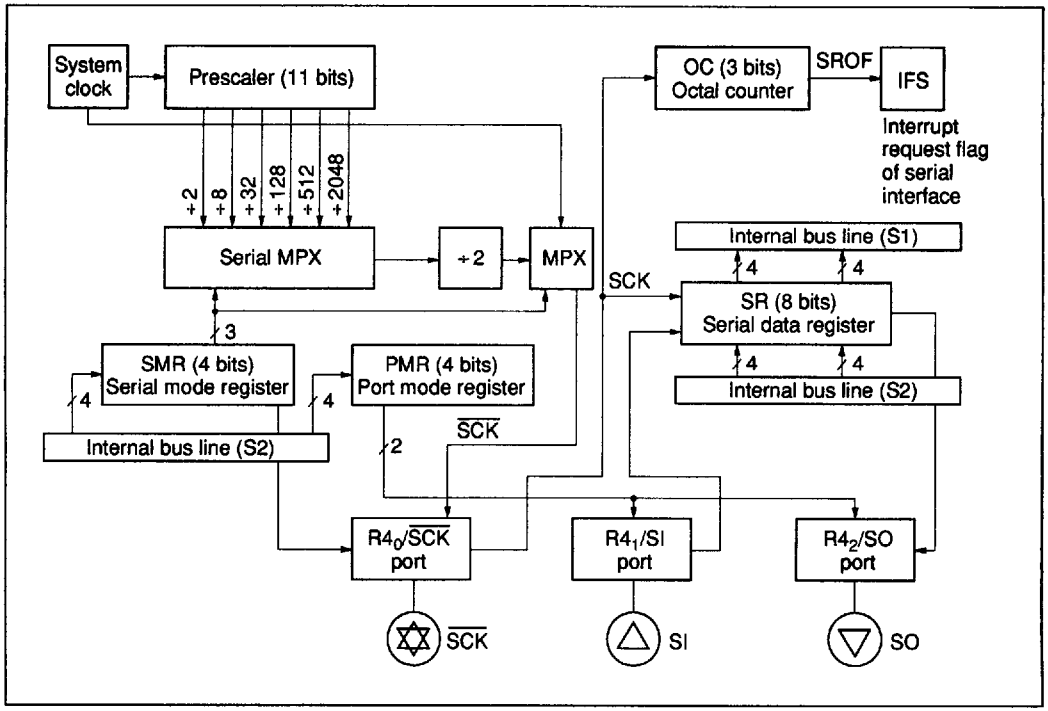


Figure 9 Serial Interface Block Diagram

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register will be output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data will be input SI pin to the serial data register, to MSB first, synchronously with the rising edge of the transmit clock. Figure 10 shows the I/O timing chart for the transmit clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Table 9 Serial Mode Register

SMR3	$R4_0/\overline{SCK}$
0	Used as $R4_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

			Transmit Clock			
SMR2	SMR1	SMR0	$R4_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
1	1	1	$\overline{SCK}$ input	External clock	—	—

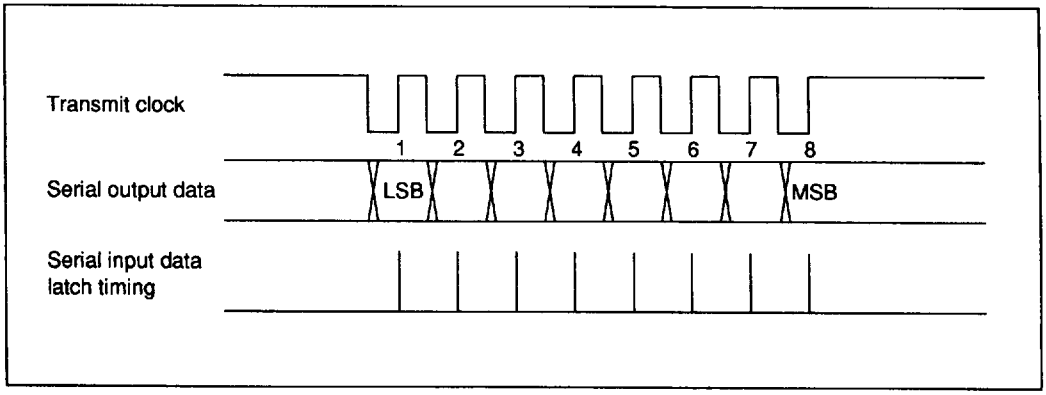


Figure 10 Serial Interface I/O Timing

Serial Interrupt Request Flag (IFS: $003, Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 10.

Serial Interrupt Mask (IMS: $003, Bit 1): The serial interrupt mask masks the interrupt request. Refer to table 11.

Selection and Change of the Operation Mode: Table 12 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register. Initialize the serial interface by the write signal to the serial mode register when the operation mode is changed.

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface is put into this state in one of two ways: either by changing the operation mode through a data change in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transmit clock is applied. If the STS instruction is executed, the serial interface shifts to the transmit clock wait state.

In transmit wait state the falling edge of the first transmit clock causes the serial interface to shift to the transfer state, while the octal counter counts up and the serial data register shifts simultaneously. If the clock continuous output mode is selected, however, the serial interface stays in the transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or by the execution of the STS instruction, so that the serial interface returns to the transmit clock wait state, and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clock.

Example of Transmit Clock Error Detection: The serial interface functions abnormally when the transmit clock is disturbed by external noise. In this case, transmit clock errors can be detected by the procedure shown in figure 12.

If more than 8 transmit clock are applied in the transmit clock wait state, the state of the serial interface shifts in the following sequence: transfer state, transmit clock wait state, and transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

Table 10 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Table 11 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 12 Serial Interface Operation Mode

SMR3	PMR1	PMR2	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

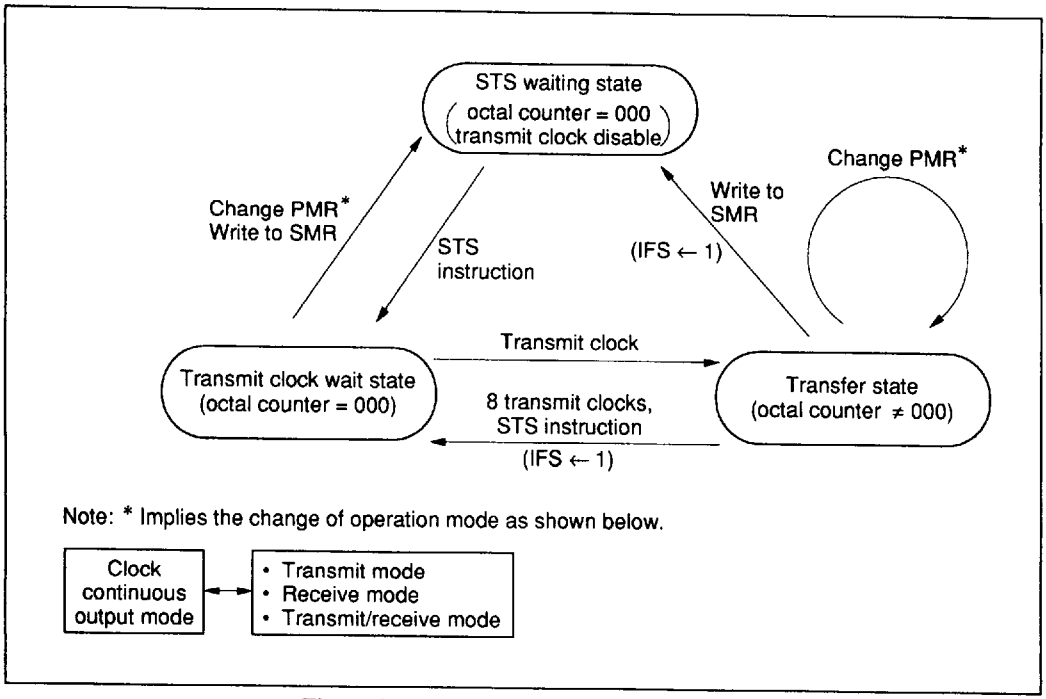


Figure 11 Serial Interface Operation State

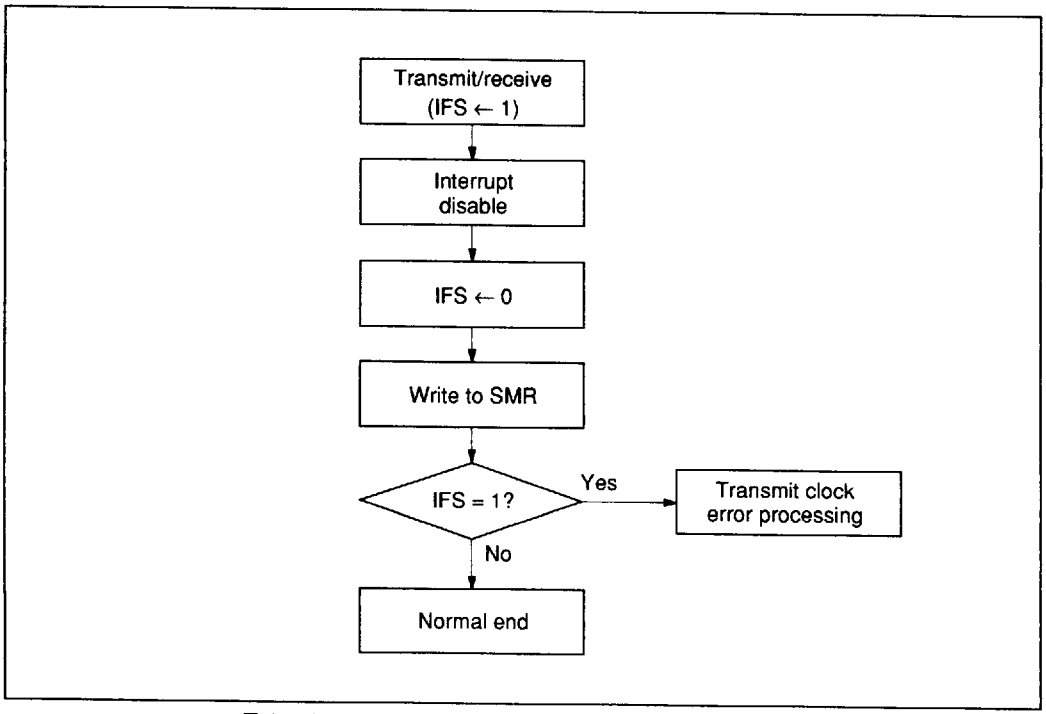


Table 12 Example of Transmit Clock Error Detection

Timers

The MCU of HMCS412C/CL/AC and HMCS414C/CL/AC contain a prescaler and a timer/counter (timer B) where as one prescaler and two timer/counters (timer A and timer B) are available on the MCU of HMCS424C/CL/AC. The functions of the prescaler and timer/counters are the same as the HMCS404C's. The timer block diagram is shown in figure 13. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up by the system clock signal as soon as the RESET input goes to logic 0. The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), and the serial mode register (SMR).

Timer A Operation (Only Applicable for HMCS424C/CL/AC): After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A counts up to \$FF, timer A is set to \$00 again, and generates an overflow output. This sets the timer A interrupt request flag (IFTA: \$001, bit 2) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input. The clock input signals to timer A are selected by timer mode register A (TMA: \$008).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

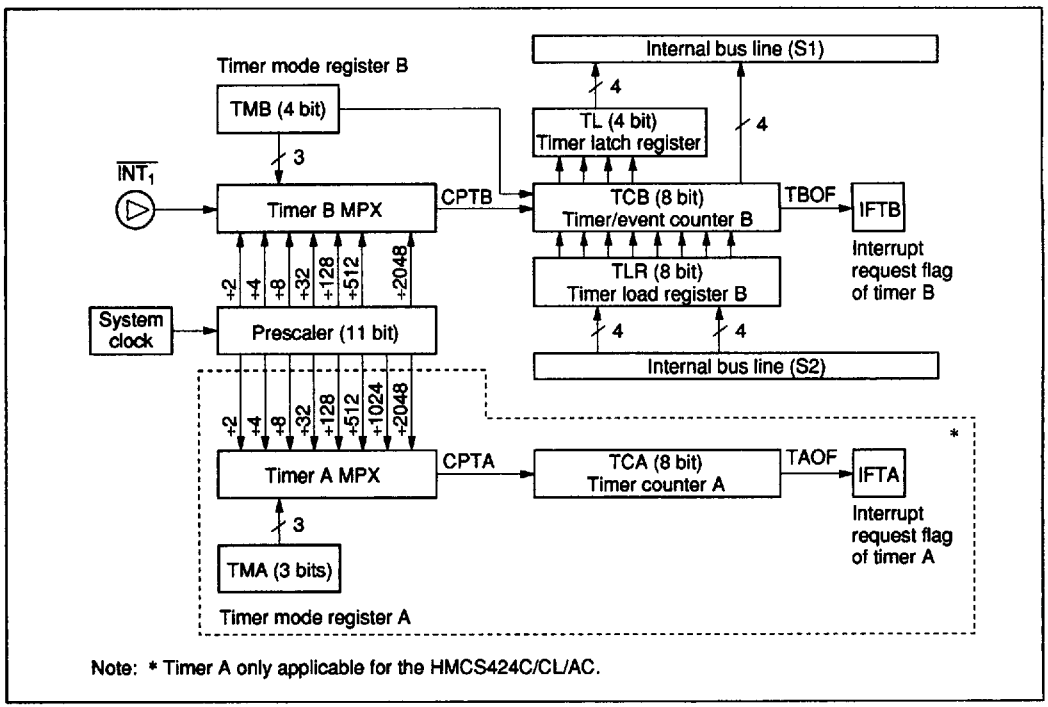


Figure 13 Timer Block Diagram

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. Then, if the auto-reload function is selected, timer B is initialized to the value of the timer load register. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set as this overflow output.

Timer Mode Register A (TMA: $008): The 3-bit write-only timer mode register A controls the prescaler divide ratio of timer A's clock input as shown in table 13.

The timer mode register A is initialized to $0 by MCU reset.

Timer Mode Register B (TMB: $009): 4-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 14. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer counter. Each has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B) (figure 2).

The timer counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Table 13 Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 14 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (external event input)

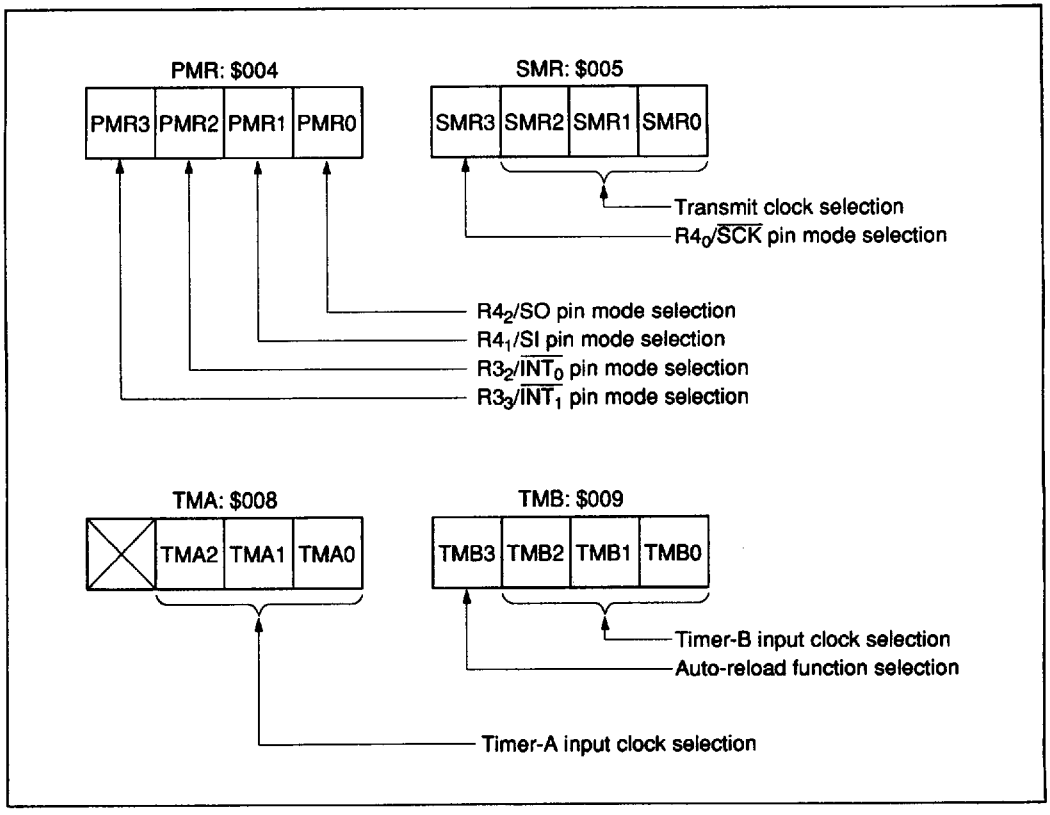


Figure 14 Mode Register Configuration and Function

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag is set by the timer A overflow output (table 15).

Timer A Interrupt Mask (IMTA: $001, Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table16).

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 17).

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 18).

Table 15 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Table 16 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 17 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Table 18 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Input/Output

The MCU has 36 I/O pins, 12 standard and 24 high voltage. One of three circuit types can be selected by the mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain). One of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, the RA_1/V_{disp} pin must be selected as V_{disp} via the mask option when at least one high-voltage pin is selected as with pull-down MOS. See table 19 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 20.

Output Circuit Operation of With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten the rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal become 0 in the stop mode, MOS (A), (B), and (C) turn off.

D Port: The I/O D port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. See table 19 as for the classification of the standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The six R ports are composed of 16 I/O pins, 4 output-only pins, and 1 input-only pin. Data is input through the LAR and LBR instructions, and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing port, while invalid data will be read from the output-only and/or non-existing ports.

The $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$ $\overline{SCK}$, SI, and SO pins, respectively. See table 19 as for the classification of standard pins, high-voltage pins, and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

High-voltage pins: Select without pull-down MOS (PMOS open drain) via the mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via the mask option and connect to GND on the printed circuit board.

$R4_0/\overline{SCK}$ and $R4_2$/SO should be set to $R4_0$ and $R4_2$ by the serial mode register and port mode register, respectively.

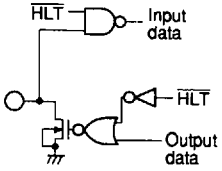
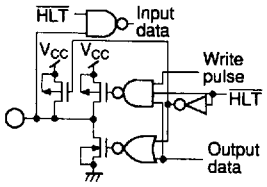
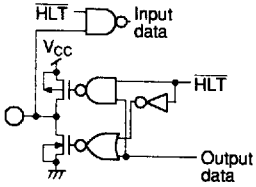
Reset

Setting the RESET pin high resets the MCU. At power-on or when cancelling the stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.

Table 21 shows the components initialized by MCU reset, and the status of each. Table 22 shows how registers recover from the stop mode.

Table 19 I/O Pin Circuit Types

Standard Pins

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Pins
I/O common pins				D_0 to D_3, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$

High Voltage Pins

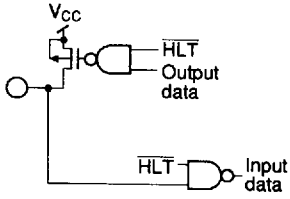
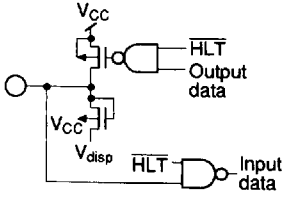
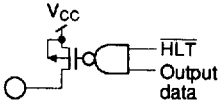
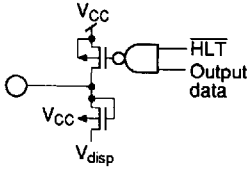
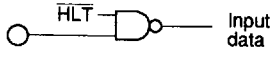
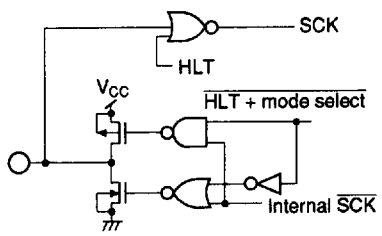
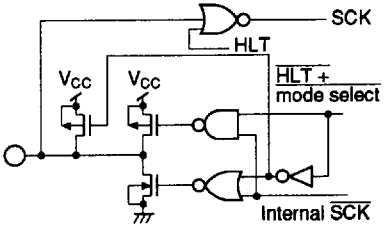
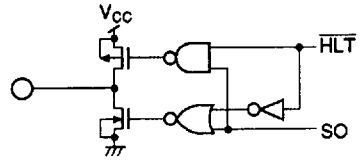
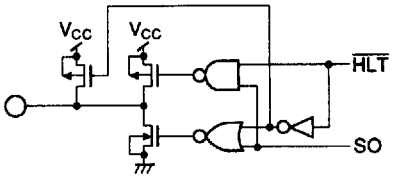
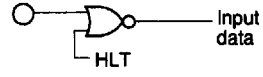
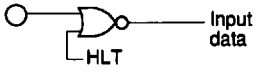
	Without Pull-Down MOS (PMOS Open Drain) (D)	With Pull-Down MOS (E)	Pins
I/O common pins			D_4 to D_{15}, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$
Output pins			$R0_0$ to $R0_3$
Input pins			RA_1

Table 19 I/O Pin Circuit Types (cont)

Standard Pins

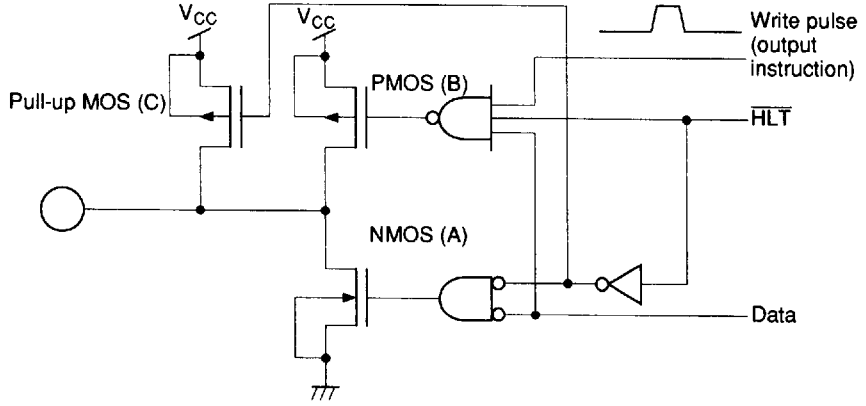
	Without Pull-Up MOS (NMOS Open Drain) or CMOS (A or C)	With Pull-Up MOS (B)	Pins
I/O common pins			SCK* (output mode)
Output pins			SO*
Input pins			INT0, INT1, SI*, SCK* (input mode

Note: In the stop mode, HLT is 0, HLT is 1, and I/O pins are in high impedance.

* Only applicable for the HMCS424C/CL/AC. If the MCU is interrupted by the serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 20 Data Input from Common Input/Output Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0



MOS Buffer	On-Resistance Value: HMCS412C, HMCS412AC, HMCS414C, HMCS414AC, HMCS424C, HMCS424AC	On-Resistance Value: HMCS412CL, HMCS414CL, HMCS424CL
A	Approx. 250 Ω	Approx. 1 kΩ
B	Approx. 1 kΩ	Approx. 1.7 kΩ
C	Approx. 30 kΩ to 160 kΩ (V_{CC} = 5 V)	Approx. 60 kΩ to 1 MΩ (V_{CC} = 3 V) Approx. 30 kΩ to 160 kΩ (V_{CC} = 5 V)

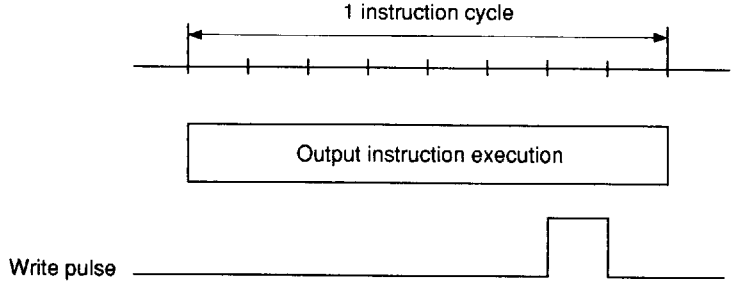


Figure 15 Output Circuit Operation of With Pull-Up MOS Standard Pins

Table 21 Initial Values after MCU Reset

Item			Initial Value	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address
Status flag (ST)			1	Enable branching with conditional branch instructions
Stack pointer (SP)			$3FF	Stack level is 0
I/O pins, output register	Standard pins	Without pull-up MOS	1	Enable input
		With pull-up MOS	1	Enable input
		CMOS	1	—
	High voltage pins	Without pull-down MOS	0	Enable input
		With pull-down MOS	0	Enable input
Interrupt flags and mask	Interrupt enable flag (IE)		0	Inhibit all interrupts
	Interrupt request flag (IF)		0	No interrupt request
	Interrupt mask (IM)		1	Mask interrupt request
Mode registers	Posrt mode register (PMR)		0000	See Port Mode Register section
	Serial mode register* (SMR)		0000	See Serial Mode Register section
	Timer mode register A* (TMA)		000	See Timer Mode Register A section
	Timer mode register B (TMB)		0000	See Timer Mode Register B section
Timer/counters	Prescaler		$000	—
	Timer counter A* (TCA)		$00	—
	Timer counter B (TCB)		$00	—
	Timer load register (TLR)		$00	—
	Octal counter*		000	—

Note: * Only applicable for the HMCS424C/CL/AC.

Table 22 Initial Values after Cancelling Stop and Other Modes by Reset

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX registers	(X/SPX)		
Y/SPY registers	(Y/SPY)		
Serial data register*	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	The contents of RAM before MCU reset are not retained. It is necessary to initialize them by software.

Note: * Only applicable for the HMCS424C/CL/AC.

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. Through the mask option the oscillator type can be selected from the following: crystal oscillator, ceramic oscillator, or resistor oscillator. Refer to table 24 for oscillator selection. In addition, see figure 17 for the layout of the crystal or ceramic oscillator. In all cases, an external clock operation is available. Three divide ratios, 1/16, 1/8, and 1/4, are selectable via the mask option (table 23).

Table 23 Internal Oscillation Circuit Mask Option

	Oscillation			Divider		
Family Name	**Crystal**	**Ceramic**	**Resistor**	**1/16**	**1/8**	**1/4**
HMCS412C	Available	Available	Available	—	Available	Available
HMCS412CL	Available	Available	—	Available	Available	—
HMCS412AC	Available	Available	—	—	—	Available
HMCS414C	Available	Available	Available	—	Available	Available
HMCS414CL	Available	Available	—	Available	Available	—
HMCS414AC	Available	Available	—	—	—	Available
HMCS424C	Available	Available	—	—	Available	Available
HMCS424CL	Available	Available	—	—	Available	—
HMCS424AC	Available	Available	—	—	—	Available

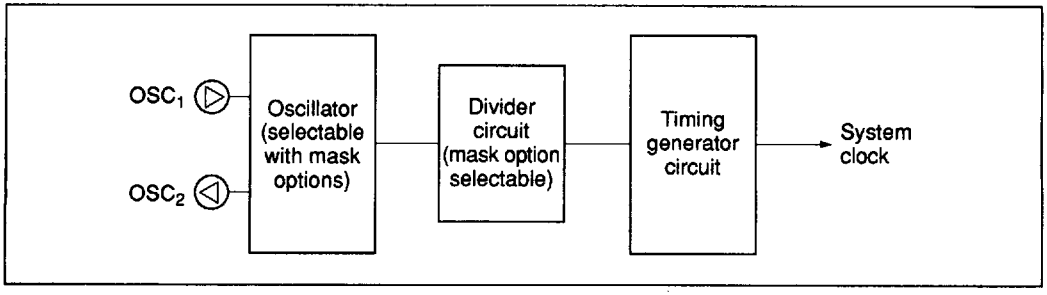


Figure 16 Internal Oscillator Circuit

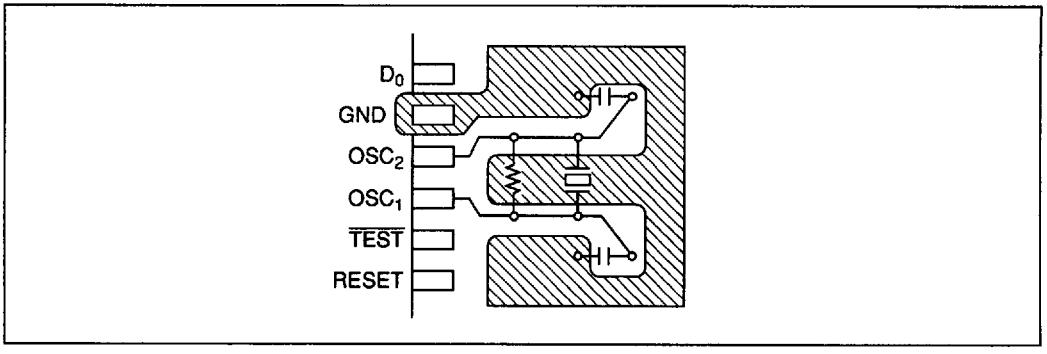
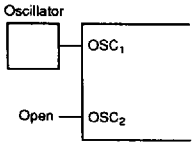
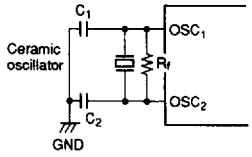
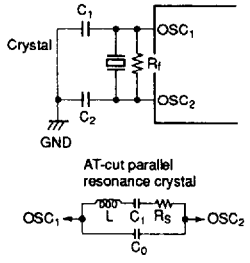
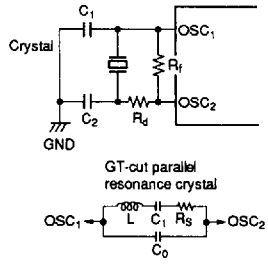
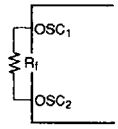


Figure 17 Layout of Crystal and Ceramic Oscillator

Table 24 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants HMCS424C	HMCS424CL	HMCS424AC
External clock operation				
Ceramic oscillator		Ceramic oscillator CSA 4.00MG CSA 2.000MK (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%	Ceramic oscillator CSA 2.000MK (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%	Ceramic oscillator CSA 4.00MG (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal oscillator		R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent circuit shown at bottom left C_0: 7 pF max. R_S: 100 Ω max. f: 1.0 MHz to 4.5 MHz	—	R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent circuit shown at bottom left C_0: 7 pF max. R_S: 100 Ω max. f: 1.0 MHz to 4.5 MHz
		—	R_f: 2 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent circuit shown at bottom left C_0: 7 pF max. R_S: 100 Ω max. f: 1.0 MHz to 2.25 MHz	—
Resistor oscillator		R_f: 18 kΩ ±1%	—	—

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic oscillator manufacture. The circuit parameters are affected by the crystal, ceramic resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic oscillator manufacture to determine the circuit parameters.
2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator (figure 17).
3. Resistor oscillator can be used for HMCS412C and HMCS414C.

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 25). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing the SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active, and the interrupts and timer/counters remain working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 25 Low-Power Dissipation Modes Function

Low-Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Registers, Flags	Interrupts Function	RAM	Input/ Output Pins	Timer/ Counters, Serial Interface	Cancellation Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*3	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	Reset*1	Stop	Retained	High impedance*2	Stop	RESET input

Notes: 1. The MCU recovers from the stop mode by RESET input. Refer to table 21 for the contents of the flag and registers.
2. A high-voltage pin of with pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. With pull-down MOS on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is in addition to the current dissipation in the stop mode (I_{STOP}).
3. When an I/O circuit is active, an I/O current may flow, depending on the state of the I/O pin in standby mode. This is in addition to the current dissipation in standby mode.

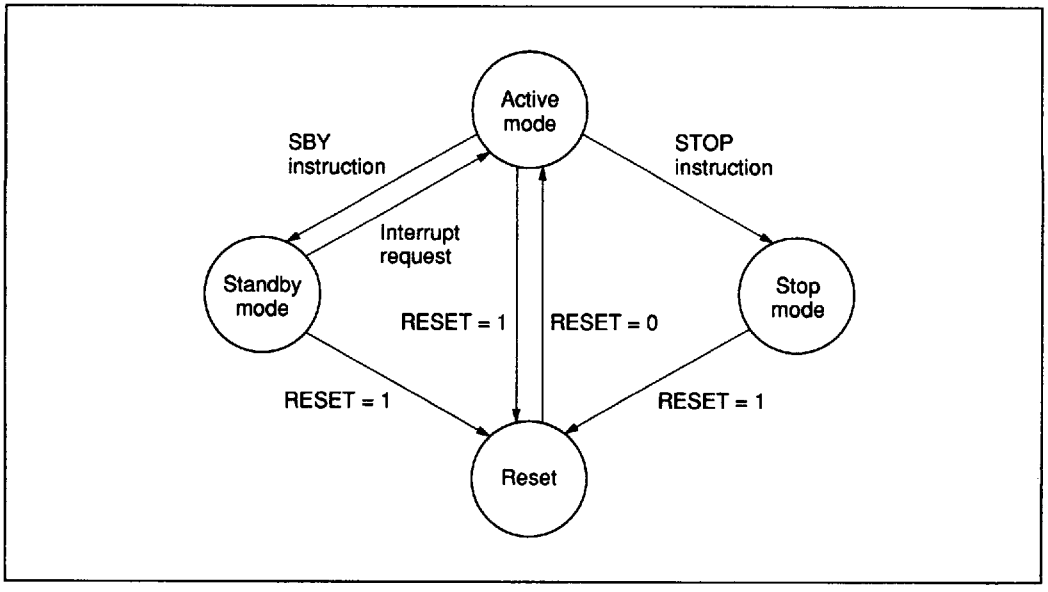


Figure 18 MCU Operation Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 19 shows the flowchart of the standby mode.

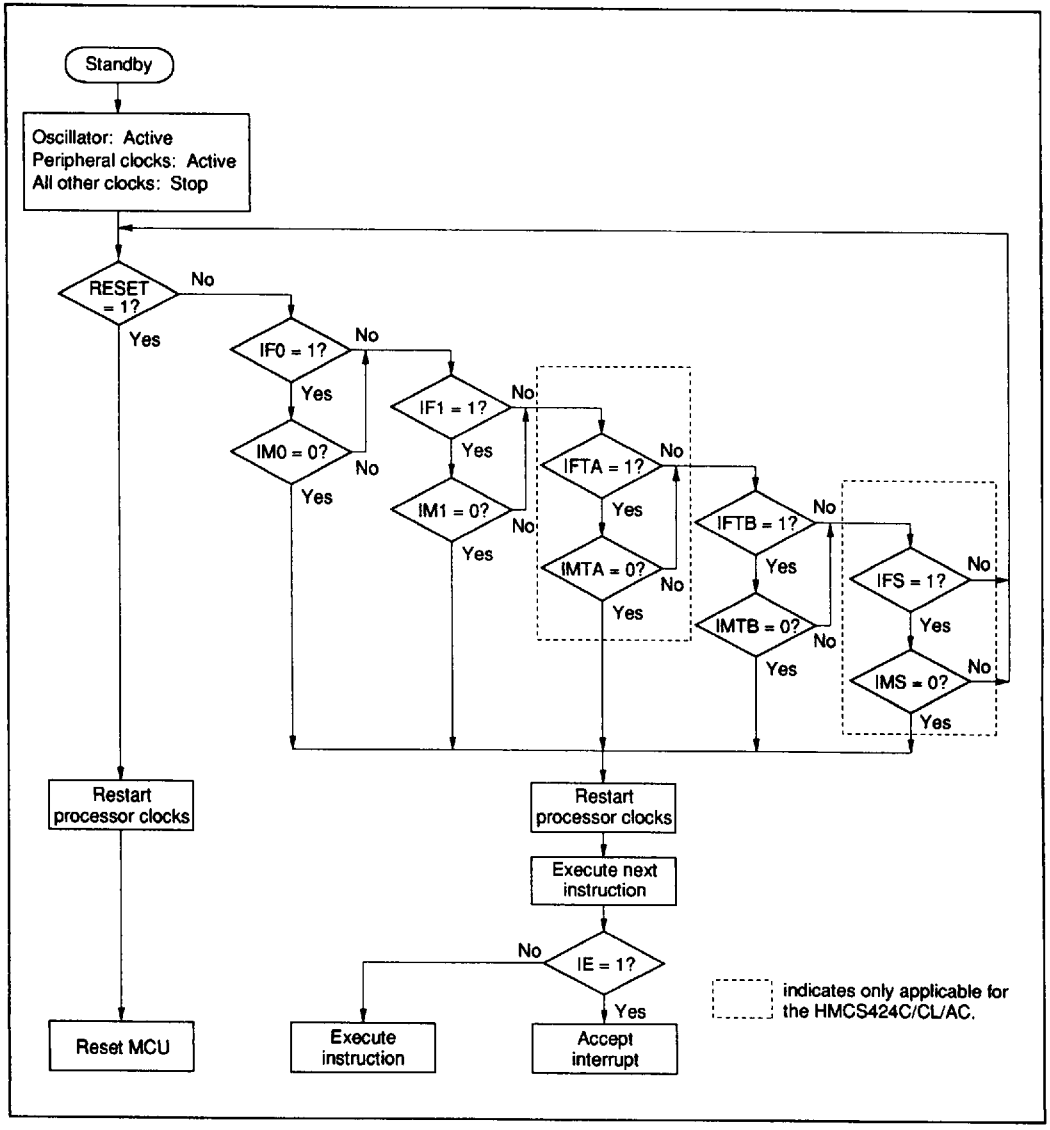


Figure 19 MCU Operating Flowchart in Standby Mode

Stop Mode: Executing the STOP instruction bring the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, RESET input must be applied for at least t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After the stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register Y/SPY registers, and carry flag will not retain their contents.

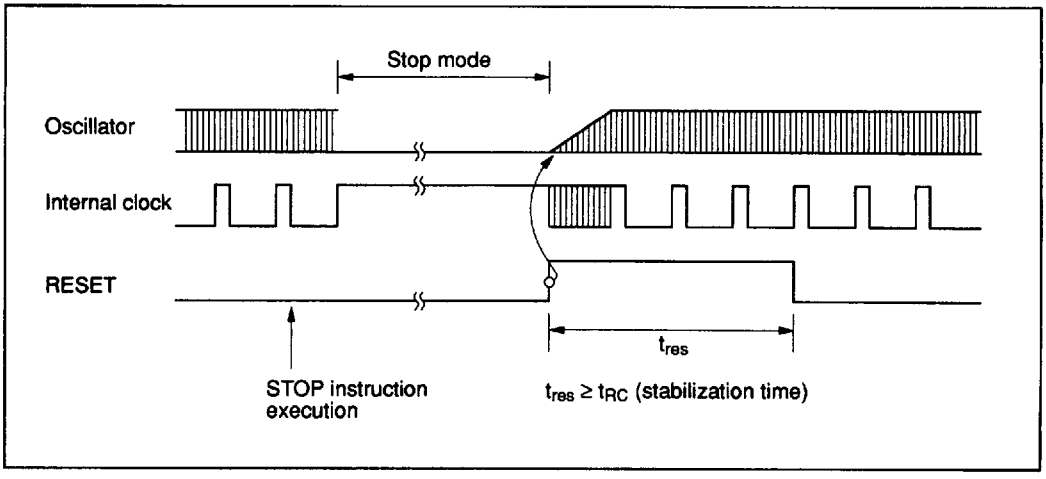


Figure 20 Timing of Stop Mode Cancellation

Addressing Modes

RAM Addressing Modes

As shown in figure 21, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits total) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the world (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 22.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address on the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 23), executing it transfer the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000 to $003F. When the CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bits immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 24). When bit 8 in the ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

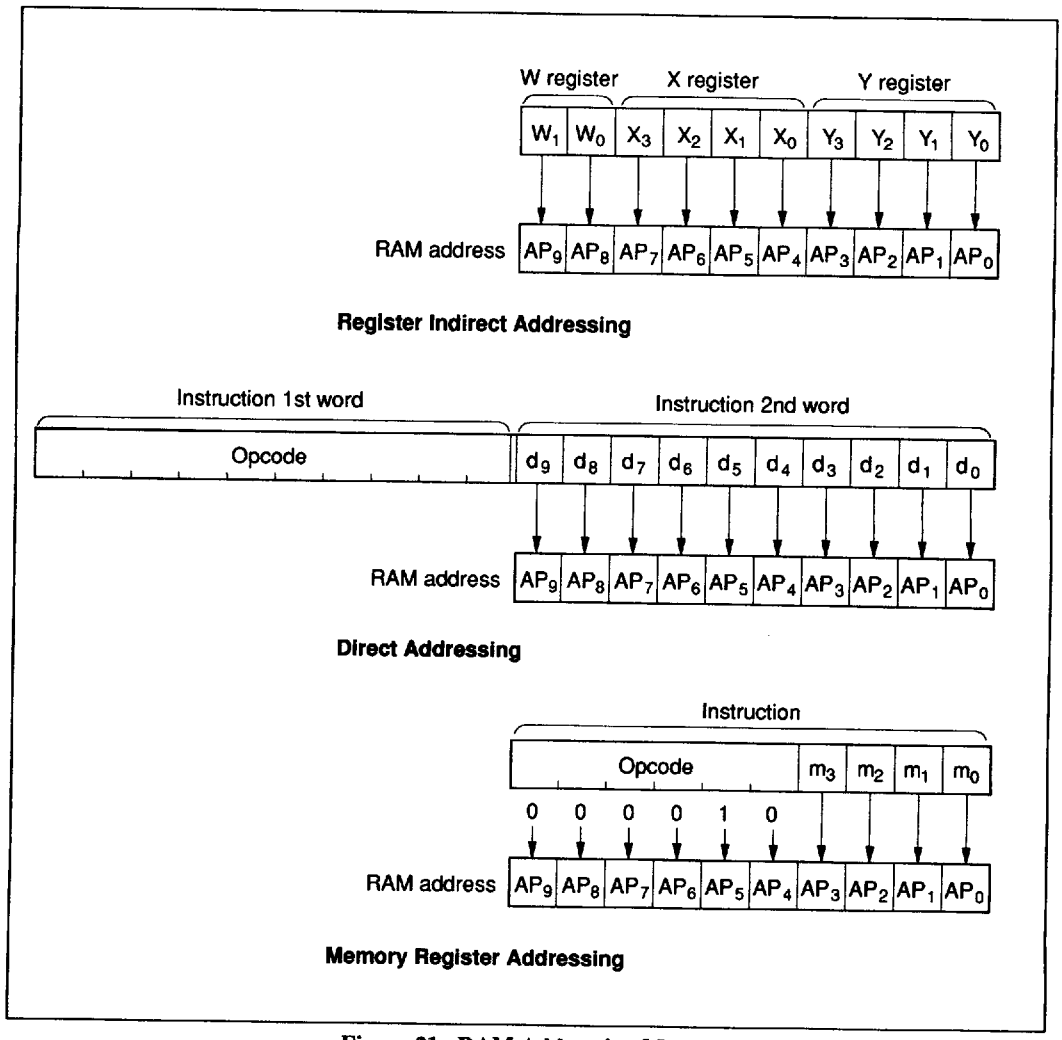


Figure 21 RAM Addressing Modes

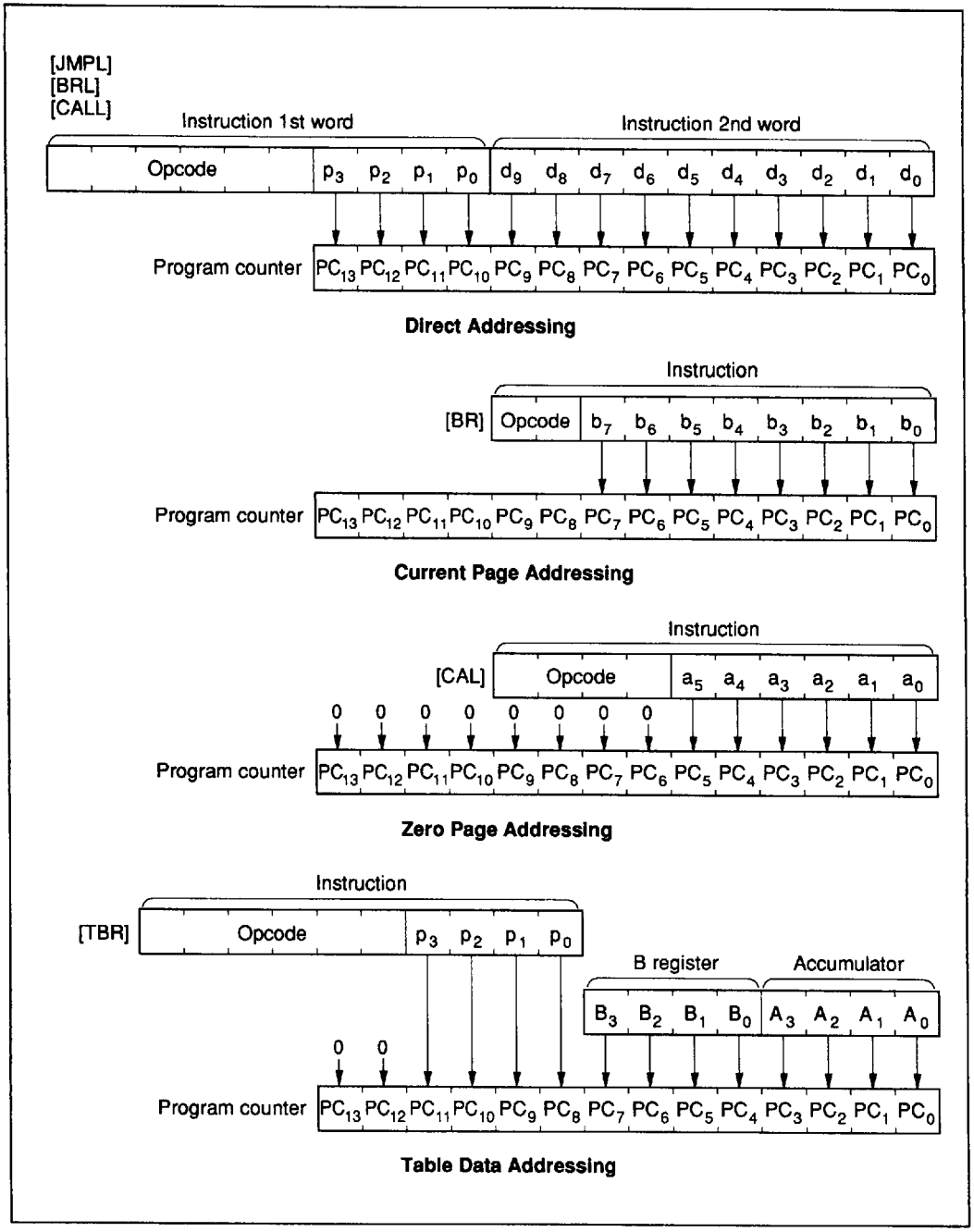


Figure 22 ROM Addressing Modes

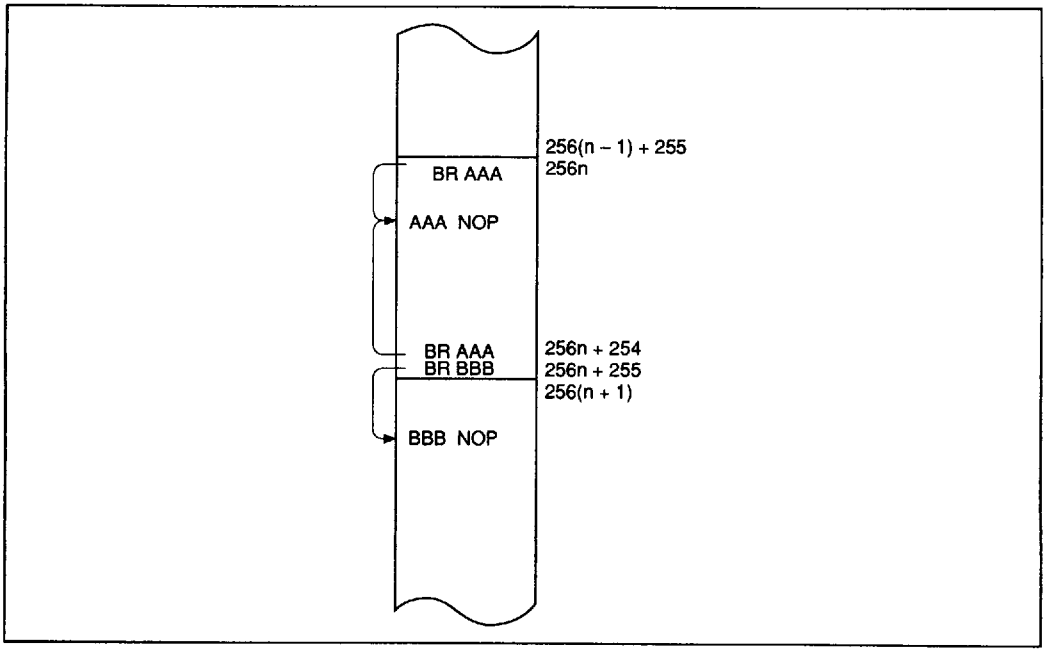


Figure 23 BR Instruction Branch Destination on a Page Boundary

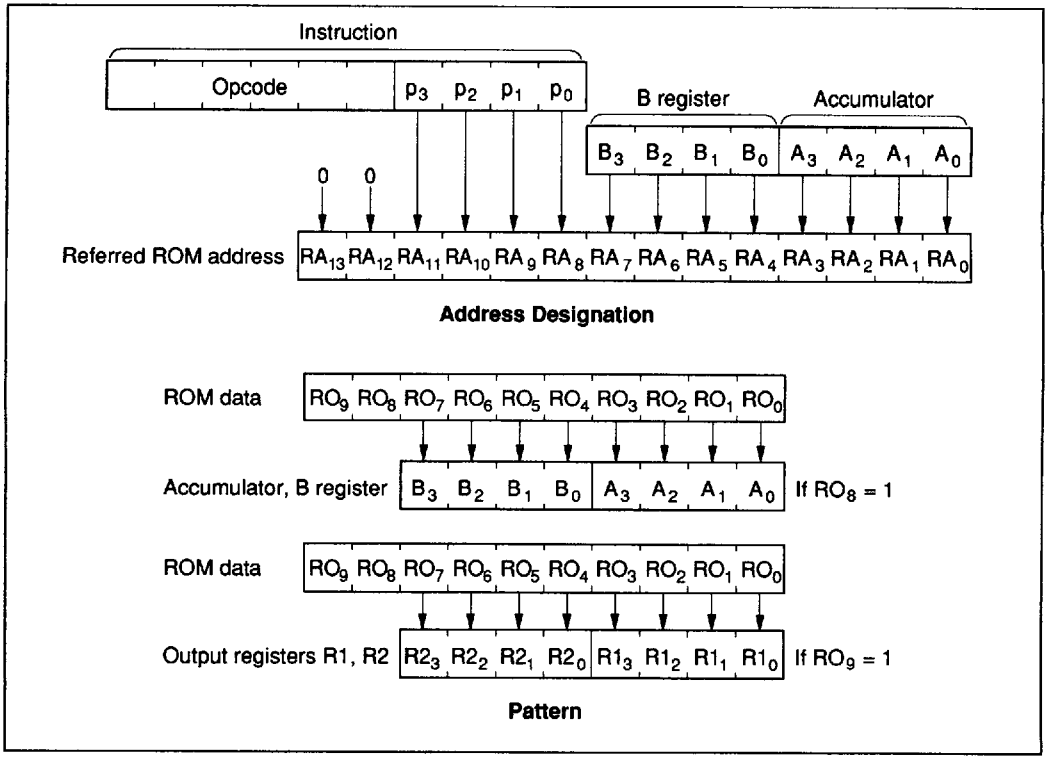


Figure 24 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	−0.3 to +7.0	V	
Pin voltage	VT	−0.3 to V_{CC} + 0.3	V	1
		V_{CC} − 45 to V_{CC} + 0.3	V	2
Total permissible input current	ΣI_o	25 (25)	mA	3
Maximum input current	I_o	15 (15)	mA	5, 6
Maximum output current	$-I_o$	4 (2)	mA	6, 7, 10
		6 (3)	mA	7, 8, 10
		30 (15)	mA	7, 9, 10
Total permissible output current	$-\Sigma I_o$	85 (100)	mA	4, 10
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
All voltages are with respect to GND.

1. Standard pins.
2. High-voltage pins.
3. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
4. Total permissible output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
5. Maximum output current is the maximum amount of input current from each I/O pin to GND.
6. D_0 to D_3, R3, and R4.
7. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
8. R0 to R2.
9. D_4 to D_{14}.
10. $-\Sigma I_o$ = 100 mA if $-I_o$ is equal to or less than 2 mA, 3 mA, or 15 mA.

HMCS412C/CL/AC Electrical Characteristics

DC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS412C: V_{CC} = 3.5 V to 6 V, HMCS412CL: V_{CC} = 2.5 V to 6 V, HMCS412AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	$0.8V_{CC}$	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	V_{CC} + 0.3	V	HMCS412C/AC	
			V_{CC} – 0.3	V_{CC} + 0.3	V	HMCS412CL	
Input low voltage	V_{IL}	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	–0.3	$0.2V_{CC}$	V		
		OSC_1	–0.3	0.5	V	HMCS412C/AC	
			–0.3	0.3	V	HMCS412CL	
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, OSC_1	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	1.8	mA	HMCS412C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷ 4	2, 5
			—	2.2	mA	HMCS412C: V_{CC} = 5 V; R_f = 18 kΩ ±1%, ÷ 8	2, 5
			—	0.8	mA	HMCS412CL: V_{CC} = 3 V; f_{OSC} = 4 MHz, ÷ 16, or f_{OSC} = 2 MHz, ÷ 8	2, 5
			—	3.0	mA	HMCS412AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	1.0	mA	HMCS412C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷ 4	3, 5
			—	1.3	mA	HMCS412C: V_{CC} = 5 V; R_f = 18 kΩ ±1%, ÷ 8	3, 5
			—	0.5	mA	HMCS412CL: V_{CC} = 3 V; f_{OSC} = 4 MHz, ÷ 16, or f_{OSC} = 2 MHz, ÷ 8	3, 5
			—	1.4	mA	HMCS412AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}; V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	V		

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3, R4: V_{CC}
   - D_4 to D_{14}, R0 to R2, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3, R4: V_{CC}
   - D_4 to D_{14}, R0 to R2, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHZ, estimate the current dissipation as follows:
   HMCS412C/AC: Maximum value at x MHz = (x/4) × (max. value at 4 MHz)
   HMCS412CL: Maximum value at x MHz = (x/2) × (max. value at 2 MHz)

Input/Output Characteristics for Standard Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS412C: V_{CC} = 3.5 V to 6 V, HMCS412CL: V_{CC} = 2.5 V to 6 V, HMCS412AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, $R3_0$, $R3_1$, R4	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, $R3_0$, $R3_1$, R4	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0 to D_3, $R3_0$, $R3_1$, R4	V_{CC} – 1.0	—	—	V	HMCS412C/AC: $-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, $R3_0$, $R3_1$, R4	V_{CC} – 0.5	—	—	V	HMCS412C/AC: $-I_{OH}$ = 0.5 mA HMCS412CL: $-I_{OH}$ = 0.3 mA	1
Output low voltage	V_{OL}	D_0 to D_3, $R3_0$, $R3_1$, R4	—	—	0.4	V	HMCS412C/AC: I_{OL} = 1.6 mA HMCS412CL: I_{OH} = 0.4 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, $R3_0$, $R3_1$, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, $R3_0$, $R3_1$, R4	30	60	150	µA	V_{CC} = 5 V, V_{in} = 0 V	3
		D_0 to D_3, $R3_0$, $R3_1$, R4	3	15	50	µA	HMCS412CL only: V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High-Voltage Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS412C: V_{CC} = 3.5 V to 6 V, HMCS412CL: V_{CC} = 2.5 V to 6 V, HMCS412AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{14}, R1, R2, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{14}, R1, R2, RA_1	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{14}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, HMCS412C/CL: V_{CC} = 5 V ± 20% HMCS412AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, HMCS412C/CL: V_{CC} = 5 V ±20% HMCS412AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 1.0	—	—	V	HMCS412C/AC: $-I_{OH}$ = 4 mA HMCS412CL: $-I_{OH}$ = 2.5 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, HMCS412C/CL: V_{CC} = 5 V ±20% HMCS412AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 2 mA, HMCS412C/CL: V_{CC} = 5 V ±20% HMCS412AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 1.0	—	—	V	HMCS412C/AC: $-I_{OH}$ = 0.8 mA HMCS412CL: $-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_4 to D_{14}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{14}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\lvert I_{IL} \rvert$	D_4 to D_{14}, R0 to R2, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{14}, R0 to R2, RA_1	125	250	600	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS412C: V_{CC} = 3.5 V to 6 V, HMCS412CL: V_{CC} = 2.5 V to 6 V, HMCS412AC: V_{CC} = 4.5 V to 6 V)

Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Crystal or ceramic oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	HMCS412C: divide-by-8	
				0.2	2	2.25	MHz	HMCS412C: divide-by-4	
				0.8	4	4.5	MHz	HMCS412CL: divide-by-16	
				0.4	2	2.25	MHz	HMCS412CL: divide-by-8	
				0.2	4	4.5	MHz	HMCS412AC: divide-by-4	
	Instruction cycle time	t_{cyc}		1.78	2	20	µs	HMCS412C	
				3.55	4	20	µs	HMCS412CL	
				0.89	1	20	µs	HMCS412AC	
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HMCS412C/AC	1
				—	—	60	ms	HMCS412CL	1
Resistor oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1.5	3	4.5	MHz	HMCS412C: R_f = 18 kΩ ±1%	
	Instruction cycle time	t_{cyc}		1.78	2.66	5.33	µs	HMCS412C: R_f = 18 kΩ ±1%	
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	HMCS412C: R_f = 18 kΩ ±1%	1
	Between pin capacitance	C_{Rf}	OSC_1, OSC_2	—	—	1	pF	HMCS412C	
External clock high and low widths		t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	HMCS412C: divide-by-8 HMCS412CL: divide-by-16 HMCS412AC: divide-by-4	2
				203	—	—	ns	HMCS412C: divide-by-4 HMCS412CL: divide-by-8	2

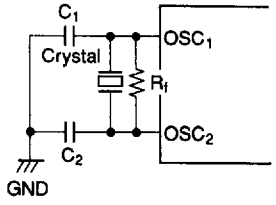
AC Characteristics (GND = 0 V, Vdisp = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS412C: V_{CC} = 3.5 V to 6 V, HMCS412CL: V_{CC} = 2.5 V to 6 V, HMCS412AC: V_{CC} = 4.5 V to 6 V) (cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	20	ms	HMCS412C/AC	4
			—	—	15	ms	HMCS412CL	4

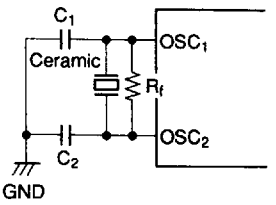
Notes: 1. The oscillator stabilization time is period from when V_{CC} reaches its minimum allowable voltage (HMCS412C: 3.5 V, HMCS412CL: 2.5 V, HMCS412AC: 4.5 V) at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. Since t_{RC} depends on the crystal or ceramic circuit constant and stray capacitance, consult with the crystal or ceramic oscillator manufacturer when designing the reset circuit. (See figure 25.)

2. See figure 26.
3. See figure 27.
4. See figure 28.

HMCS412C/AC

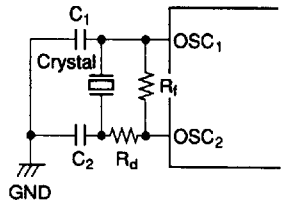


Crystal: 4.194304 MHz
NC-18C (Nihon Denpa Kogyo)
R_f = 1 MΩ ±20%,
$C_1 = C_2$ = 22 pF ±20%

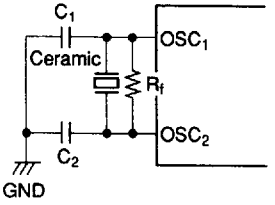


Ceramic: CSA4.00 MG (Murata)
R_f = 1 MΩ ±20%,
$C_1 = C_2$ = 30 pF ±20%

HMCS412CL



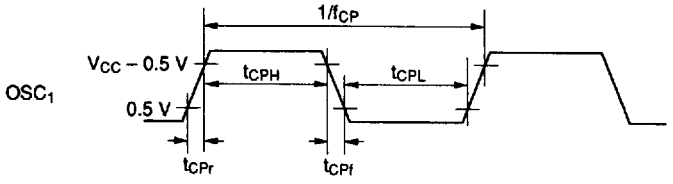
Crystal: 2.097152 MHz
DS-MGQ 308 (Seiko)
R_f = 1 MΩ ±20%, R_d = 2.2 kΩ ±20%
$C_1 = C_2$ = 10 pF ±20%



Ceramic: CSA 2.000MK (Murata)
R_f = 1 MΩ ±20%,
$C_1 = C_2$ = 30 pF ±20%

Figure 25 Oscillation Circuits

HMCS412C/AC



HMCS412CL

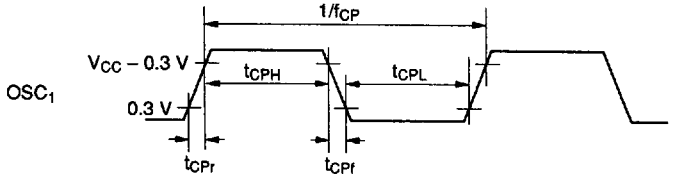


Figure 26 Oscillator Timing

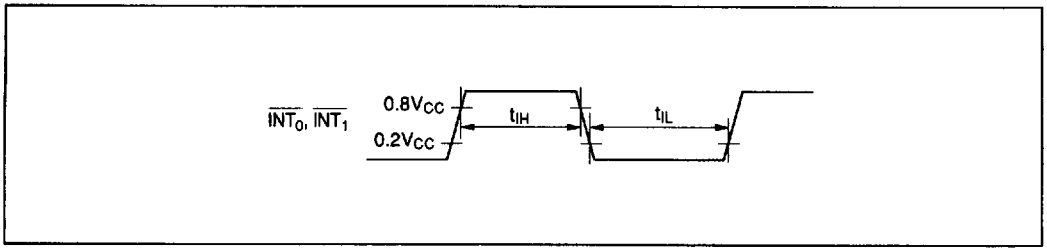


Figure 27 Interrupt Timing

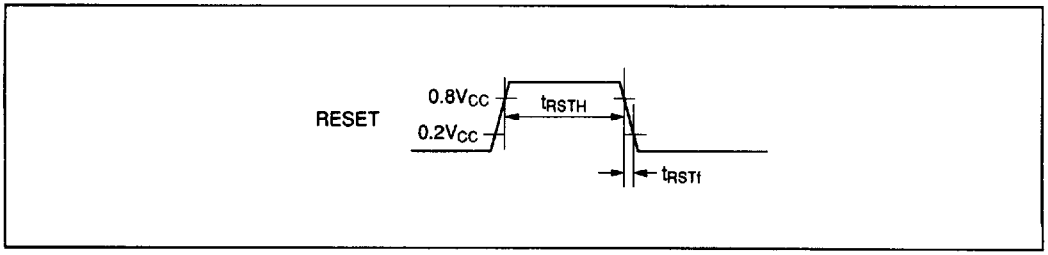


Figure 28 Reset Timing

HMCS412C/CL/AC
Option List

Please check off the appropriate applications and enter the necessary information.

5-V operation:	☐ HMCS412C (HD404240)
3-V operation:	☐ HMCS412CL (HD40L4240)
High speed operation:	☐ HMCS412AC (HD40A4240)

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

1. I/O option

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (cannot be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

Note: I/O options masked by ▨ are not available.

Pin	I/O		I/O option				
			A	B	C	D	E
D0	Standard pins	I/O				▨	▨
D1		I/O				▨	▨
D2		I/O				▨	▨
D3		I/O				▨	▨
D4	High voltage pins	I/O	▨	▨	▨		
D5		I/O	▨	▨	▨		
D6		I/O	▨	▨	▨		
D7		I/O	▨	▨	▨		
D8		I/O	▨	▨	▨		
D9		I/O	▨	▨	▨		
D10		I/O	▨	▨	▨		
D11		I/O	▨	▨	▨		
D12		I/O	▨	▨	▨		
D13		I/O	▨	▨	▨		
D14		I/O	▨	▨	▨		

Pin		I/O		I/O option				
				A	B	C	D	E
R0	R00	High voltage pins	O	▨	▨	▨		
	R01		O	▨	▨	▨		
	R02		O	▨	▨	▨		
	R03		O	▨	▨	▨		
R1	R10		I/O	▨	▨	▨		
	R11		I/O	▨	▨	▨		
	R12		I/O	▨	▨	▨		
	R13		I/O	▨	▨	▨		
R2	R20		I/O	▨	▨	▨		
	R21		I/O	▨	▨	▨		
	R22		I/O	▨	▨	▨		
	R23		I/O	▨	▨	▨		
R3	R30	Standard pins	I/O				▨	▨
	R31		I/O				▨	▨
	R32		I/O				▨	▨
	R33		I/O				▨	▨
R4	R40		I/O				▨	▨
	R41		I/O				▨	▨
	R42		I/O				▨	▨
	R43		I/O				▨	▨
RA	RA1	High voltage pin	I	Use checklist RA1/Vdisp				

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (Div)

Divider	4	8	16
HMCS412C	☐	☐	
HMCS412CL		☐	☐
HMCS412AC	☐		

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. Oscillator (CPG option)

☐ HMCS412C (5-V operation)	☐ HMCS412CL (3-V operation)	☐ HMCS412AC (high speed operation)
☐ Resistor (Rf = 18 kΩ ±1%, ÷ 8)		
☐ Ceramic oscillator	☐ Ceramic oscillator	☐ Ceramic oscillator
☐ Crystal oscillator	☐ Crystal oscillator	☐ Crystal oscillator
☐ External clock	☐ External clock	☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-42
☐ DP-42S
☐ FP-44A

HMCS414C/CL/AC Electrical Characteristics

DC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS414C: V_{CC} = 3.5 V to 6 V, HMCS414CL: V_{CC} = 2.5 V to 6 V, HMCS414AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	$0.8V_{CC}$	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	V_{CC} + 0.3	V	HMCS414C/AC	
			V_{CC} – 0.3	V_{CC} + 0.3	V	HMCS414CL	
Input low voltage	V_{IL}	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	–0.3	$0.2V_{CC}$	V		
		OSC_1	–0.3	0.5	V	HMCS414C/AC	
			–0.3	0.3	V	HMCS414CL	
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, OSC_1	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	1.8	mA	HMCS412C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷ 4	2, 5
			—	2.2	mA	HMCS412C: V_{CC} = 5 V; R_f = 18 kΩ ±1%, ÷ 8	2, 5
			—	0.8	mA	HMCS414CL: V_{CC} = 3V; f_{OSC} = 4 MHz, ÷ 16, or f_{OSC} = 2 MHz, ÷ 8	2, 5
			—	3.0	mA	HMCS414AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	1.0	mA	HMCS412C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷ 4	3, 5
			—	1.3	mA	HMCS412C: V_{CC} = 5 V; R_f = 18 kΩ ±1%, ÷ 8	3, 5
			—	0.5	mA	HMCS414CL: V_{CC} = 3 V; f_{OSC} = 4 MHz, ÷ 16, or f_{OSC} = 2 MHz, ÷ 8	3, 5
			—	1.4	mA	HMCS414AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}; V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	V		

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3, R4: V_{CC}
   - D_4 to D_{14}, R0 to R2, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3, R4: V_{CC}
   - D_4 to D_{14}, R0 to R2, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHZ, estimate the current dissipation as follows:
   HMCS414C/AC; Maximum value at x MHz = (x/4) × (max. value at 4 MHz)
   HMCS414CL; Maximum value at x MHz = (x/2) × (max. value at 2 MHz)

Input/Output Characteristics for Standard Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS414C: V_{CC} = 3.5 V to 6 V, HMCS414CL: V_{CC} = 2.5 V to 6 V, HMCS414AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, $R3_0$, $R3_1$, R4	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, $R3_0$, $R3_1$, R4	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_3, $R3_0$, $R3_1$, R4	V_{CC} – 1.0	—	—	V	HMCS414C/AC: $-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, $R3_0$, $R3_1$, R4	V_{CC} – 0.5	—	—	V	HMCS414C/AC: $-I_{OH}$ = 0.5 mA; HMCS414CL: $-I_{OH}$ = 0.3 mA	1
Output low voltage	V_{OL}	D_0 to D_3, $R3_0$, $R3_1$, R4	—	—	0.4	V	HMCS414C/AC: I_{OL} = 1.6 mA HMCS414CL: I_{OH} = 0.4 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, $R3_0$, $R3_1$, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, $R3_0$, $R3_1$, R4	30	60	150	µA	V_{CC} = 5 V, V_{in} = 0 V	3
		D_0 to D_3, $R3_0$, $R3_1$, R4	3	15	50	µ A	HMCS414CL only: V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High-Voltage Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS414C: V_{CC} = 3.5 V to 6 V, HMCS414CL: V_{CC} = 2.5 V to 6 V, HMCS414AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{14}, R1, R2, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{14}, R1, R2, RA_1	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{14}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, HMCS414C/CL: V_{CC} = 5 V ± 20% HMCS414AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, HMCS414C/CL: V_{CC} = 5 V ±20% HMCS414AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 1.0	—	—	V	HMCS414C/AC: $-I_{OH}$ = 4 mA HMCS414CL: $-I_{OH}$ = 2.5 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, HMCS414C/CL: V_{CC} = 5 V ±20% HMCS414AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 2 mA, HMCS414C/CL: V_{CC} = 5 V ±20% HMCS414AC: V_{CC} = 4.5 V to 6 V	
			V_{CC} – 1.0	—	—	V	HMCS414C/AC: $-I_{OH}$ = 0.8 mA HMCS414CL: $-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_4 to D_{14}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{14}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\lvert I_{IL} \rvert$	D_4 to D_{14}, R0 to R2, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{14}, R0 to R2, RA_1	125	250	600	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS414C: V_{CC} = 3.5 V to 6 V, HMCS414CL: V_{CC} = 2.5 V to 6 V, HMCS414AC: V_{CC} = 4.5 V to 6 V)

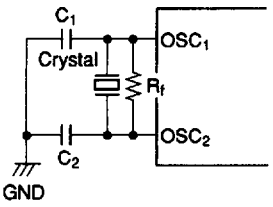
Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Crystal or ceramic oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	HMCS414C: divide-by-8	
				0.2	2	2.25	MHz	HMCS414C: divide-by-4	
				0.8	4	4.5	MHz	HMCS414CL: divide-by-16	
				0.4	2	2.25	MHz	HMCS414CL: divide-by-8	
				0.2	4	4.5	MHz	HMCS414AC: divide-by-4	
	Instruction cycle time	t_{cyc}		1.78	2	20	µs	HMCS414C	
				3.55	4	20	µs	HMCS414CL	
				0.89	1	20	µs	HMCS414AC	
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HMCS414C/AC	1
				—	—	60	ms	HMCS414CL	1
Resistor oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1.5	3	4.5	MHz	HMCS414C: R_f = 18 kΩ ±1%	
	Instruction cycle time	t_{cyc}		1.78	2.66	5.33	µs	HMCS414C: R_f = 18 kΩ ±1%	
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	HMCS414C: R_f = 18 kΩ ±1%	1
	Between pin capacitance	C_{Rf}	OSC_1, OSC_2	—	—	1	pF	HMCS414C	
External clock high and low widths		t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	HMCS414C: divide-by-8 HMCS414CL: divide-by-16 HMCS414AC: divide-by-4	2
				203	—	—	ns	HMCS414C: divide-by-4 HMCS414CL: divide-by-8	2

AC Characteristics (GND = 0 V, Vdisp = V_{CC} – 40 V to V_{CC}, Ta = –20°C to + 75°C, HMCS414C: V_{CC} = 3.5 V to 6 V, HMCS414CL: V_{CC} = 2.5 V to 6 V, HMCS414AC: V_{CC} = 4.5 V to 6 V) (cont)

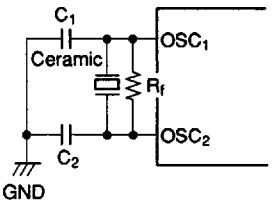
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	20	ms	HMCS414C/AC	4
			—	—	15	ms	HMCS414CL	4

Notes: 1. The oscillator stabilization time is period from when V_{CC} reaches its minimum allowable voltage (HMCS414C: 3.5 V, HMCS414CL: 2.5 V, HMCS414AC: 4.5 V) at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. Since t_{RC} depends on the crystal or ceramic circuit constant and stray capacitance, consult with the crystal or ceramic oscillator manufacturer when designing the reset circuit. (See figure 29.)
2. See figure 30.
3. See figure 31.
4. See figure 32.

HMCS414C/AC

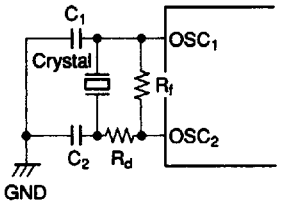


Crystal: 4.194304 MHz
NC-18C (Nihon Denpa Kogyo)
R_f = 1 MΩ ±20%,
$C_1 = C_2$ = 22 pF ±20%

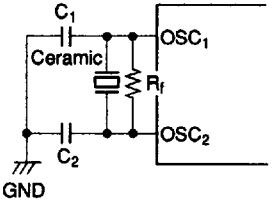


Ceramic: CSA4.00 MG (Murata)
R_f = 1 MΩ ±20%,
$C_1 = C_2$ = 30 pF ±20%

HMCS414CL



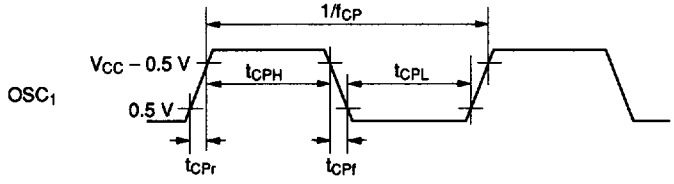
Crystal: 2.097152 MHz
DS-MGQ 308 (Seiko)
R_f = 1 MΩ ±20%, R_d = 2.2 kΩ ±20%
$C_1 = C_2$ = 10 pF ±20%



Ceramic: CSA 2.000MK (Murata)
R_f = 1 MΩ ±20%,
$C_1 = C_2$ = 30 pF ±20%

Figure 29 Oscillation Circuits

HMCS414C/AC



HMCS414CL

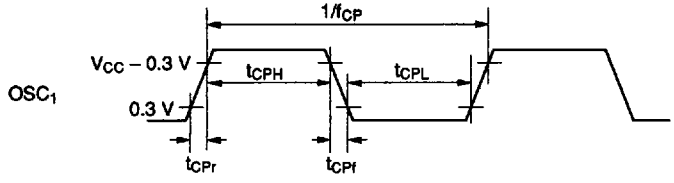


Figure 30 Oscillator Timing

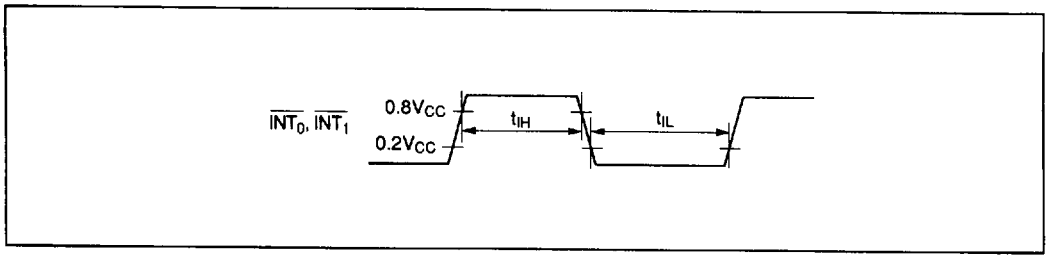


Figure 31 Interrupt Timing

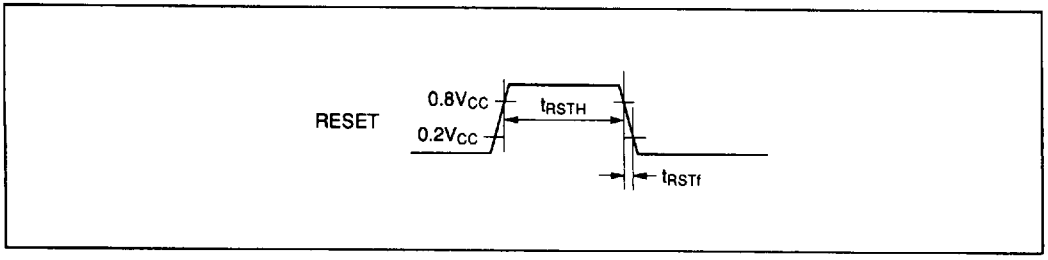


Figure 32 Reset Timing

HMCS414C/CL/AC
Option List

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

Please check off the appropriate applications and enter the necessary information.

5-V operation:	☐ HMCS414C (HD614141)
3-V operation:	☐ HMCS414CL (HD614146)
High speed operation:	☐ HMCS414AC (HD614149)

1. I/O option

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (cannot be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

Note: I/O options masked by ▒ are not available.

Pin	I/O		I/O option				
			A	B	C	D	E
D0	Standard pins	I/O				▒	▒
D1		I/O				▒	▒
D2		I/O				▒	▒
D3		I/O				▒	▒
D4	High voltage pins	I/O	▒	▒	▒		
D5		I/O	▒	▒	▒		
D6		I/O	▒	▒	▒		
D7		I/O	▒	▒	▒		
D8		I/O	▒	▒	▒		
D9		I/O	▒	▒	▒		
D10		I/O	▒	▒	▒		
D11		I/O	▒	▒	▒		
D12		I/O	▒	▒	▒		
D13		I/O	▒	▒	▒		
D14		I/O	▒	▒	▒		

Pin		I/O		I/O option				
				A	B	C	D	E
R0	R00	High voltage pins	O	▒	▒	▒		
	R01		O	▒	▒	▒		
	R02		O	▒	▒	▒		
	R03		O	▒	▒	▒		
R1	R10		I/O	▒	▒	▒		
	R11		I/O	▒	▒	▒		
	R12		I/O	▒	▒	▒		
	R13		I/O	▒	▒	▒		
R2	R20		I/O	▒	▒	▒		
	R21		I/O	▒	▒	▒		
	R22		I/O	▒	▒	▒		
	R23		I/O	▒	▒	▒		
R3	R30	Standard pins	I/O				▒	▒
	R31		I/O				▒	▒
	R32		I/O				▒	▒
	R33		I/O				▒	▒
R4	R40		I/O				▒	▒
	R41		I/O				▒	▒
	R42		I/O				▒	▒
	R43		I/O				▒	▒
RA	RA1	High voltage pin	I	Use checklist RA1/Vdisp				

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (Div)

Divider	4	8	16
HMCS414C	☐	☐	
HMCS414CL		☐	☐
HMCS414AC	☐		

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator (OSC1 and OSC2)

☐ HMCS414C (5-V operation)	☐ HMCS414CL (3-V operation)	☐ HMCS414AC (high speed operation)
☐ Resistor (Rf = 18 kΩ ±1%, ÷ 8)		
☐ Ceramic oscillator	☐ Ceramic oscillator	☐ Ceramic oscillator
☐ Crystal oscillator	☐ Crystal oscillator	☐ Crystal oscillator
☐ External clock	☐ External clock	☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-42
☐ FP-42S
☐ FP-44A

HMCS424C/CL/AC Electrical Characteristics

DC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	$0.8V_{CC}$	V_{CC} + 0.3	V		
		SI	$0.7V_{CC}$	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	V_{CC} + 0.3	V	HMCS424C/AC	
			V_{CC} – 0.3	V_{CC} + 0.3	V	HMCS424CL	
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	–0.3	$0.2V_{CC}$	V		
		SI	–0.3	$0.3V_{CC}$	V		
		OSC_1	–0.3	0.5	V	HMCS424C/AC	
			–0.3	0.3	V	HMCS424CL	
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 1.0	—	V	HMCS424C/AC: $-I_{OH}$ = 1.0 mA	
			V_{CC} – 0.5	—	V	HMCS424C/AC: $-I_{OH}$ = 0.5 mA; HMCS424CL: $-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	0.4	V	HMCS424C/AC: I_{OL} = 1.6 mA; HMCS424CL: I_{OL} = 0.4 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{SCK}$, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, SI, SO, OSC_1	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	2	mA	HMCS424C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷4	2, 5
			—	0.7	mA	HMCS424CL: V_{CC} = 3 V; f_{OSC} = 2 MHz, ÷ 4	2, 5
			—	3.2	mA	HMCS424AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4	2, 5

DC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V) (cont)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	1.2	mA	HMCS424C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷ 4	3, 5
			—	0.5	mA	HMCS424CL: V_{CC} = 3 V; f_{OSC} = 2 MHz, ÷ 8	3, 5
			—	1.7	mA	HMCS424AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	10	µA	HMCS424C/AC: $V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}; $V_{in(RESET)}$ = 0 V to 0.3 V HMCS424CL: $V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}; $V_{in(RESET)}$ = 0 V to 0.2 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	V		

Notes: 1. Excluding pull up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3, R4: V_{CC}
   - D_4 to D_{14}, R0 to R2, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: Stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3, R4: V_{CC}
   - D_4 to D_{14}, R0 to R2, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHZ, estimate the current dissipation as follows:
   HMCS424C/AC: Maximum value at x MHz = (x/4) × (max. value at 4 MHz)
   HMCS424CL: Maximum value at x MHz = (x/2) × (max. value at 2 MHz)

Input/Output Characteristics for Standard Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3, R4	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3, R4	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_3, R3, R4	V_{CC} – 1.0	—	—	V	HMCS424C/AC: $-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, R3, R4	V_{CC} – 0.5	—	—	V	HMCS424C/AC: $-I_{OH}$ = 0.5 mA; HMCS424CL: $-I_{OH}$ = 0.3 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3, R4	—	—	0.4	V	HMCS424C/AC: I_{OL} = 1.6 mA HMCS424CL: I_{OL} = 0.4 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3, R4	30	60	150	µA	V_{CC} = 5 V, V_{in} = 0 V	3
		D_0 to D_3, R3, R4	3	15	50	µ A	HMCS424CL only: V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High-Voltage Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{14}, R1, R2, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{14}, R1, R2, RA_1	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{14}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, HMCS424C/CL: V_{CC} = 5 V ± 20%; HMCS424AC: V_{CC} = 4.5 V to 6.0 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, HMCS424C/CL: V_{CC} = 5 V ±20%; HMCS424AC: V_{CC} = 4.5 V to 6.0 V	
			V_{CC} – 1.0	—	—	V	HMCS424C/AC: $-I_{OH}$ = 4 mA; HMCS424CL: $-I_{OH}$ = 2.5 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, HMCS424C/CL: V_{CC} = 5 V ±20% HMCS424AC: V_{CC} = 4.5 V to 6.0 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 2 mA, HMCS424C/CL: V_{CC} = 5 V ±20%; HMCS424AC: V_{CC} = 4.5 V to 6.0 V	
			V_{CC} – 1.0	—	—	V	HMCS424C/AC: $-I_{OH}$ = 0.8 mA HMCS424CL: $-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_4 to D_{14}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{14}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\lvert I_{IL} \rvert$	D_4 to D_{14}, R0 to R2, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{14}, R0 to R2, RA_1	125	250	600	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	HMCS424C: divide-by-8	
			0.2	2	2.25	MHz	HMCS424C: divide-by-4	
			0.4	2	2.25	MHz	HMCS424CL: divide-by-8	
			0.2	4	4.5	MHz	HMCS424AC: divide-by-4	
Instruction cycle time	t_{cyc}		1.78	2	20	µs	HMCS424C	
			3.55	4	20	µs	HMCS424CL	
			0.89	1	20	µs	HMCS424AC	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HMCS424C/AC	1
			—	—	60	ms	HMCS424CL	1
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	HMCS424C: divide-by-8 HMCS424AC: divide-by-4	2
			203	—	—	ns	HMCS424C: divide-by-4 HMCS424CL: divide-by-8	2

AC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V) (cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	20	ms	HMCS424C/AC	4
			—	—	15	ms	HMCS424CL	4

Notes: 1. The oscillator stabilization time is period from when V_{CC} reaches its minimum allowable voltage (HMCS424C: 3.5 V, HMCS424CL: 2.5 V, HMCS424AC: 4.5 V) at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. Since t_{RC} depends on the crystal or ceramic circuit constant and stray capacitance, consult with the crystal or ceramic oscillator manufacturer when designing the reset circuit.

2. See figure 33.
3. See figure 34.
4. See figure 35.

Serial Interface Timing Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1, 2
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1, 2
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HMCS424C/AC	1, 2
			—	—	300	ns	HMCS424CL	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HMCS424C	1, 2
			—	—	600	ns	HMCS424CL	1, 2
			—	—	250	ns	HMCS424AC	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns	HMCS424C	1
			1000	—	—	ns	HMCS424CL	1
			300	—	—	ns	HMCS424AC	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HMCS424C/AC	1
			500	—	—	ns	HMCS424CL	1

Notes: 1. See figure 36.
2. See figure 37.

Serial Interface Timing Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C, HMCS424C: V_{CC} = 3.5 V to 6 V, HMCS424CL: V_{CC} = 2.5 V to 6 V, HMCS424AC: V_{CC} = 4.5 V to 6 V)

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HMCS424C/AC	1
			—	—	300	ns	HMCS424CL	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HMCS424C	1, 2
			—	—	600	ns	HMCS424CL	1, 2
			—	—	250	ns	HMCS424AC	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns	HMCS424C	1
			1000	—	—	ns	HMCS424CL	1
			300	—	—	ns	HMCS424AC	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HMCS424C/AC	1
			500	—	—	ns	HMCS424CL	1

Notes: 1. See figure 36.
2. See figure 37.

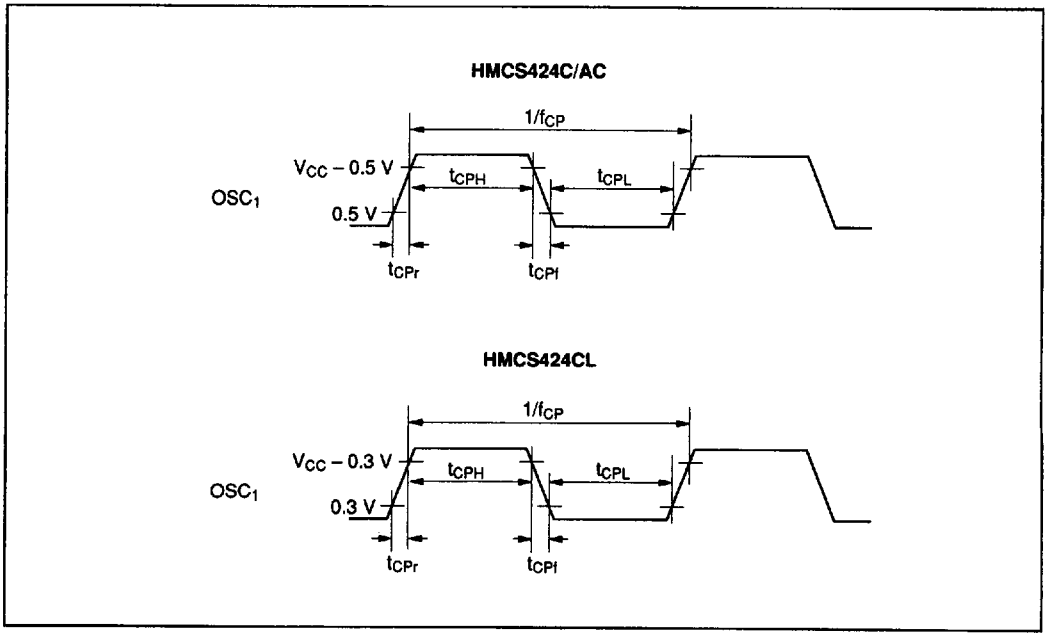


Figure 33 Oscillator Timing

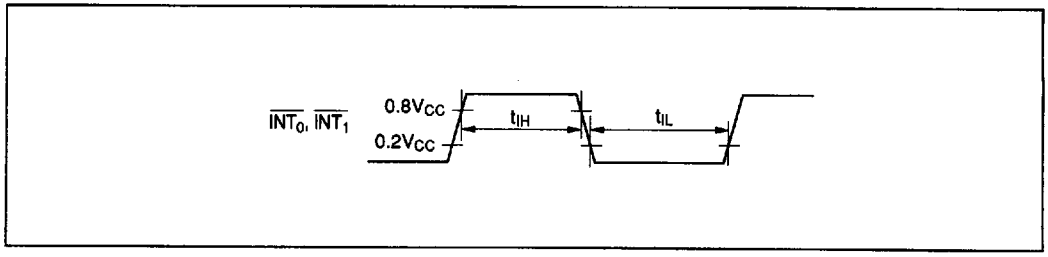


Figure 34 Interrupt Timing

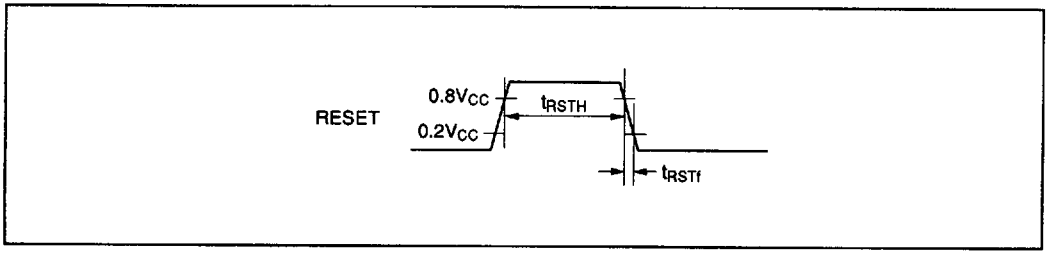
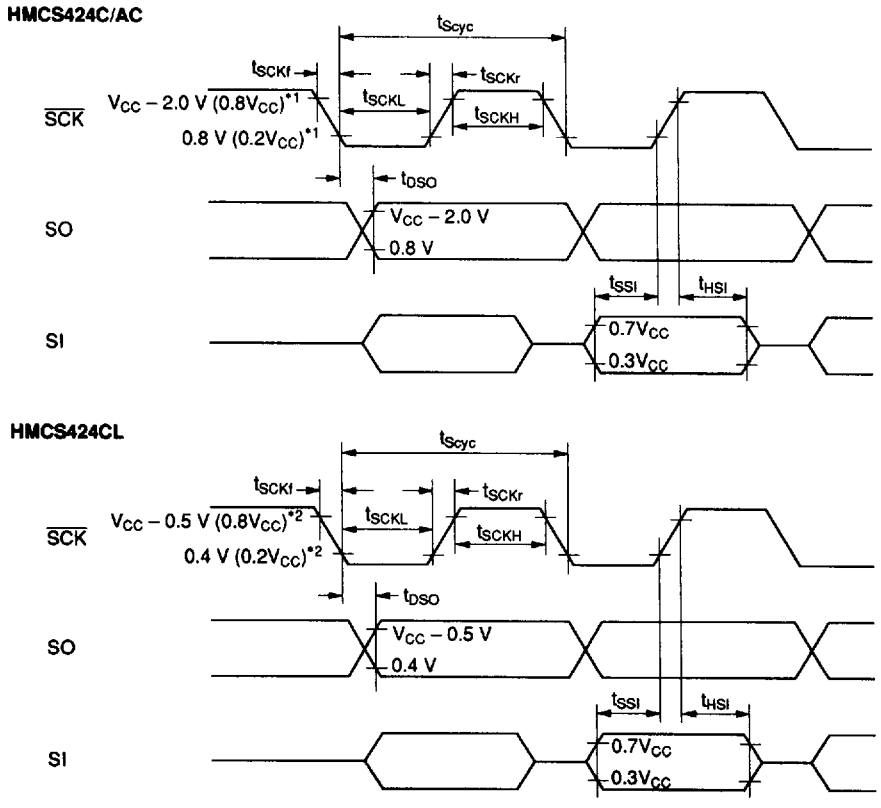


Figure 35 Reset Timing



Notes: 1. V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
$0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input.

2. V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
$0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input.

Figure 36 Serial Interface Timing

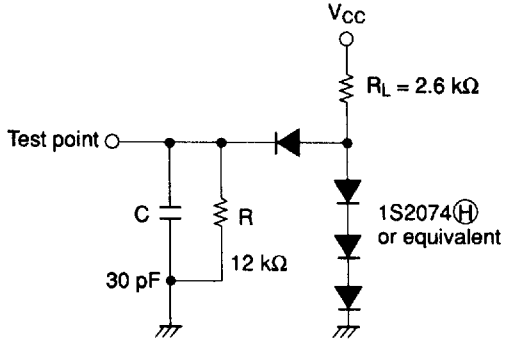


Figure 37 Timing Load Circuit

HMCS424C/CL/AC
Option List

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

Please check off the appropriate applications and enter the necessary information.

5-V operation:	☐ HMCS424C (HD404240)
3-V operation:	☐ HMCS424CL (HD40L4240)
High speed operation:	☐ HMCS424AC (HD40A4240)

1. I/O option

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (cannot be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

Note: I/O options masked by ▒ are not available.

Pin	I/O		I/O option				
			A	B	C	D	E
D0	Standard pins	I/O				▒	▒
D1		I/O				▒	▒
D2		I/O				▒	▒
D3		I/O				▒	▒
D4	High voltage pins	I/O	▒	▒	▒		
D5		I/O	▒	▒	▒		
D6		I/O	▒	▒	▒		
D7		I/O	▒	▒	▒		
D8		I/O	▒	▒	▒		
D9		I/O	▒	▒	▒		
D10		I/O	▒	▒	▒		
D11		I/O	▒	▒	▒		
D12		I/O	▒	▒	▒		
D13		I/O	▒	▒	▒		
D14		I/O	▒	▒	▒		

Pin		I/O		I/O option				
				A	B	C	D	E
R0	R00	High voltage pins	O	▒	▒	▒		
	R01		O	▒	▒	▒		
	R02		O	▒	▒	▒		
	R03		O	▒	▒	▒		
R1	R10		I/O	▒	▒	▒		
	R11		I/O	▒	▒	▒		
	R12		I/O	▒	▒	▒		
	R13		I/O	▒	▒	▒		
R2	R20		I/O	▒	▒	▒		
	R21		I/O	▒	▒	▒		
	R22		I/O	▒	▒	▒		
	R23		I/O	▒	▒	▒		
R3	R30	Standard pins	I/O				▒	▒
	R31		I/O				▒	▒
	R32		I/O				▒	▒
	R33		I/O				▒	▒
R4	R40		I/O				▒	▒
	R41		I/O				▒	▒
	R42		I/O				▒	▒
	R43		I/O				▒	▒
RA	RA1	High voltage pin	I	Use checklist RA1/Vdisp				

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (Div)

Divider	4	8
HMCS424C	☐	☐
HMCS424CL		☐
HMCS424AC	☐	

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator (OSC1 and OSC2)

☐ HMCS424C (5-V operation)	☐ HMCS424CL (3-V operation)	☐ HMCS424AC (high speed operation)
☐ Ceramic oscillator	☐ Ceramic oscillator	☐ Ceramic oscillator
☐ Crystal oscillator	☐ Crystal oscillator	☐ Crystal oscillator
☐ External clock	☐ External clock	☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-42
☐ DP-42S
☐ FP-44A