HMCAD5831LP9BE

v00.0312

26 GS/S 3-BIT ANALOG-TO-DIGITAL CONVERTER W/ OVERRANGE, INHIBIT, AND 1:2 DEMUX

Typical Applications

The HMCAD5831LP9BE is ideal for:

- Serial Data Links
- Test Equipment for Link Diagnostics
- Clock & Data Recovery
- Spectrometers
- Ultra Wideband Phased Arrays
- Radio Astronomy

Features

Full Flash Architecture

Over/Under Range Bit

Data Inhibit Function

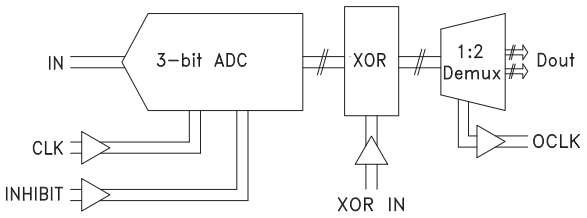
Data XOR Function

1:2 Demux

Programmable Differential CML Output Swing

64 Lead Plastic 9 x 9 mm SMT Package: 81 mm^2

Functional Diagram



General Description

The HMCAD5831LP9BE is a wideband 3-bit analog-to-digital converter with over/under range bit. The converter operates at speeds up to 26 GS/s with a Nyquist input. Reference ladder end voltages are set externally by the user allowing the user to customize input common mode and swing levels. ADC outputs can be forced to 0 by using the Data Inhibit function. Output data can be modulated by an external clock via the XOR CML input. The HMCAD5831LP9BE also features a 1:2 demux with half rate clock output. The output bits are binary weighted, where X2 and Y2 are the MSBs. The single-ended RF input can be AC or DC coupled and supports broadband operation.

The HMCAD5831LP9BE operates from -5 V and -3.3 V supplies and is available in ROHS-compliant 9 x 9 mm SMT package.

Electrical Specifications, T_A = +25 °C, AVEE = -5 V, OVEE = -3.3 V

Parameter	Conditions	Min.	Typ.	Max	Units
Resolution			3		bits
Sample Rate			20	26 [1]	GHz
DNL (including Overrange Bit)		-0.5		0.5	lsbs
INL (including Overange Bit)		-0.5	±0.3	0.5	lsbs
Input Bandwidth			20		GHz
Input DC Voltage			0		V
Input Voltage Swing	Can be user defined		256		mV
Input Rin			50		Ω
Clock Power, Single Ended			-3		dBm
Clock, XOR Rin	Differential		100		Ω
Ladder Top Voltage (RTF)	Can be user defined		-0.808		V

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Electrical Specifications *(continued)*

Parameter	Conditions	Min.	Typ.	Max	Units
Ladder Bottom Voltage (RBF)	Can be user defined		-1.064		V
Output Amplitude [2]	Single ended, peak to peak		286		mVp-p
Output High Voltage [2]			-33		mV
Output Low Voltage [2]			-319		mV
XOR Clock Rate			156.25		MHz
XOR Input Power, Single Ended			-3		dBm
Data Inhibit Rin	Single ended		600		Ω
Data Inhibit High Voltage			200		mV
Data Inhibit Low Voltage			-200		mV
Data, Clock, OVR Bits Rout	Differential		100		Ω
Data, Clock, OVR Bits Rout	Single ended		50		Ω
Demux Ratio			1:2		
ENOB (20 GS/s)	fin = 312.5 MHz		2.9		bits
ENOB (20 GS/s)	fin = 9.6875 GHz		2.9		bits
ENOB (20 GS/s)	fin = 19.6875 GHz		2.9		bits
ENOB (26 GS/s)	fin = 406.25 MHz		2.9		bits
ENOB (26 GS/s)	fin = 12.5938 GHz		2.9		bits
SFDR (20 GS/s)	fin = 312.5 MHz		24.7		dBFS
SFDR (20 GS/s)	fin = 9.6875 GHz		25.7		dBFS
SFDR (20 GS/s)	fin = 19.6875 GHz		27.2		dBFS
Power Supply Voltage		-4.5	-5	-5.5	V
Power Supply Current (-5 V)			725		mA
Power Supply Voltage		-3	-3.3	-3.6	V
Power Supply Current (-3.3 V)			176		mA
Power			4.2		W

[1] Requires sufficient clock power and cooling.
[2] With a single 200 Ω resistor tied from VREF1 and VREF2 to OGND. VREF1 and VREF2 are connected off chip.

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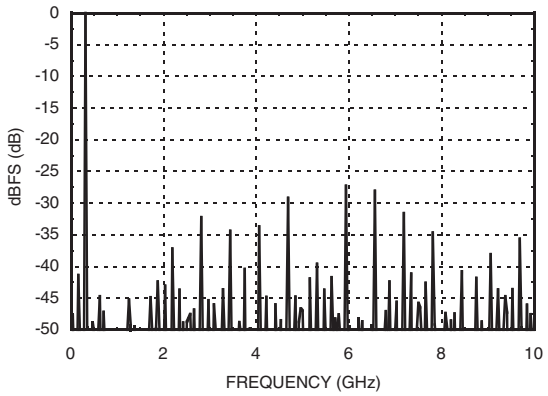
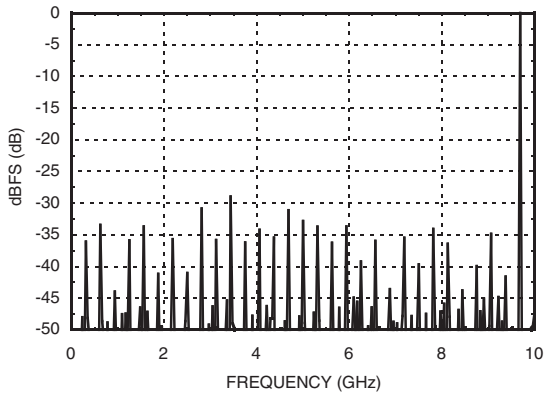
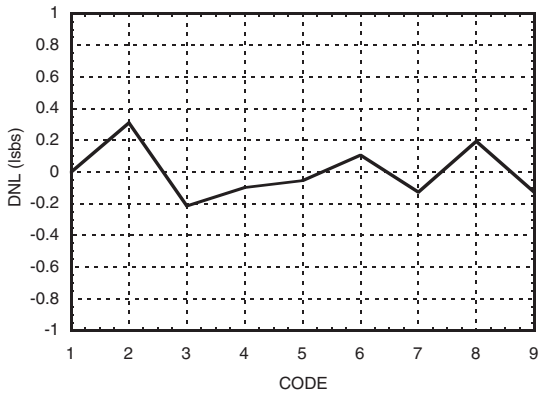
Spectral Performance FFT
(312.5 MHz input, 20 GS/s clock)



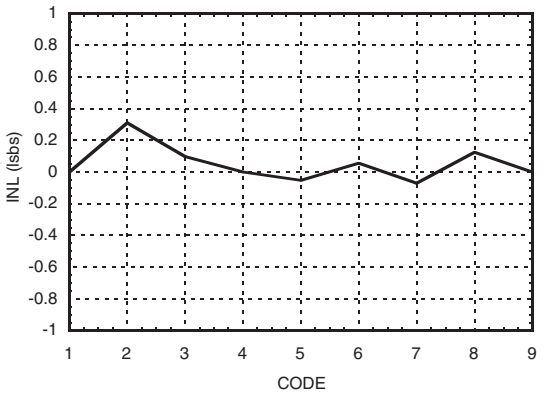
Spectral Performance FFT
(9.6875 GHz input, 20 GS/s clock)



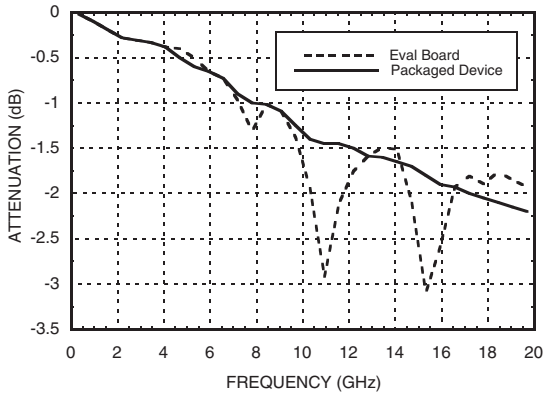
Differential Nonlinearity
(Including overrange bits)



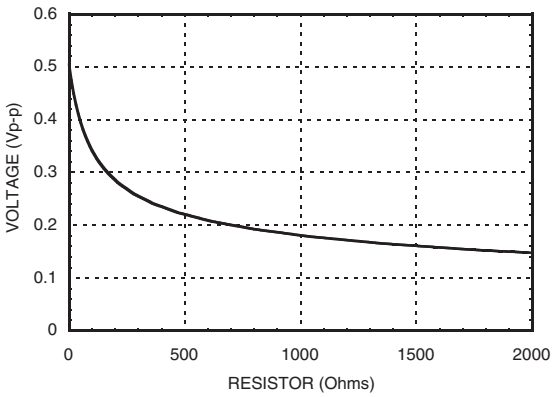
Integral Nonlinearity
(Including overrange bits)



Bandwidth [1]

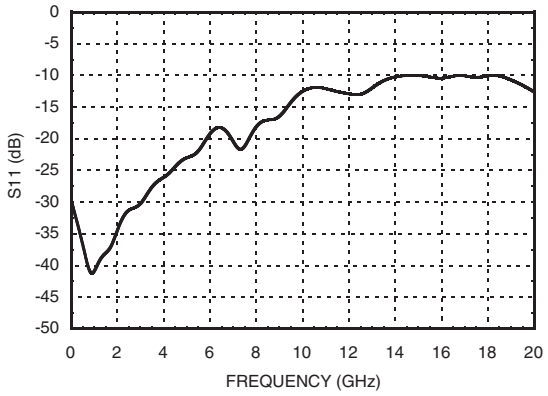


VREF Resistor Value vs. Output Voltage Swing [2]

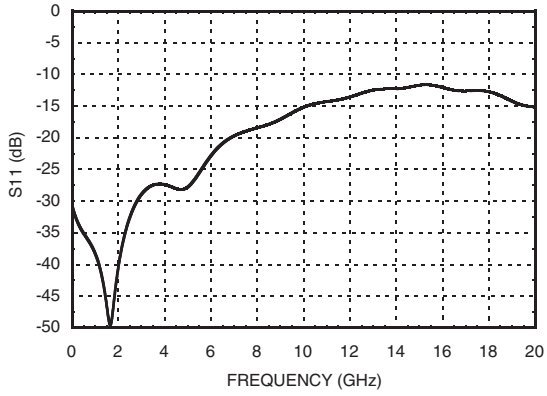


[1] This graph was made by measuring the analog input power required to get full scale on the digital output. The increase in power from DC should be equal to the attenuation. The effects of the cables and the circuit board were estimated and subtracted from the measured attenuation to determine the input attenuation of the packaged part.
[2] Single-ended voltage swing into 50 ohm resistor.

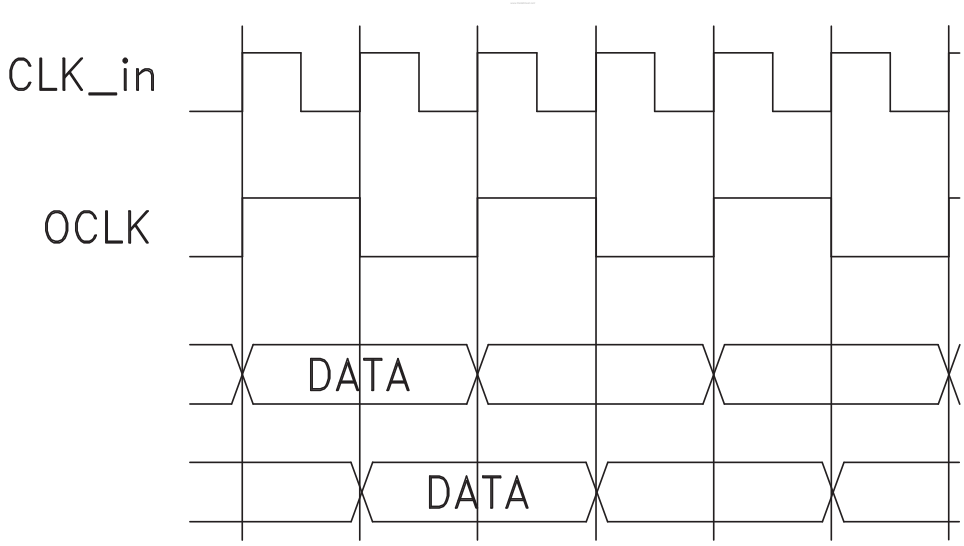
Signal S11 [1]



Clock S11 [1]

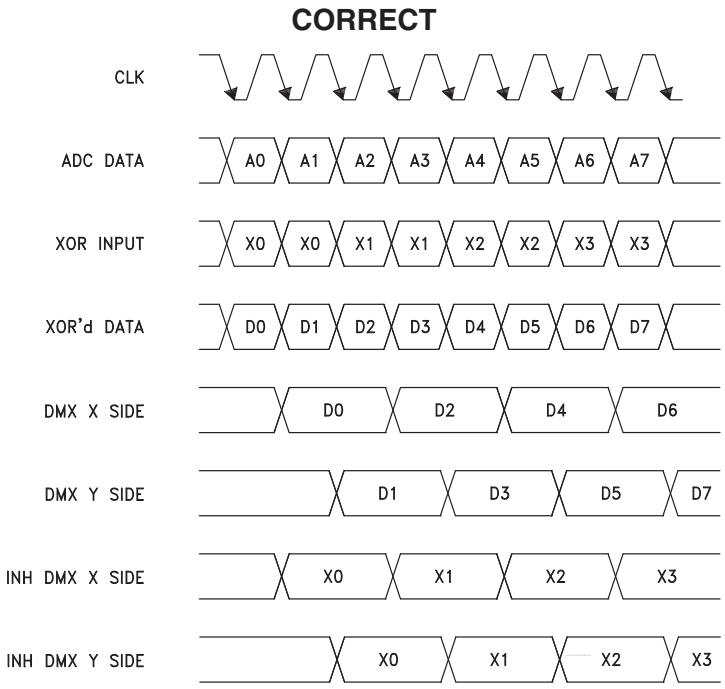


Timing Diagram

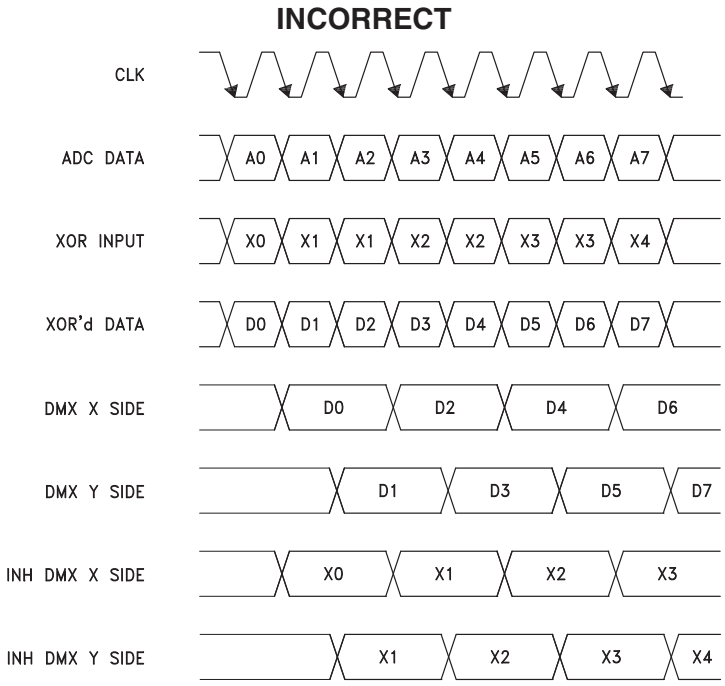


[1] This is S11 data taken from the input of the evaluation board. The gating function on the network analyzer was employed to remove the effects of the PCB and look only at the packaged part.

XOR Input Alignment Timing Diagrams For X Side Leading



Data
D0 = A0 xor X0
D1 = A1 xor X0
D2 = A2 xor X1
D3 = A3 xor X1
D4 = A4 xor X2
D5 = A5 xor X2



Data
D0 = A0 xor X0
D1 = A1 xor X1
D2 = A2 xor X1
D3 = A3 xor X2
D4 = A4 xor X2
D5 = A5 xor X3

The FPGA aligns the data with the X side leading. In the incorrect case, a 1-bit shift is caused by the 1 clock cycle delay in the XOR.

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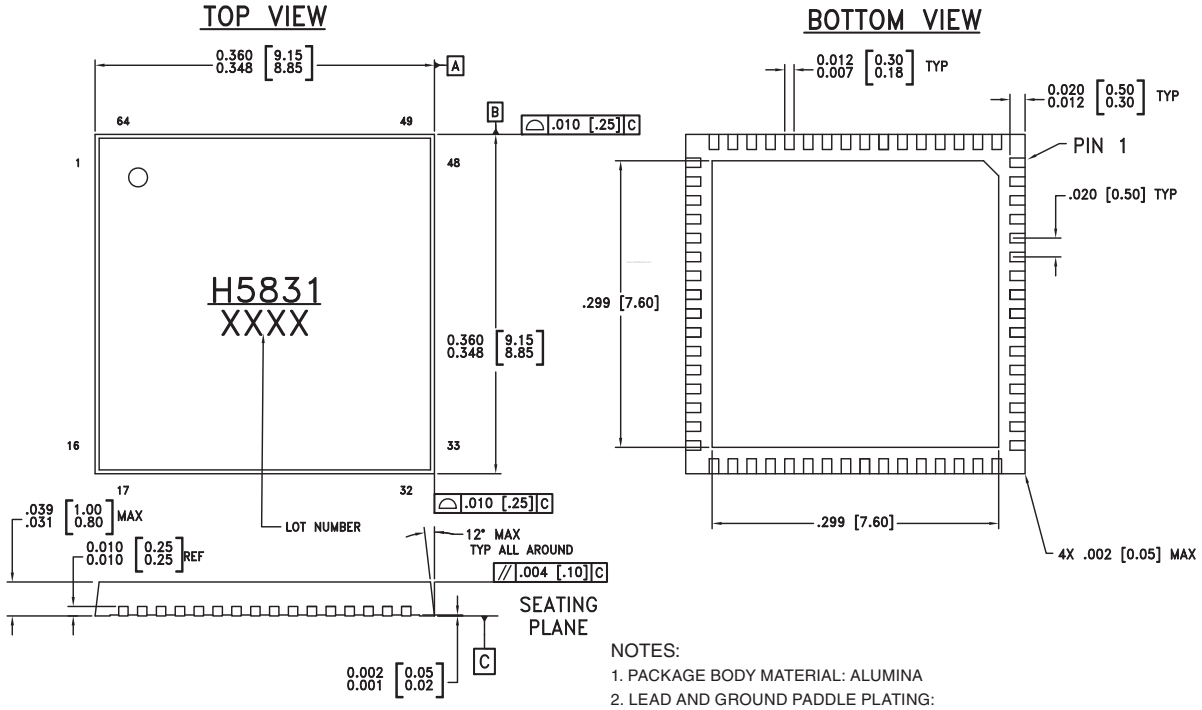
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-5.5 V to +0.5 V
Power Supply Voltage (OVee)	-3.6 V to +0.5 V
Input and Clock Signals	-2 V to +0.5 V
Output Signals	-1.5 V to 0.5 V
Junction Temperature	125 °C
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case device to package paddle	2.5 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +70 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

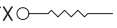
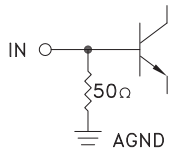
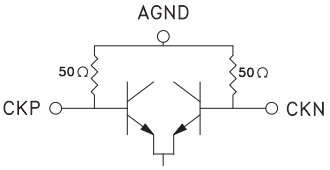
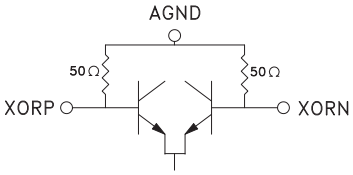
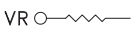
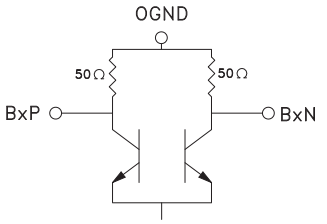
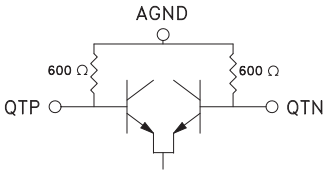
Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO AVEE
8. PART IS OPERATED WITH A HEATSINK OF 25 SQ. CM. SURFACE AREA AND AN AIRFLOW OF 10 CFM.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 15	RTF, RBF	Reference ladder top and bottom taps	
2, 7, 9, 10, 13, 16, 17, 18, 21, 60, 63, 64	AGND	Analog ground	
3, 4, 5, 6, 14	AVEE	-5 V analog rail These pins and the exposed paddle must be connected to the negative voltage supply.	
8	IN	Single-ended RF input referenced to AGND.	
11, 12	CKP, CKN	Differential clock inputs Current Mode Logic (CML) referenced to AGND.	
19, 20	XORP, XORN	Differential XOR inputs Current Mode Logic (CML) referenced to AGND.	
22, 23, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 58, 59	OGND	Digital ground	
24, 25, 56, 57	OVEE	-3.3 V digital rail	
26, 55	VREF2, VREF1	Output level control Output level may be increased or decreased by applying a voltage to Vref pins.	
28, 29, 31, 32, 34, 35, 37, 38, 43, 44, 46, 47, 49, 50, 52, 53	XVN, XVP, YVN, YVP, XON, XOP, YON, YOP, X1N, X1P, Y1N, Y1P, X2N, X2P, Y2N, Y2P	Differential outputs Current Mode Logic (CML) referenced to OGND.	
40, 41	OCLKN, OCLKP	Differential clock output Current Mode Logic (CML) referenced to AGND.	
61, 62	QTN, QTP	Differential data inhibit inputs	

Reference Ladder

The ADC's voltage reference ladder comprises 8, 18 Ω resistors, or 144 Ω total resistance. Pin 1, RTF, and pin 15, RBF, are provided for the top and bottom reference taps. These pins are driven by external supplies to establish the desired full-scale range of the ADC. The RF signal input (pin 8, IN) to the ADC drives an internal emitter follower with a nominal VBE of -900 mV. Hence the center of full-scale range should center near -900 mV. The voltage at pin RTF is then -900 mV + $V_{full\text{-}scale}$/2. Likewise the voltage at pin RBF is -900 mV - $V_{full\text{-}scale}$/2.

As an example, if the user had a peak-to-peak input voltage swing of 256 mV and required the full-scale input range of the ADC to be 256 mV as well, RTF would be -900 mV + 128 mV = -772 mV. RBF would be -900 mV - 128 mV = -1.028 V. Note that the diode drop, -900 mV, is dependent on temperature and process variations.

RTF and RBF values in the "Electrical Specifications" table on pages 1 and 2 are shown as nominal values only. Note that ladder end voltages, RTF and RBF, are set by the common-mode level of the input, IN.

For operation of 10 GHz input and 20 GS/s sample rate, recommended maximum input swing is 0.512 V as set by RTF and RBF. For lower input frequencies, the device will operate with a maximum 1.5 V input swing. The Electrical Specifications table lists typical operating ranges.

VREF Pins

Pins 26 and 55 (VREF1 amd VREF2) should be connected together off chip and the pair is then connected to the OGND through a resistor. These pins are used to vary the output swing voltage. The Application Circuit shown uses a 200 Ω resistor. This provides the typical output swings listed in the Electrical Specifications table. Increasing the voltage on VREF1 and VREF2 will increase the output swing. Conversely, decreasing the VREF1 and VREF2 voltages will decrease the output swing.

Overrange Output

Pins 28, 29, 31, and 32 provide overrange output bits. This function indicates when the input signal is out of range of the reference ladder voltages. The bit will be high when either the signal is above RTF or below RBF. The overrange bit is cleared for the next clock cycle containing in-range data.

Data Inhibit

All data outputs can be forced to "0" by enabling the Data Inhibit function (pins 61 and 62). By driving the QTP pin high and the QTN pin low, the ADC core will produce all 0s. This occurs prior to the XOR funciton and the demux. When QTP is low and QTN is high, the chip operates normally.

Data XOR

All data outputs from the ADC core can be modulated by an external source. This allows the user to use AC coupling for output line connection to a SERDES input of an FPGA. This function occurs prior to the demux. The XOR input signal is retimed by the full rate internal clock and requires low jitter and suitable rise and fall times. Please contact Hittite Microwave for sample driver circuits. Typical modulation frequencies are 100 MHz to 300 MHz. For a square wave signal, a multiple of two divisor of the full rate internal clock should be used, e.g. 1/128th or 1/64th of the ADC clock. Due to the nature of the retiming scheme, the demux channel relationship timing can vary. This is dependent on when the XOR input is sampled relative to the full rate internal clock. See timing diagrams on page 5. For example, a nominal setup may have demux side X leading and side Y trailing. If the XOR input is shifted relative to the internal clock, side Y may lead and side X may trail. It is highly recommended that a variable delay be used to adjust the phase of the XOR input to avoid transitions that are very close to internal clock edges. See Typical Operation Example for more information. The XOR function can be used with the Data Inhibit function to produce a sync pattern for aligning the lanes of SERDES inputs. The device outputs are inverted when XOR is low.

Evaluation Board Description

EVAL01-HMC5831LP9 (131499) demonstrates the HMCAD5831LP9BE in an environment ready to be connected to an FPGA. Along with the ADC, the board features three other Hittite Microwave components. The clock output of the ADC is divided down by 64 (two stages of 8, U1, and U2) to produce a clock ouput that is 1/128th of the ADC clock input. This clock is available to drive the FPGA or other system components. The ADC XOR input has programmable delay (U4) allowing the user to fine-tune the XOR clock edges going into the ADC. The INHIBIT and D8BX inputs are 0 to +3.3 V, compatible with most FPGAs. Finally, the ADC_VR pin allows the user to control the output voltage swing of the ADC. Output connectors J2 and J3 are high-performance SAMTEC connectors, part number ERF8-013-05.0-DV.

Ten-Level Operation

The HMCAD5831LP9BE can be used as a ten-level (3.32 bits) ADC by combining the regular data outputs with the Overrange Bit. The bottom code (code 0) is equal to OVR high and all the bits low. For codes 1 through 8, the ADC functions normally (with OVR low). The top code, code 9, is all bits high. Note that the INL/DNL plots include OVR in this manner.

Typical Operation Example

An FPGA with suitably fast SERDES inputs can capture data from the HMCAD5831LP9BE using the following routine. The FPGA produces an INHIBIT high signal causing the ADC core to produce all 0s. The XOR input to the ADC runs at some slow clock rate and modulates the ADC output to produce a known waveform at the FPGA inputs. The FPGA then uses these signals to align the lanes. When the lanes are aligned, the INHIBIT signal goes low and the ADC produces signal data that continues to be modulated by the XOR input. The FPGA then corrects for the modulation. Note that the FPGA can generate the XOR modulation signal (in which case a PRBS sequence could be used). Depending on the phase of the XOR input modulation waveform, either demux output (X or Y) can be the leading data sample. In this case, the FPGA would need to resolve which lane is the leader. This can be accomplished by driving the ADC with a known signal, evaluating the outputs and reassembling FPGA data if necessary. It is recommended to do this on each power up. It is also recommended to perform a routine to ensure that the XOR input waveform is properly aligned with the internal clock. This can be accomplished by sweeping the external variable delay stage.

High-Temperature Operation

It is highly recommended that the part be used with a heat sink and fan. Performance diminishes as temperature increases. Nominal conditions for part evaluation occurred at an ambient temperature of 25 °C. The evaluation board has a heat sink with an area of 25 cm^2. With this setup, the paddle of the part was measured to be 45 °C. When the paddle temperature was raised to 75 °C, limited performance was maintained, with an increased clock power level. At 75 °C, performance is guaranteed up to 10 GHz input frequency, 20 GS/s clock rate only. For temperatures above 75 °C, device performance is not guaranteed above 20 GS/s.

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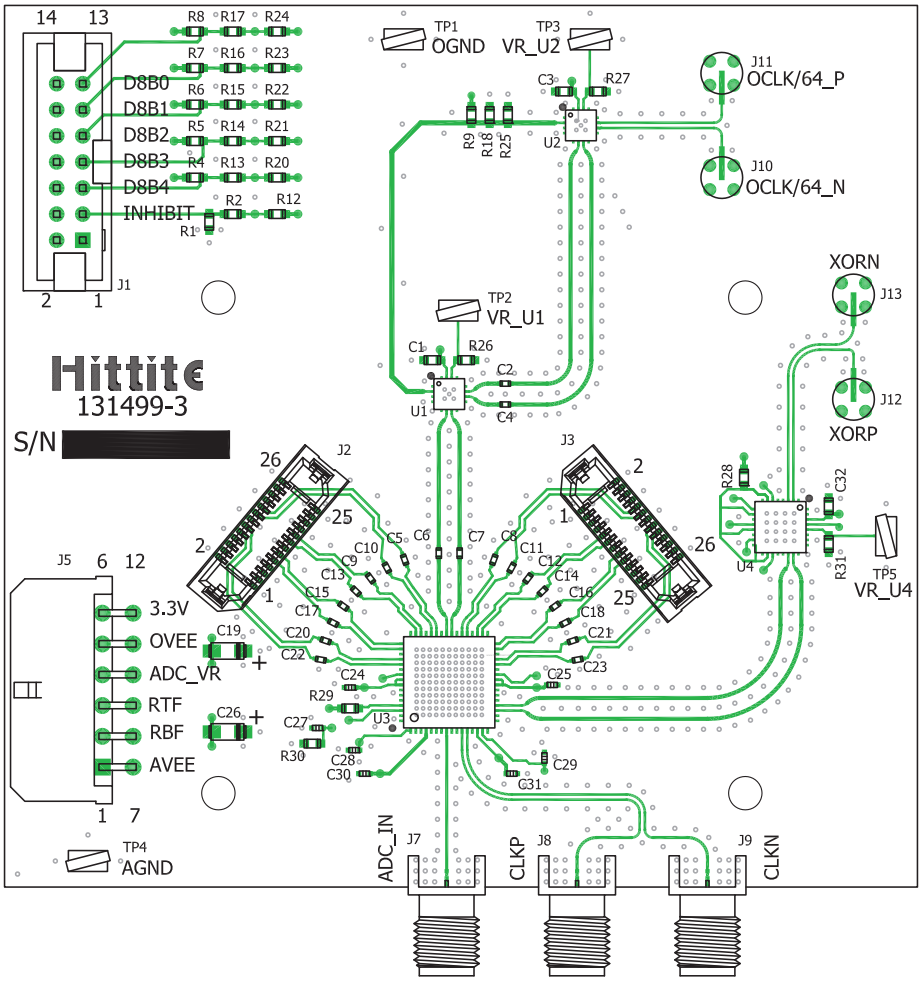
Evaluation PCB



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List of Materials for Evaluation PCB EVAL01-HMC5831LP9 [1]

Item	Description
J1	14 Position Straight Header
J2, J3	Edge Rate Socket Strip, 26 Position
J5	Conn Header 12 Position 3mm 2 Rows
J7 - J9	PCN Mount k RF Connectors
J10 - J13	SMP Full Detent RF Connectors
C1, C3, C32	1000 µF Capacitor, 0603 Pkg.
C2, C4 - C18, C20 - C23	1000 µF Capacitor, 0402 Pkg
C19, C26	4.7 µF Capacitor, 1206 Pkg.
C24 - C25, C27 - C31	100 nF Capacitor 0402 Pkg.
R1, R4 - R8	33 K Ohm Resistor, 0603 Pkg.
R2, R12 - R17, R20 - R24	3.3 K Ohm Resistor, 0603 Pkg.
R18, R25, R28	1.2 K Ohm Resistor, 0603 Pkg.
R26, R27, R31	51 Ohm Resistor, 0603 Pkg.
R29	14 K Ohm Resistor, 0603 Pkg.
R30	200 Ohm Resistor, 0603 Pkg.
U1, U2	HMC859LC3 Divide By 8, 26 GHz
U3	HMC5831LP9 20 GS/s 3-bit ADC
U4	HMC856LC5 5-Bit Time Delay, 26 GHz
PCB [2]	131499 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to AVEE. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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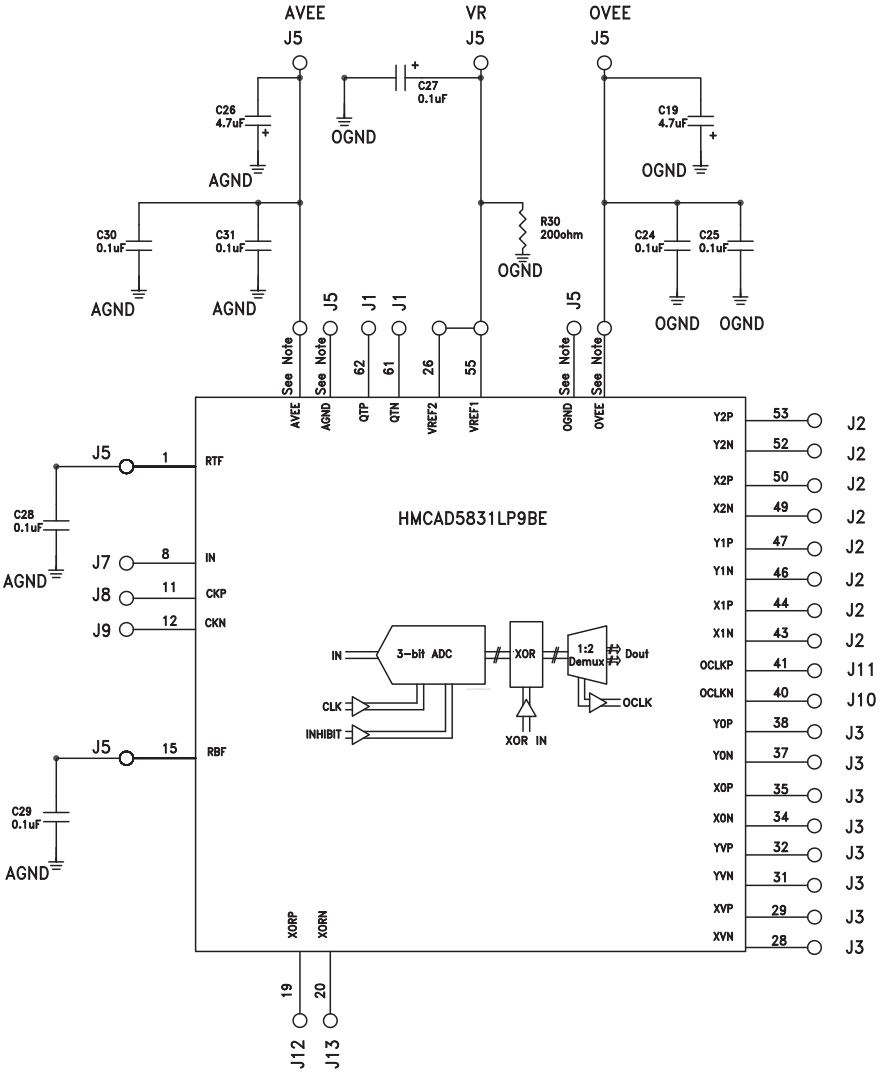
Application Circuit



Pin Number	Function	Description
2, 7, 9, 10, 13, 16, 17, 18, 21, 60, 63, 64	AGND	Analog ground
3, 4, 5, 6, 14	AVEE	-5 V analog rail These pins and the exposed paddle must be connected to the negative voltage supply.
22, 23, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 58, 59	OGND	Digital ground
24, 25, 56, 57	OVEE	-3.3 V digital rail
J5		12-position MOLEX.
J2, J3		SAMTEC