HMC849LP4CE

HIGH ISOLATION SPDT NON-REFLECTIVE SWITCH, DC - 6 GHz

Typical Applications

The HMC849LP4CE is ideal for:

- Cellular/4G Infrastructure
- WiMAX, WiBro & Fixed Wireless
- Automotive Telematics
- Mobile Radio
- Test Equipment

Features

High Isolation: up to 60 dB

Single Positive Control: 0/+3V to +5V

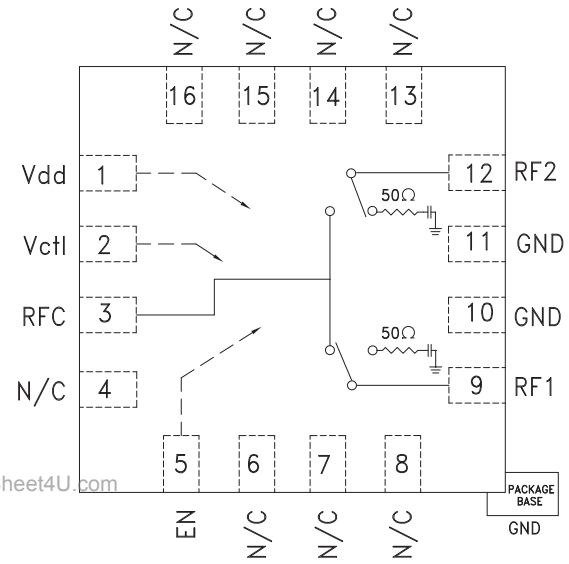
High Input IP3: +52 dBm

Non-Reflective Design

"All Off" State

24 Lead 4x4 mm QFN Package: 16 mm²

Functional Diagram



General Description

The HMC849LP4CE is a high isolation non-reflective DC to 6 GHz GaAs pHEMT SPDT switch in a low cost leadless surface mount package. The switch is ideal for cellular/WiMAX/4G Infrastructure applications yielding up to 60 dB isolation, low 0.8 dB insertion loss and +52 dBm input IP3. Power handling is excellent up through the 5 - 6 GHz WiMAX band with the switch offering a P1dB compression point of +31 dBm. On-chip circuitry allows a single positive voltage control of 0/+3V or 0/+5V at very low DC currents. An enable input (EN) set to logic high will put the switch in an "all off" state.

Electrical Specifications, T_A = +25 °C, Vctl = 0/Vdd, Vdd = +3V to +5V, 50 Ohm System

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 2.0 GHz 2.0 - 4.0 GHz 4.0 - 6.0 GHz		0.8 1.0 1.7	1.3 1.5 2.5	dB dB
Isolation (RFC to RF1/RF2)	DC - 2.0 GHz 2.0 - 4.0 GHz 4.0 - 6.0 GHz	53 48 40	60 55 52		dB dB
Return Loss (On State)	DC - 4.0 GHz 4.0 - 6.0 GHz		17 13		dB dB
Return Loss (Off State)	DC - 6.0 GHz		15		dB
Input Power for 1 dB Compression +3V +5V	0.35 - 4.0 GHz	29 34	30 35		dBm dBm
Input Third Order Intercept (Two-Tone Input Power = +7 dBm Each Tone)	DC - 6.0 GHz		52		dBm
Switching Speed tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 4.0 GHz		 80 150		 ns ns

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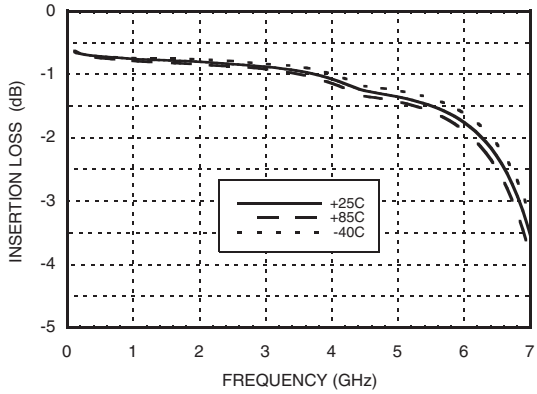
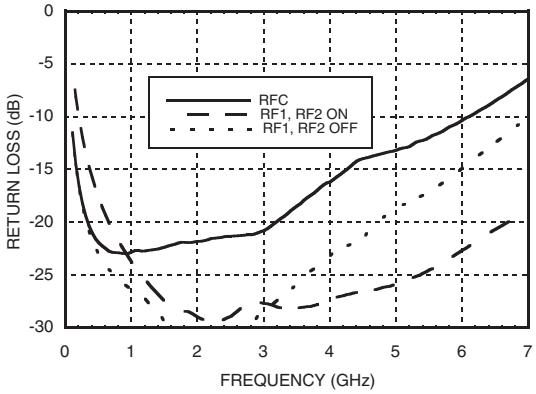
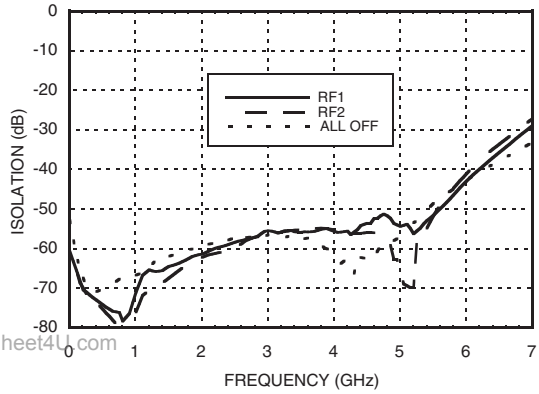
Insertion Loss



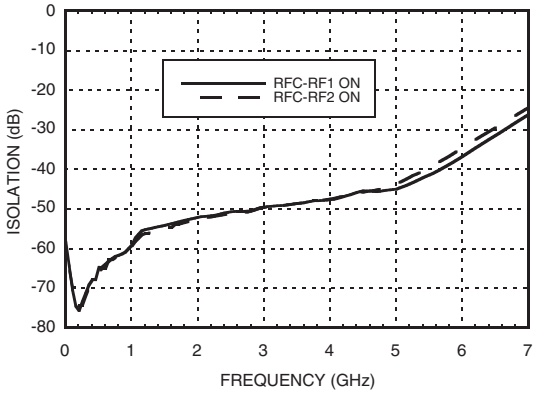
Return Loss [1]



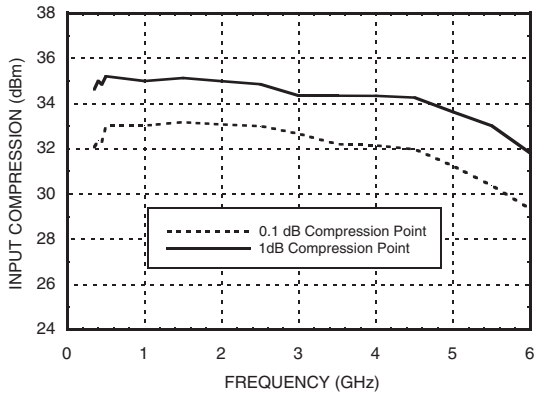
Isolation Between Ports RFC and RF1 / RF2



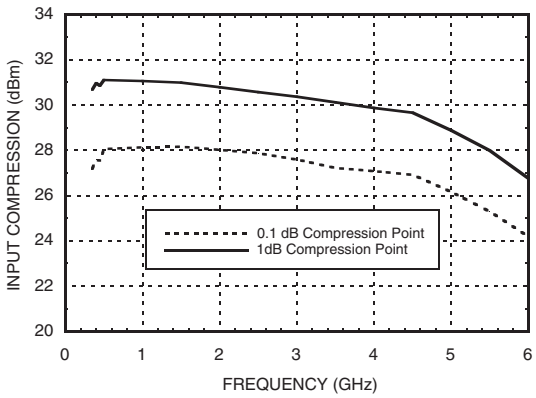
Isolation Between Ports RF1 and RF2



0.1 and 1 dB Input Compression Point, Vdd = 5V



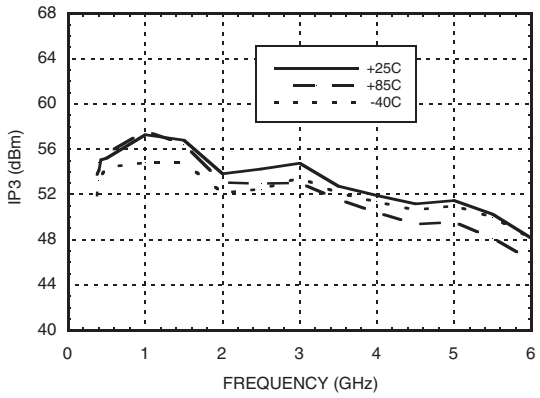
0.1 and 1 dB Input Compression Point, Vdd = 3V



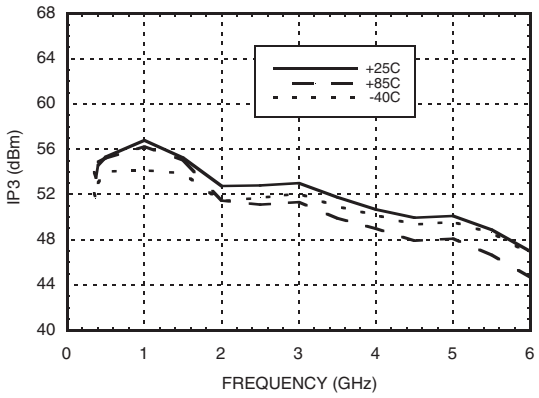
[1] RFC is reflective in “all off” state.

RoHS✓ EARTH FRIENDLY

Input Third Order Intercept Point, Vdd = 5V



Input Third Order Intercept Point, Vdd = 3V



Absolute Maximum Ratings

Bias Voltage (Vdd)	7V
Control Voltage (Vctl, EN)	-1V to Vdd +1V
RF Input Power *	
Through Path 3V/5V	30.60 / 33 dBm
Termination Path 3V/5V	26.4 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 17.6 mW/°C for through path, and 6.8 mW/°C for termination path above 85 °C)	
Through Path	1.144 W
Termination Path	0.441 W
Thermal Resistance (channel to package bottom)	
Through Path	56.8 °C/W
Termination Path	147.3 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

* The RF input power is quite lower than the breakdown power levels. Hence, the only concern with this product is the thermal limit.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Bias Voltage & Current

Vdd (V)	Idd (Typ.) (mA)
3	0.80
5	0.85

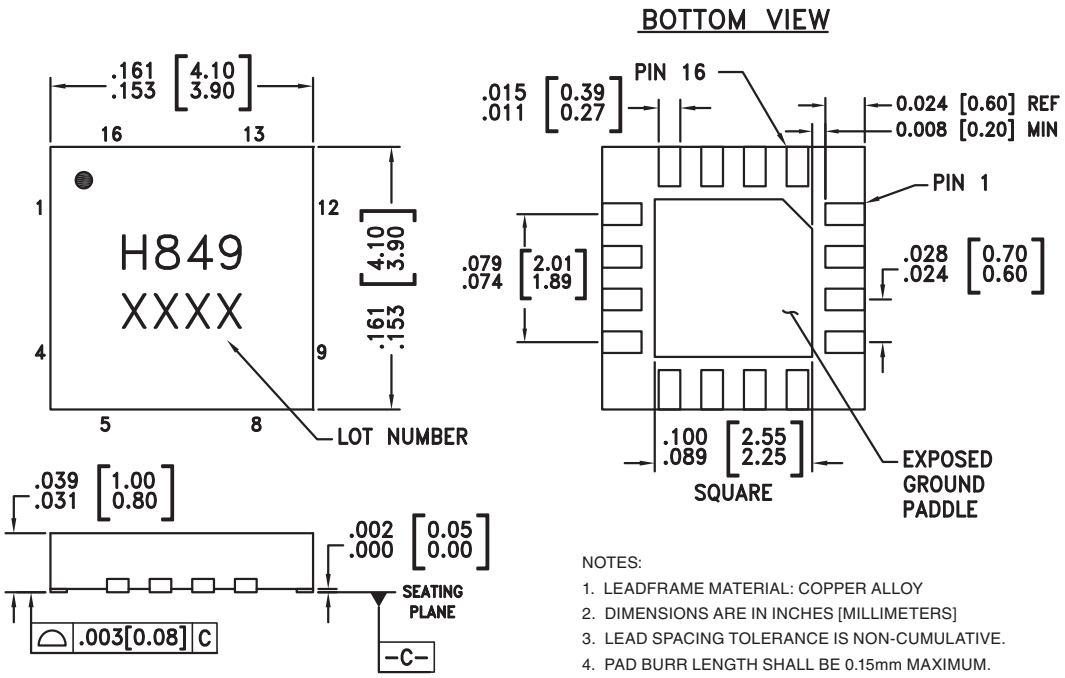
Digital Control Voltages

State	Bias Condition
Low	0 to +0.8 Vdc @ <1 µA Typical
High	+2.0 to +5.0 Vdc @ 30 µA Typical

Truth Table

Control Input		Signal Path State	
Vctl	EN	RFC - RF1	RFC - RF2
Low	Low	OFF	ON
High	Low	ON	OFF
Low	High	OFF	OFF
High	High	OFF	OFF

Outline Drawing



NOTES:

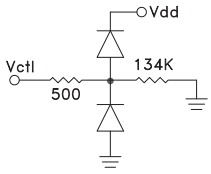
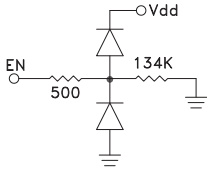
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

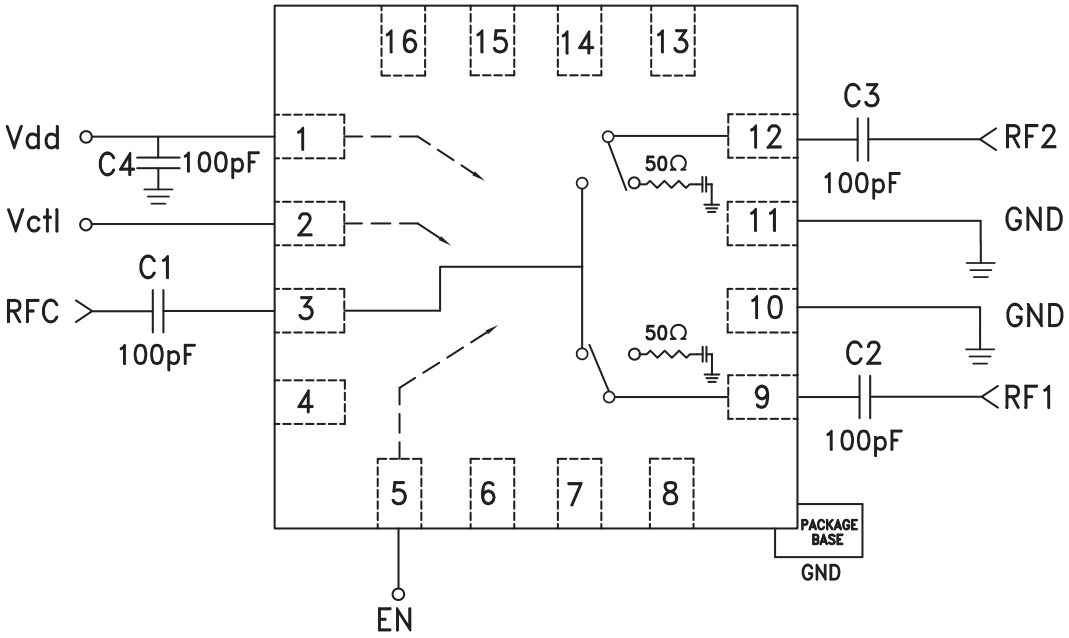
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC849LP4CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H849 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2	Vctl	Control input. See truth and control voltage tables.	
3, 9, 12	RFC, RF1, RF2	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
4, 6, 7, 8, 13, 14, 15, 16	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
5	EN	Enable. See truth and control voltage tables.	
10, 11	GND	Package bottom must also be connected to PCB RF ground.	

Application Circuit



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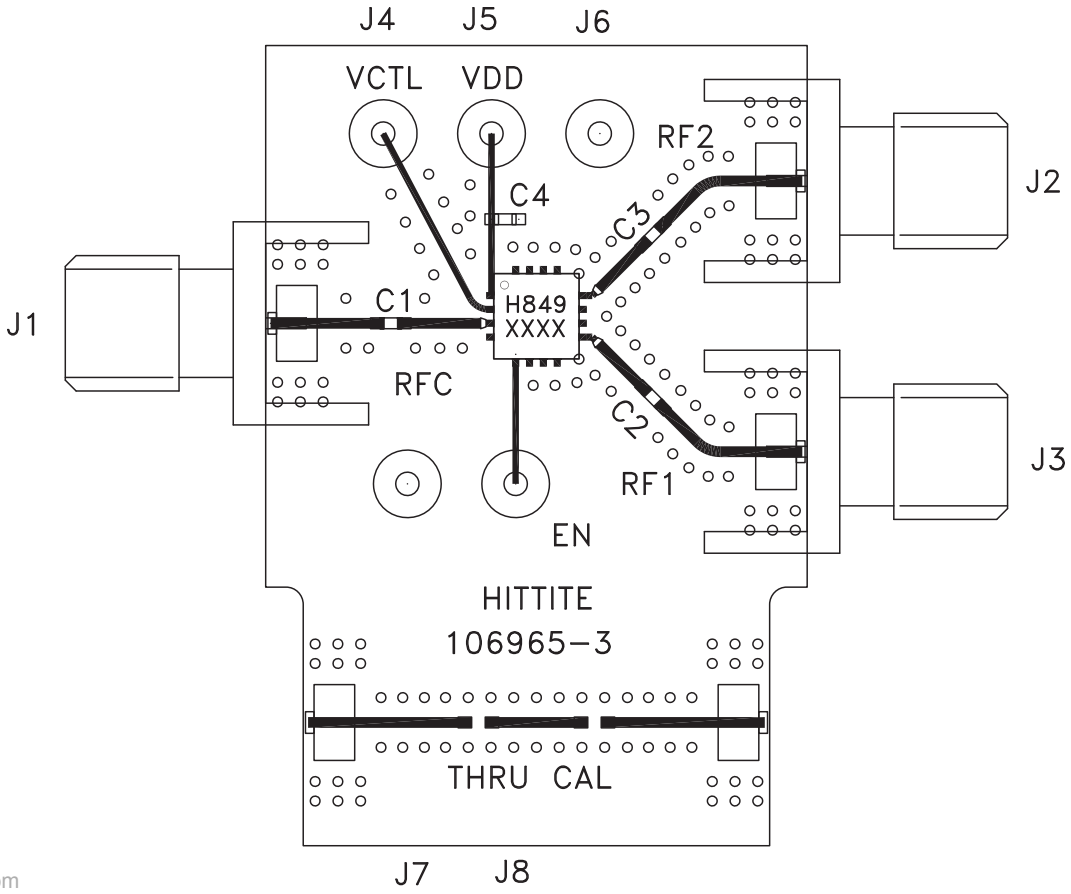
Evaluation PCB



List of Materials for Evaluation PCB 106975 [1]

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4 - J8	DC Pin
C1 - C4	100 Capacitor, 0402 Pkg.
U1	HMC849LP4CE SPDT Switch
PCB [2]	106965 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.