13 Gbps, FAST RISE TIME 1:2 FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

Typical Applications

The HMC744LC3C is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Clock Buffering up to 13 GHz

Features

Inputs Terminated Internally in 50 Ohms

Differential & Single-Ended Operation

Propagation Delay: 120 ps

Fast Rise and Fall Times: 22 / 20 ps

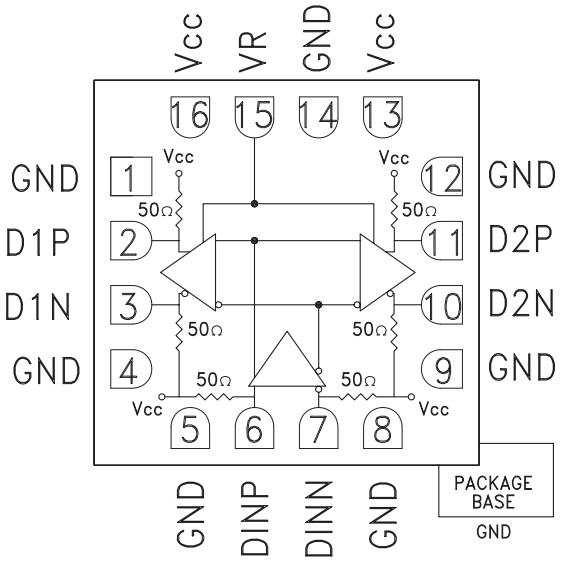
Programmable Differential
Output Voltage Swing: 600 - 1100 mV

Low Power Consumption: 287 mW typ.

Single Supply: +3.3V

16 Lead Ceramic 3x3mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC744LC3C is a 1:2 Fanout Buffer designed to support data transmission rates up to 13 Gbps, and clock frequencies as high as 13 GHz. The HMC744-LC3C also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All input and output signals to the HMC744LC3C are terminated with 50 Ohms to Vcc on-chip, and may be either AC or DC coupled. Inputs or outputs can be connected directly to a 50 Ohm to Vcc terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to ground. The HMC744LC3C operates from a single +3.3V DC supply, and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25°C Vcc = +3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		3.0	3.3	3.6	V
Power Supply Current			87		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Input High Voltage		2.8		3.8	V
Input Low Voltage		2.1		3.3	V
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVpp
	Differential, peak-to-peak		1100		mVpp
Output High Voltage			3.25		V
Output Low Voltage			2		V
Output Rise / Fall Time	Single-Ended, 20% - 80%		22 / 20		ps

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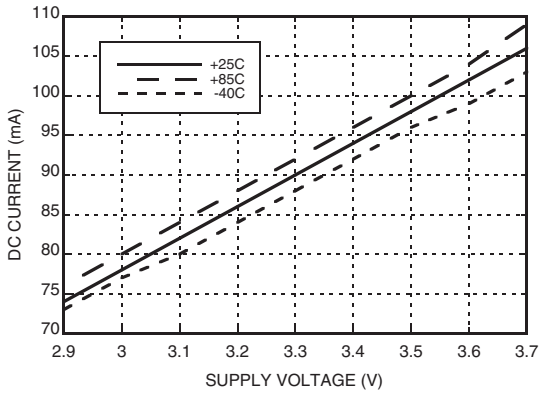
Electrical Specifications, (continued)

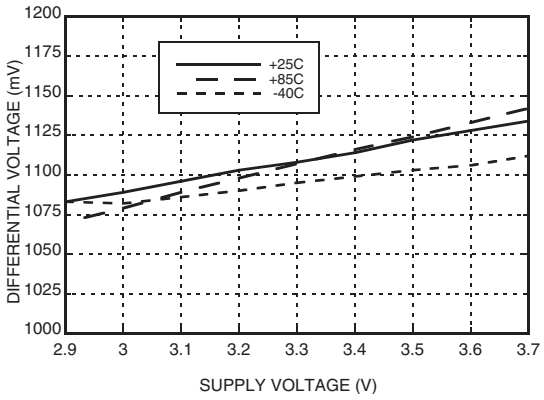
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter J_R	rms			0.2	ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [1]		2	6	ps
Propagation Delay, td			120		ps
D1 to D2 Data Skew, t_{SKEW}			0		ps

[1] Deterministic jitter measured at 13 GHz with a 300 mVpp, 2^{15}-1 PRBS input sequence.

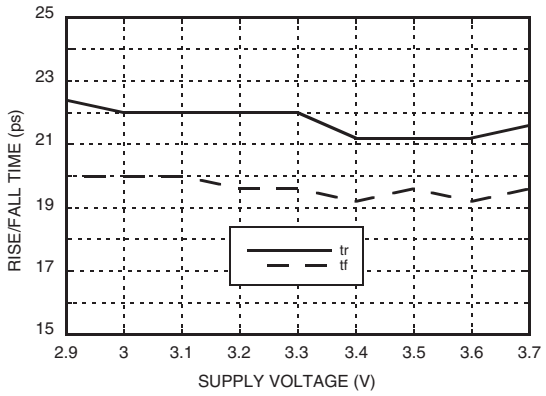
DC Current vs. Supply Voltage [1] [2]



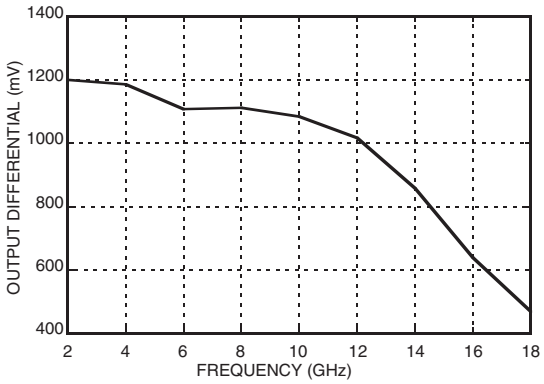
Output Differential vs. Supply Voltage [1] [2]



Rise / Fall Time vs. Supply Voltage [1] [2]



Output Differential vs. Frequency [1]



[1] VR = +3.3V [2] Frequency = 13 GHz

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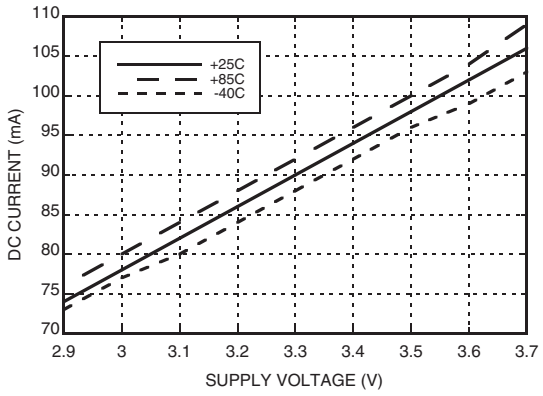
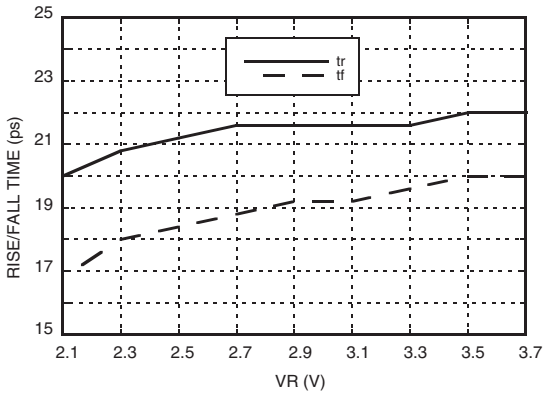
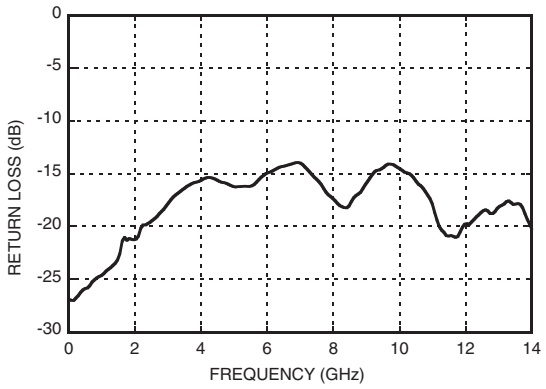
Output Differential vs. VR [2]



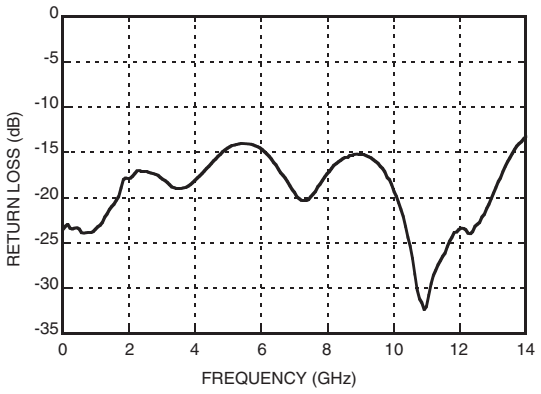
Rise / Fall Time vs. VR [2]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] VR = +3.3V [2] Frequency = 13 GHz

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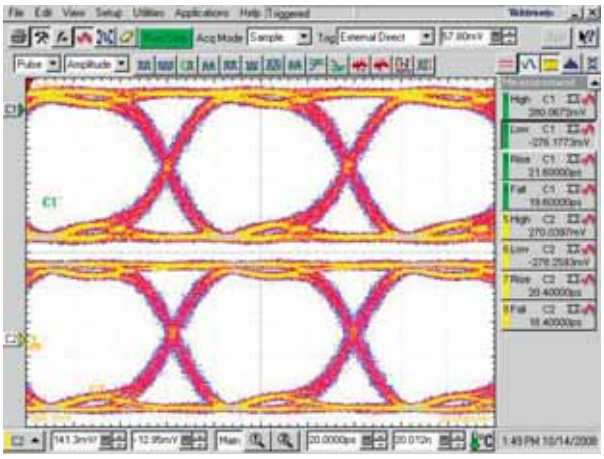
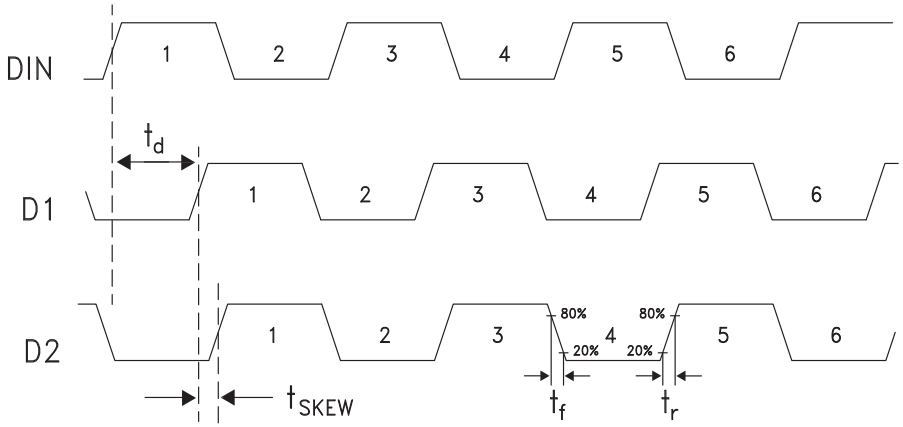
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 13 Gbps PN code. Both output channels shown.
Device is AC coupled to scope

Timing Diagram



Truth Table

Input	Outputs	
DIN	D1	D2
L	L	L
H	H	H
Notes: DIN = DINP - DINN D1 = D1P - D1N D2 = D2P - D2N	H - Positive differential voltage L - Negative differential voltage	

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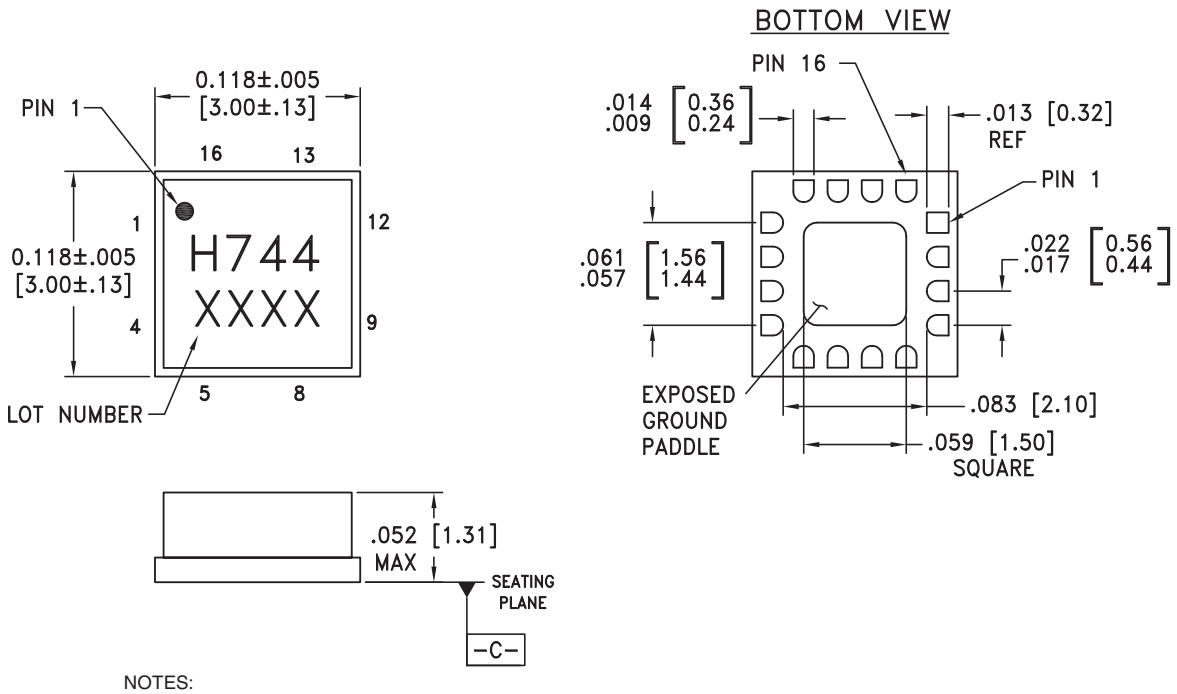
Absolute Maximum Ratings

Power Supply Voltage (Vcc)	-0.5V to +3.7V
Input Signals	Vcc - 2V to Vcc + 0.5V
Output Signals	+1V to +3.7V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

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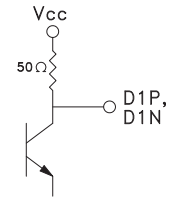
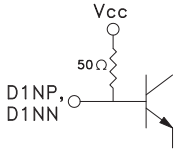
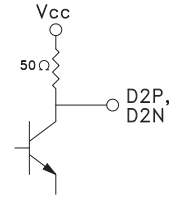
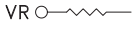
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	D1P, D1N	Clock / Data Output Port 1	
6, 7	DINP, DINN	Clock / Data Inputs	
10, 11	D2N D2P	Clock / Data Output Port 2	
13, 16	Vcc	Positive Supply	
14, Package Base	GND	Supply Ground	
15	VR	Output level control. Output level may be adjusted by applying a voltage to VR per "Output Differential vs. VR" plot.	

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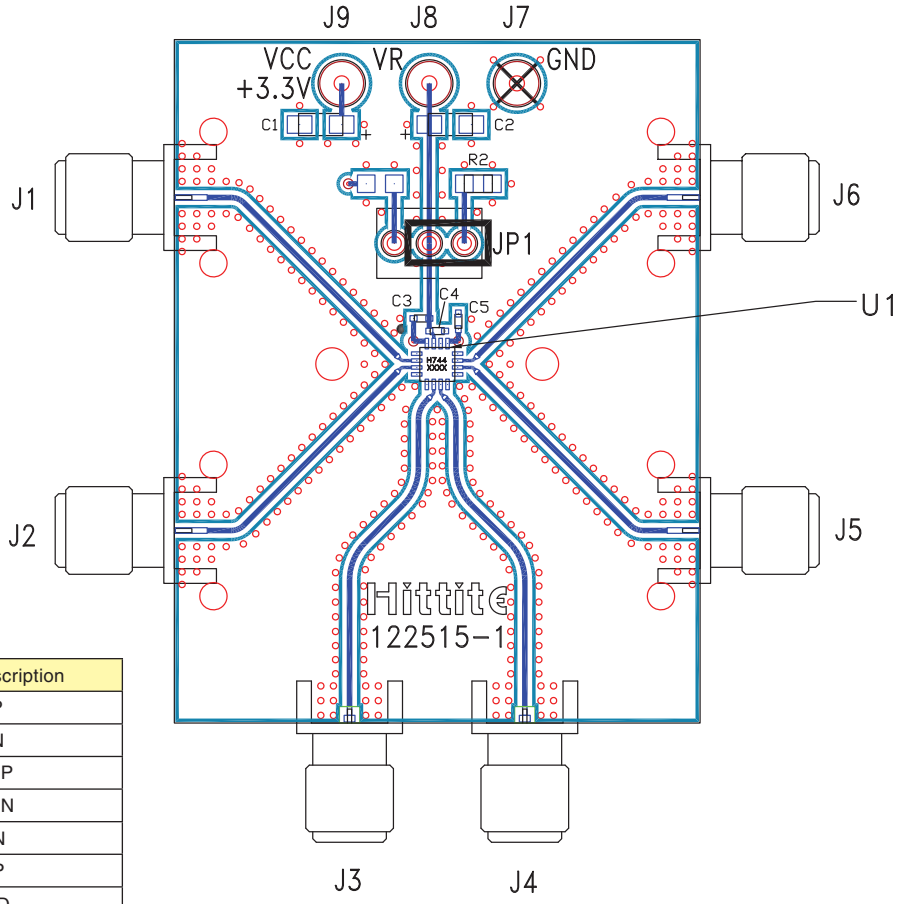
Evaluation PCB



Item	Description
J1	D1P
J2	D1N
J3	DINP
J4	DINN
J5	D2N
J6	D2P
J7	GND
J8	VR
J9	Vcc

List of Materials for Evaluation PCB 122517 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
JP1	Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R2	10 Ohm Resistor, 0603 Pkg.
U1	HMC744LC3C High Speed Logic, Fanout Buffer
PCB [2]	122515 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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Application Circuit