Three Channels Integrated Power Management IC for Handheld Portable Equipment

Features

- Three Integrated Regulators
  REG1: 600mA PWM Step-Down DC/DC
  REG2: 300mA Low Noise LDO
  REG3: 300mA Low Noise LDO
- Independent Enable/Disable Control
- Minimal External Components
- 3×3mm, Thin-DFN (TDFN3×3-10) Package
  − Only 0.75mm Height
  − RoHS Compliant

Applications

- Portable Devices and PDAs
- MP3/MP4 Players
- Wireless Handhelds
- GPS Receivers, etc.

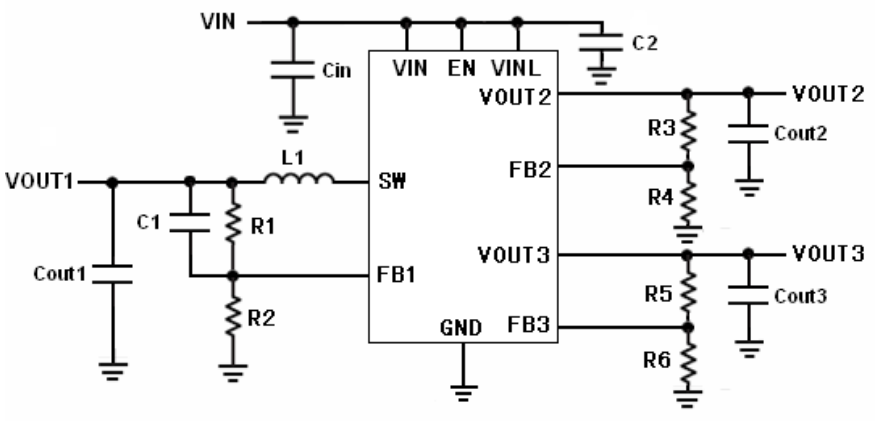
Description

The HM8332 is a complete, cost effective, highly-efficient power management solution that is ideal for a wide range of portable handheld equipment. This device integrates one PWM step-down DC/DC converter and two low noise, low dropout linear regulators (LDOs) in a single, thin, space-saving package. This device is ideal for a wide range of portable handheld equipment that can benefit from the advantages of technology but does not require a high level of integration.

REG1 is a fixed-frequency, current-mode PWM step-down DC/DC converter that is optimized for high efficiency and is capable of supplying up to 600mA output current. REG2, REG3 are low noise, high PSRR linear regulators that are capable of supplying up to 300mA, and 300mA, respectively.

The HM8332 is available in a tiny 3mm × 3mm 10-pin Thin-DFN package that is just 0.75mm thin.

Typical Application



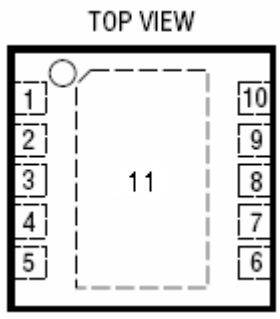
∗ Output Voltage :

REG1: V_{OUT1} = 0.625V • [1 + (R1/R2)]

REG2: V_{OUT2} = 1.212V • [1 + (R3/R4)]

REG3: V_{OUT3} = 1.212V • [1 + (R5/R6)]

Pin Assignment



DFN3*3-10

PIN NUMBER DFN3*3-10	PIN NAME	DESCRIPTION
1	VIN	Power Input for REG1
2	SW	Switching node Output for REG1
3	GND	Power Ground
4	VOUT2	Output voltage for REG2
5	FB2	Output Feedback Sense for REG2
6	VINL	Power input for REG2, REG3
7	VOUT3	Output voltage for REG3
8	FB3	Output Feedback Sense for REG3
9	EN	Enable control input for REG1，REG2, REG3
10	FB1	Output Feedback Sense for REG1
11	GND	Power Ground

Absolute Maximum Ratings

- SW to GND,VINL, VIN, FB1, FB2，FB3，VOUT2, VOUT3, EN, to GND……..……-0.3~+6V
- SW to VIN…… -6~+0.3V
- Junction to Ambient Thermal Resistance ……33℃/W
- Operating Temperature Range……-40~85℃
- Junction Temperature……125℃
- Storage Temperature…… -55~150℃
- Lead Temperature (Soldering, 10 sec)…… 300℃

Electrical Characteristics (REG1)

V_{VP1} = 3.6V, T_A = 25℃, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Operating Range		2.6		5.5	V
Quiescent Current	V_{VP1}=4.2V, I_{OUT1} =0mA		260		μA
Shutdown Current	V_{VP1}=4.2V, EN=0		0.1		μA
FB1 Voltage			0.625		V
Load Current Limit		450	600		mA
Oscillator Frequency	V_{OUT1} ≥ 1.2V	0.8	1.2	1.5	MHz
	V_{OUT1} = 0V		0.53		
PMOS Switch On Resistance	I_{SW} = -100mA		0.45	0.75	Ω
NMOS Switch On Resistance	I_{SW} =100mA		0.3	0.45	Ω
SW Leakage Current	V_{VP1} =5.5V, V_{SW} =5.5V or 0V			1	μA
Thermal Shutdown Temperature	Temperature Rising		160		℃
Thermal Shutdown Hysterics	Temperature Falling		20		℃

Electrical Characteristics (REG2，REG3)

V_{INL} = 3.6V, C_{OUT2} = 1μF, T_A = 25℃, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Operating Range		2		5.5	V
Output Voltage Regulation Accuracy	T_A=25℃	-1.2	$V_{OUT2,3}$	+2	%
Supply Current Per Output	Regulator Enabled		50		μA
	Regulator Disabled		0		
FB2,3 Voltage			1.212		V
Output Current Limit			300		mA
Stable $C_{OUT2,3}$ Range		1		20	μF
Thermal Shutdown Temperature	Temperature Rising		160		℃
Thermal Shutdown Hysterics	Temperature Falling		20		℃

Application Information

VIN (PIN1): Power Input for REG1. Bypass to GND with a high quality ceramic capacitor placed as close as possible to the REG1.

SW (PIN2): Switching node Output for REG1. Connect this pin to the switching end of the inductor.

GND (PIN3): Power Ground, as close to the IC as possible.

VOUT2 (PIN4): Output voltage for REG2, capable of delivering up to 300mA of output current.

FB2 (PIN5): Output Feedback Sense. Receives the feedback voltage from an external resistive divider across the output. The output voltage for REG1 is set by a resistive divider according to the following formula: V_{OUT2} = 1.212V • [1 + (R3/R4)].

VINL (PIN6): Power input for REG2, REG3. Bypass to GND with a high quality ceramic capacitor placed as close as possible to the IC.

VOUT3 (PIN7): Output voltage for REG3, capable of delivering up to 300mA of output current.

FB3 (PIN8): Output Feedback Sense. Receives the feedback voltage from an external resistive divider across the output. The output voltage for REG3 is set by a resistive divider according to the following

formula: V_{OUT3} = 1.212V • [1 + (R5/R6)].

EN (PIN9): Enable control input for REG1, REG2, and REG3. Drive EN to the VIN, VINL or a logic high for normal operation, drive EN to GND or a logic low to disable REG1, REG2, and REG3.

FB1 (PIN10): Output Feedback Sense. Receives the feedback voltage from an external resistive divider across the output. The output voltage for REG1 is set by a resistive divider according to the following formula: V_{OUT1} = 0.625V • [1 + (R1/R2)].

GND (PIN11): Power Ground.

Application Information

The basic HM8332 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by CIN and COUT.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 4.7μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation (1). A reasonable starting point for setting ripple current is $\triangle I_L$ = 240mA (40% of 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 0.9A rated inductor should be enough for most applications (600mA + 120mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the HM8332 requires to operate. Table 1 shows some typical surface mount inductors that work well in HM8332 applications.

Table1: Suggested Inductors

Component Supplier	Series	Inductance (uH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR 3015	2.2	60	1480	3 x 3 x 1.5
TAIYO YUDEN	NR 3015	4.7	120	1020	3 x 3 x 1.5
Sumida	CDRH2D14	2.2	75	1500	4.5 x 3.2 x 1.55
Sumida	CDRH2D14	4.7	135	1000	4.5 x 3.2 x 1.55
GOTREND	GTSD32	2.2	58	1500	3.85 x 3.85 x 1.8
GOTREND	GTSD32	4.7	146	1100	3.85 x 3.85 x 1.8

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX}\frac{\left[V_{OUT}(V_{IN}-V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies.

An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Efficiency Considerations

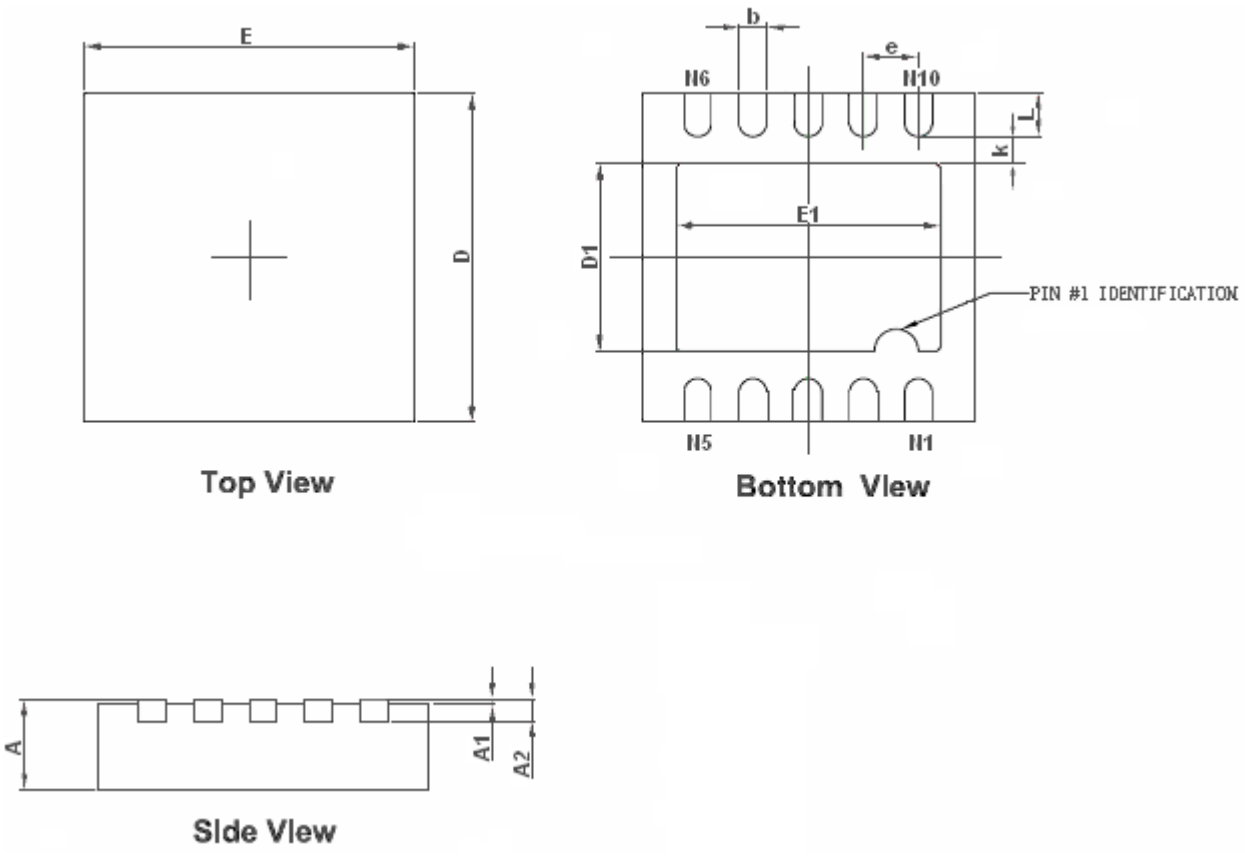
The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge $\triangle Q$ moves from VIN to ground. The resulting $\triangle Q/\triangle t$ is the current out of VIN that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f (Q_T+Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP}$ x DC + $R_{DS(ON)BOT}$ x (1-DC) The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Packaging Information

DFN3*3-10 Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A2	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
k	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020