# HM62W16255HI Series

4M High Speed SRAM (256-kword × 16-bit)

HITACHI

ADE-203-1038B (Z)
Rev. 2.0
Jan. 20, 2000

## Description

The HM62W16255HI is a 4-Mbit high speed static RAM organized 256-kword × 16-bit. It has realized high speed access time by employing CMOS process (4-transistor + 2-poly resistor memory cell)and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 44-pin SOJ and 400-mil 44-pin plastic TSOPII.

## Features

- Single 3.3 V supply: 3.3 V ± 0.3V
- Access time: 15 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- Operating current: 160 mA (max)
- TTL standby current: 50 mA (max)
- CMOS standby current: 5 mA (max)
- Center $V_{CC}$ and $V_{SS}$ type pinout
- Temperature range: –40 to 85°C

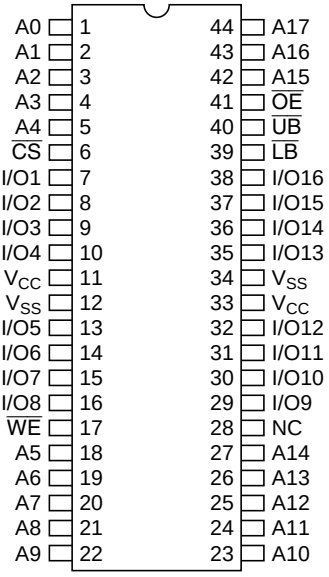
Hitachi semiconductor

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM62W16255HJPI-15 | 15 ns | 400-mil 44-pin plastic SOJ (CP-44D) |
| HM62W16255HTTI-15 | 15 ns | 400-mil 44-pin plastic TSOPII (TTP-44DE) |

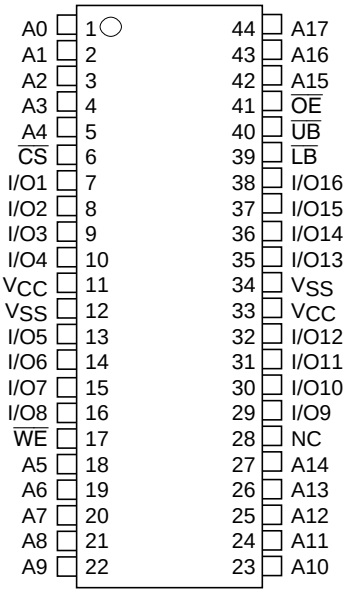
## Pin Arrangement

HM62W16255HJPI Series




(Top View)

HM62W16255HTTI Series

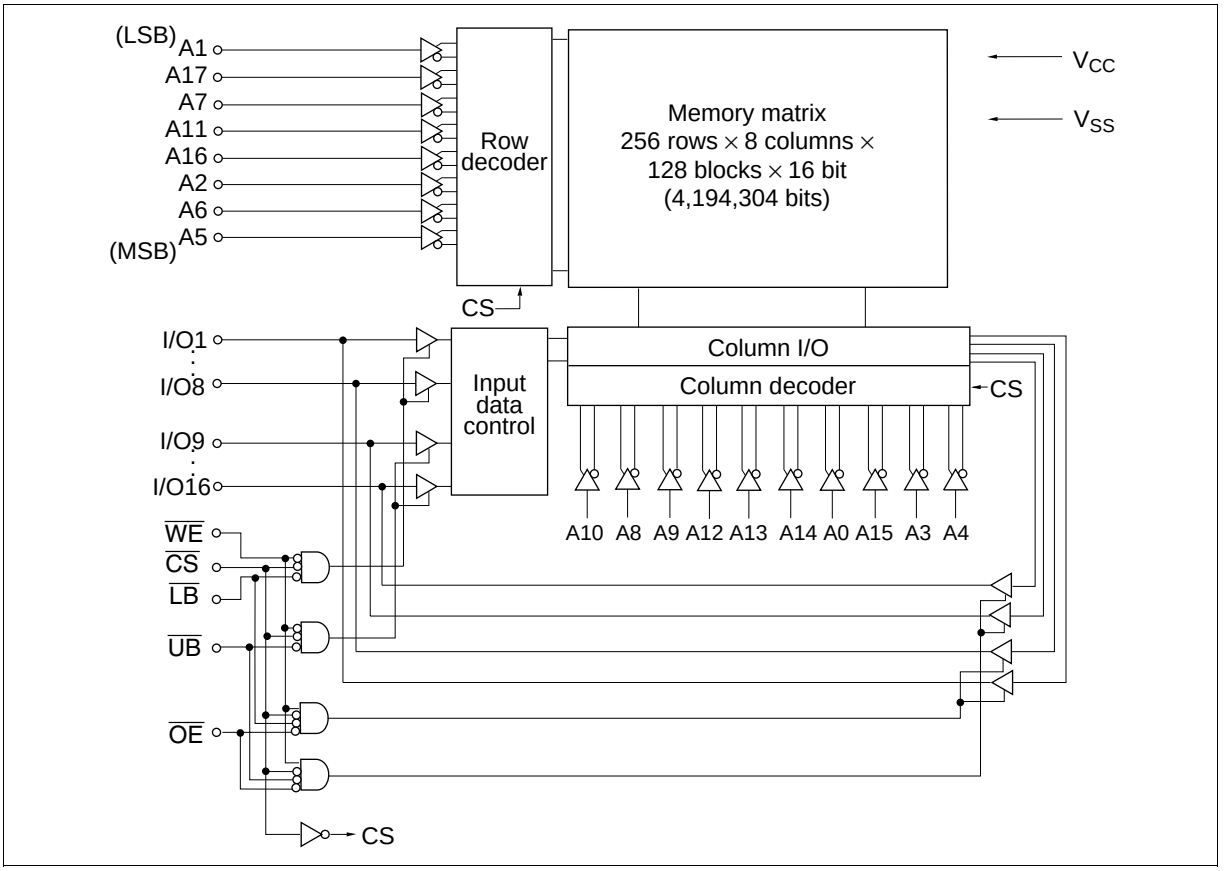



(Top View)

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A17 | Address input |
| I/O1 to I/O16 | Data input/output |
| $\overline{CS}$ | Chip select |
| $\overline{OE}$ | Output enable |
| $\overline{WE}$ | Write enable |
| $\overline{UB}$ | Upper byte select |
| $\overline{LB}$ | Lower byte select |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

## Block Diagram



## Operation Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | Mode | $V_{CC}$ current | I/O1–I/O8 | I/O9–I/O16 | Ref. cycle |
|---|---|---|---|---|---|---|---|---|---|
| H | × | × | × | × | Standby | $I_{SB}$, $I_{SB1}$ | High-Z | High-Z | — |
| L | H | H | × | × | Output disable | $I_{CC}$ | High-Z | High-Z | — |
| L | L | H | L | L | Read | $I_{CC}$ | Output | Output | Read cycle |
| L | L | H | L | H | Lower byte read | $I_{CC}$ | Output | High-Z | Read cycle |
| L | L | H | H | L | Upper byte read | $I_{CC}$ | High-Z | Output | Read cycle |
| L | L | H | H | H | — | $I_{CC}$ | High-Z | High-Z | — |
| L | × | L | L | L | Write | $I_{CC}$ | Input | Input | Write cycle |
| L | × | L | L | H | Lower byte write | $I_{CC}$ | Input | High-Z | Write cycle |
| L | × | L | H | L | Upper byte write | $I_{CC}$ | High-Z | Input | Write cycle |
| L | × | L | H | H | — | $I_{CC}$ | High-Z | High-Z | — |

Note: ×: H or L

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +4.6 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5*[1] to $V_{CC}$ + 0.5*[2] | V |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | –40 to +85 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –40 to +85 | °C |

Notes: 1. $V_T$ (min) = –2.0 V for pulse width (under shoot) ≤ 8 ns
2. $V_T$ (max) = $V_{CC}$ + 2.0 V for pulse width (over shoot) ≤ 8 ns

## Recommended DC Operating Conditions (Ta = –40 to +85°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$*3 | 3.0 | 3.3 | 3.6 | V |
| | $V_{SS}$*4 | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.5*2 | V |
| | $V_{IL}$ | –0.5*1 | — | 0.8 | V |

Notes: 1. $V_{IL}$ (min) = –2.0 V for pulse width (under shoot) ≤ 8 ns
2. $V_{IH}$ (max) = $V_{CC}$ + 2.0 V for pulse width (over shoot) ≤ 8 ns
3. The supply voltage with all $V_{CC}$ pins must be on the same level.
4. The supply voltage with all $V_{SS}$ pins must be on the same level.

## DC Characteristics (Ta = –40 to +85°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)

| Parameter | | Symbol | Min | Typ*1 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | | $\|I_{LI}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Output leakage current*1 | | $\|I_{LO}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Operating power supply current | 15 ns cycle | $I_{CC}$ | — | — | 160 | mA | Min cycle<br>$\overline{CS}$ = $V_{IL}$, Iout = 0 mA<br>Other inputs = $V_{IH}$/$V_{IL}$ |
| Standby power supply current | 15 ns cycle | $I_{SB}$ | — | — | 50 | mA | Min cycle, $\overline{CS}$ = $V_{IH}$,<br>Other inputs = $V_{IH}$/$V_{IL}$ |
| | | $I_{SB1}$ | — | 0.05 | 5 | mA | f = 0 MHz<br>$V_{CC} \geq \overline{CS} \geq V_{CC}$ – 0.2 V,<br>(1) 0 V ≤ Vin ≤ 0.2 V or<br>(2) $V_{CC}$ ≥ Vin ≥ $V_{CC}$ – 0.2 V |
| Output voltage | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA |
| | | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –4 mA |

Note: 1. Typical values are at $V_{CC}$ = 3.3 V, Ta = +25°C and not guaranteed.

## Capacitance (Ta = +25°C, f = 1.0 MHz)

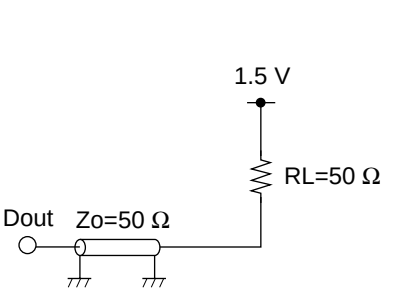
| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input capacitance*1 | Cin | — | — | 6 | pF | Vin = 0 V |
| Input/output capacitance*1 | $C_{I/O}$ | — | — | 8 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

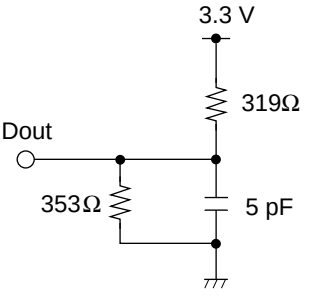
## AC Characteristics (Ta = –40 to +85°C, $V_{CC}$ = 3.3 V ± 0.3 V, unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)




Output load (A)




Output load (B)
(for $t_{CLZ}$, $t_{OLZ}$, $t_{LBLZ}$, $t_{UBLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{LBHZ}$, $t_{UBHZ}$, $t_{WHZ}$, and $t_{OW}$)

### Read Cycle

| | | HM62W16255HI | | | |
|---|---|---|---|---|---|
| | | -15 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Read cycle time | $t_{RC}$ | 15 | — | ns | |
| Address access time | $t_{AA}$ | — | 15 | ns | |
| Chip select access time | $t_{ACS}$ | — | 15 | ns | |
| Output enable to output valid | $t_{OE}$ | — | 7 | ns | |
| Byte select to output valid | $t_{LB}$, $t_{UB}$ | — | 7 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | — | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 3 | — | ns | 1 |
| Output enable to output in low-Z | $t_{OLZ}$ | 0 | — | ns | 1 |
| Byte select to output in low-Z | $t_{LBLZ}$, $t_{UBLZ}$ | 0 | — | ns | 1 |
| Chip deselect to output in high-Z | $t_{CHZ}$ | — | 7 | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 7 | ns | 1 |
| Byte deselect to output in high-Z | $t_{LBHZ}$, $t_{UBHZ}$ | — | 7 | ns | 1 |

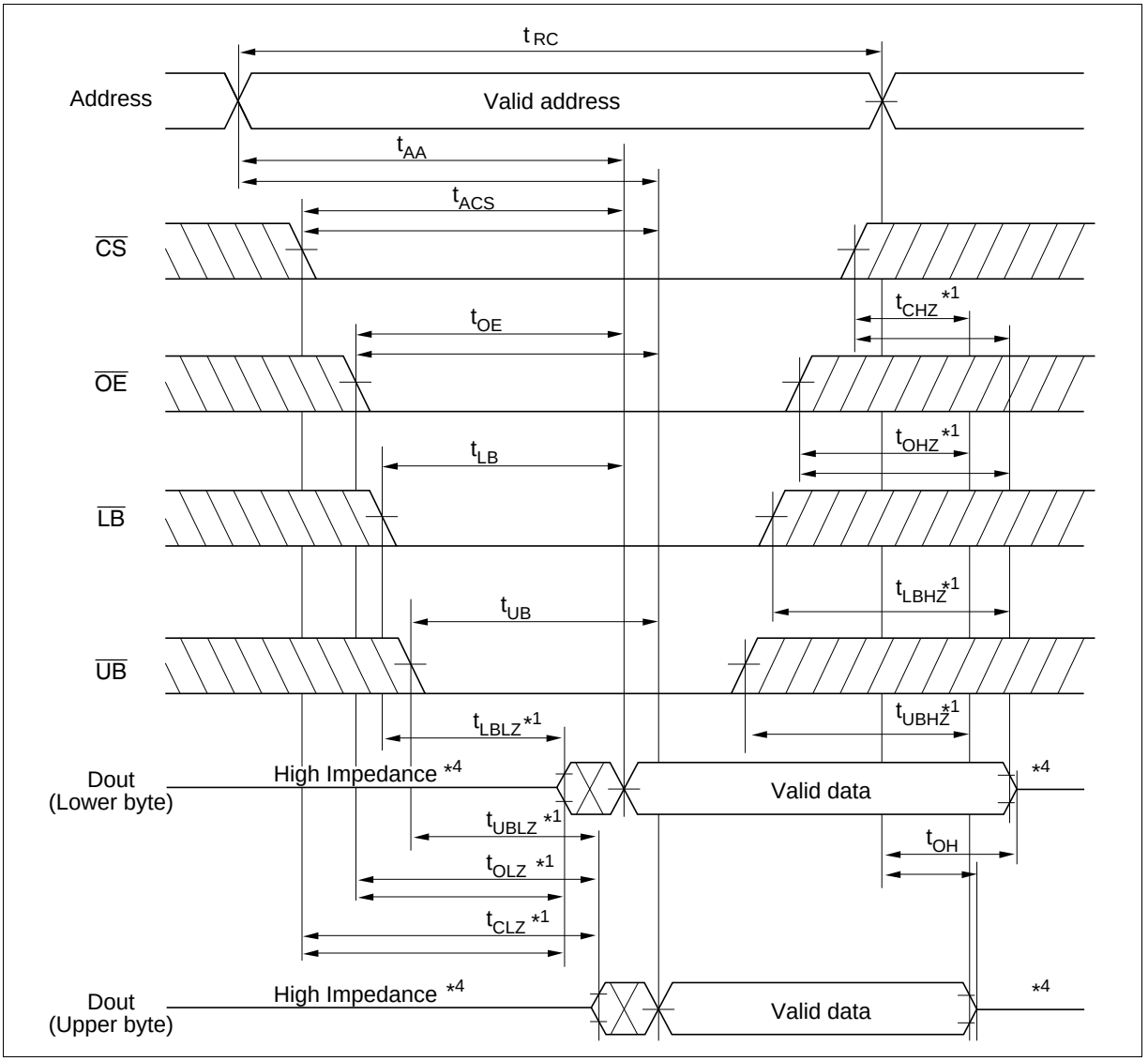
## Write Cycle

| | | HM62W16255HI | | | |
|---|---|---|---|---|---|
| | | -15 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Write cycle time | $t_{WC}$ | 15 | — | ns | |
| Address valid to end of write | $t_{AW}$ | 10 | — | ns | |
| Chip select to end of write | $t_{CW}$ | 10 | — | ns | 8 |
| Write pulse width | $t_{WP}$ | 10 | — | ns | 7 |
| Byte select to end of write | $t_{LBW}$, $t_{UBW}$ | 10 | — | ns | 9, 10 |
| Address setup time | $t_{AS}$ | 0 | — | ns | 5 |
| Write recovery time | $t_{WR}$ | 0 | — | ns | 6 |
| Data to write time overlap | $t_{DW}$ | 7 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | ns | |
| Write disable to output in low-Z | $t_{OW}$ | 3 | — | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 7 | ns | 1 |
| Write enable to output in high-Z | $t_{WHZ}$ | — | 7 | ns | 1 |

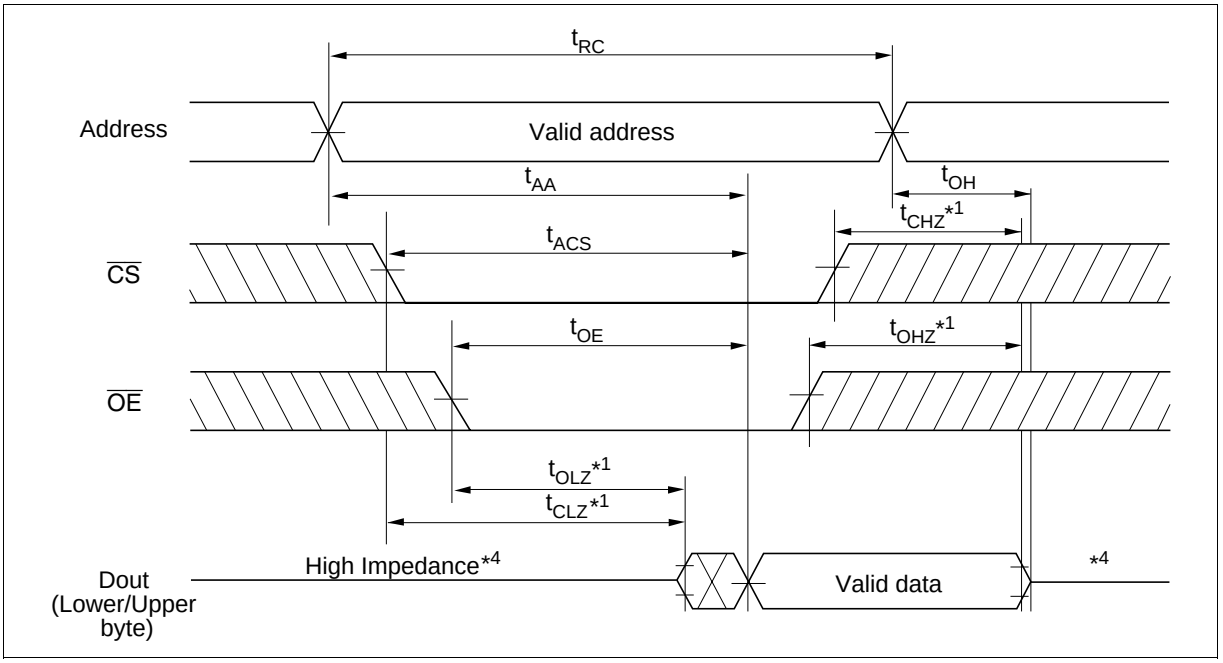
Notes:
1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
4. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. $t_{AS}$ is measured from the latest address transition to the latest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going low.
6. $t_{WR}$ is measured from the earliest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going high to the first address transition.
7. A write occurs during the overlap of low $\overline{CS}$, low $\overline{WE}$ and low $\overline{LB}$ or low $\overline{UB}$.
8. $t_{CW}$ is measured from the later of $\overline{CS}$ going low to the end of write.
9. $t_{LBW}$ is measured from the later of $\overline{LB}$ going low to the end of write.
10. $t_{UBW}$ is measured from the later of $\overline{UB}$ going low to the end of write.

## Timing Waveforms

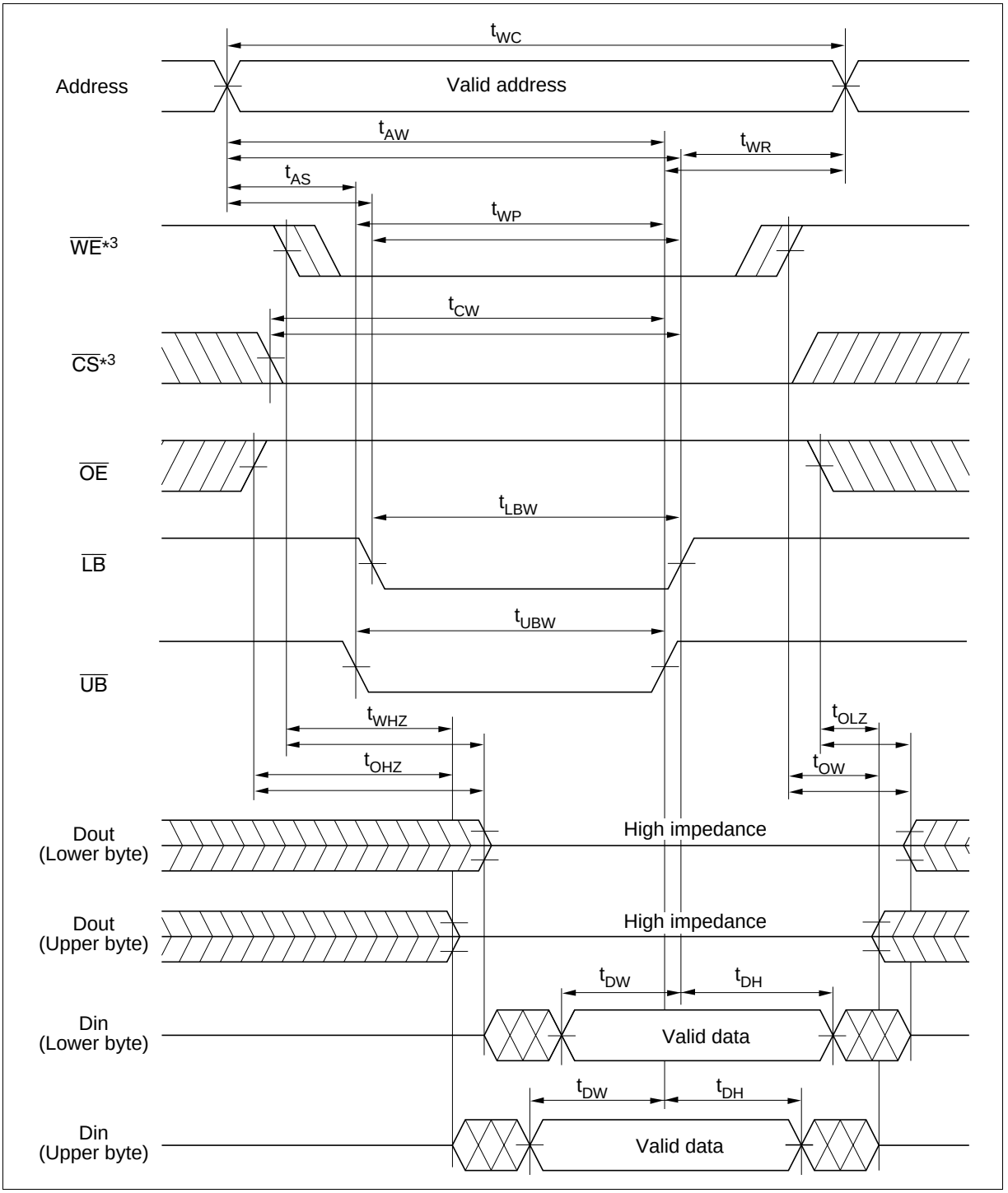
**Read Timing Waveform (1)** ($\overline{WE}$ = $V_{IH}$)



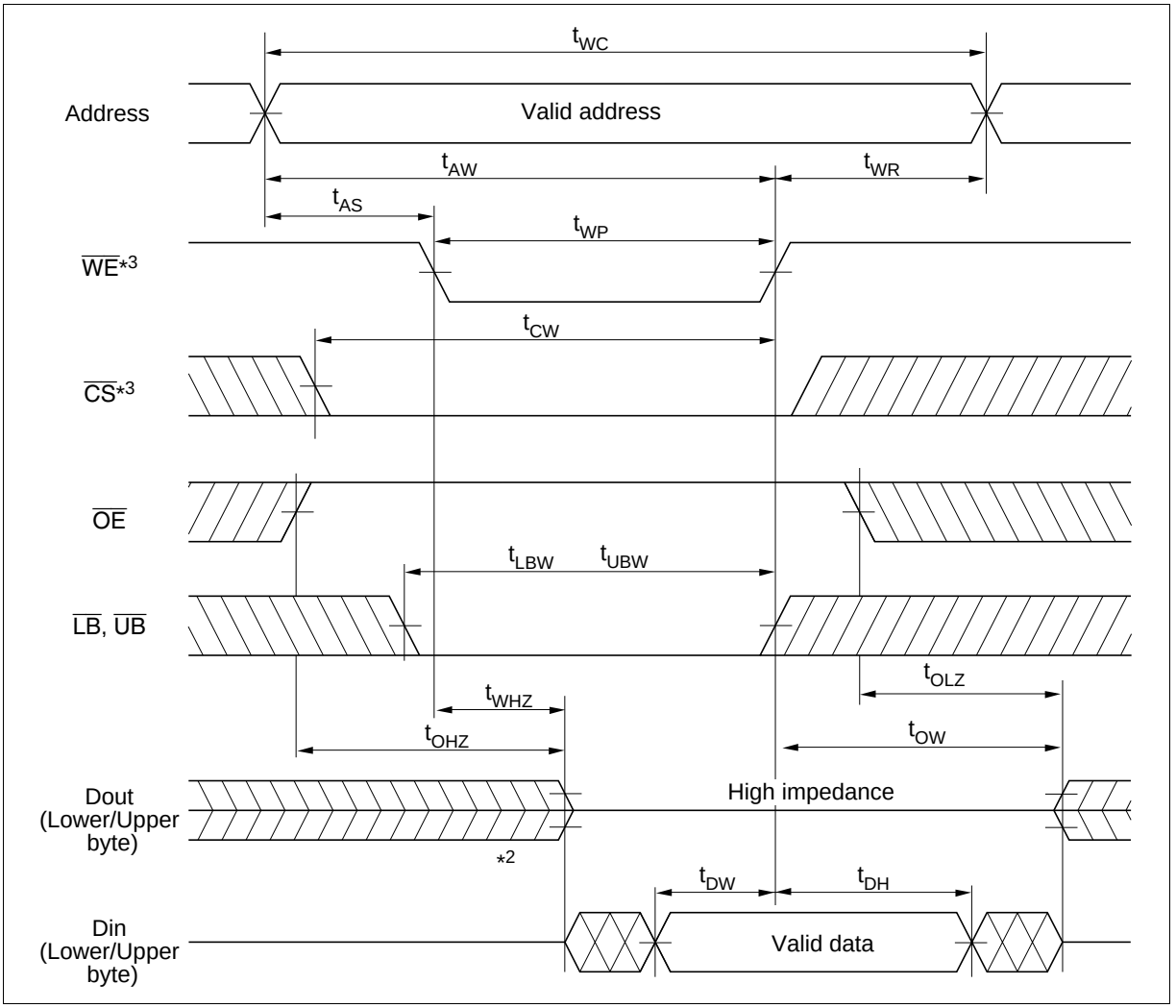
**Read Timing Waveform (2)** ($\overline{WE}$ = $V_{IH}$, $\overline{LB}$ = $V_{IL}$, $\overline{UB}$, = $V_{IL}$)



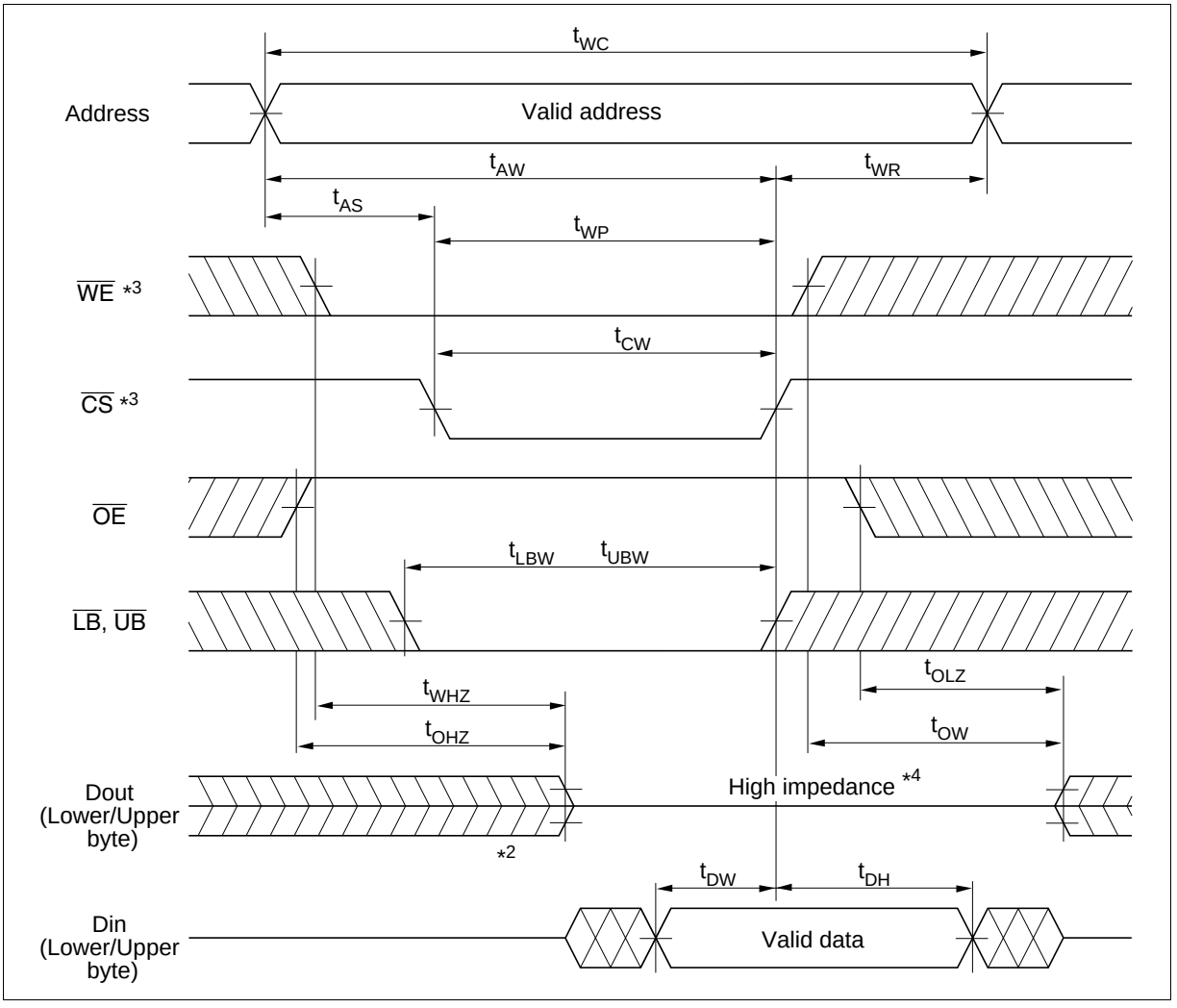
**Write Timing Waveform (1)** ($\overline{LB}$, $\overline{UB}$ Controlled)



**Write Timing Waveform (2)** ($\overline{WE}$ Controlled)



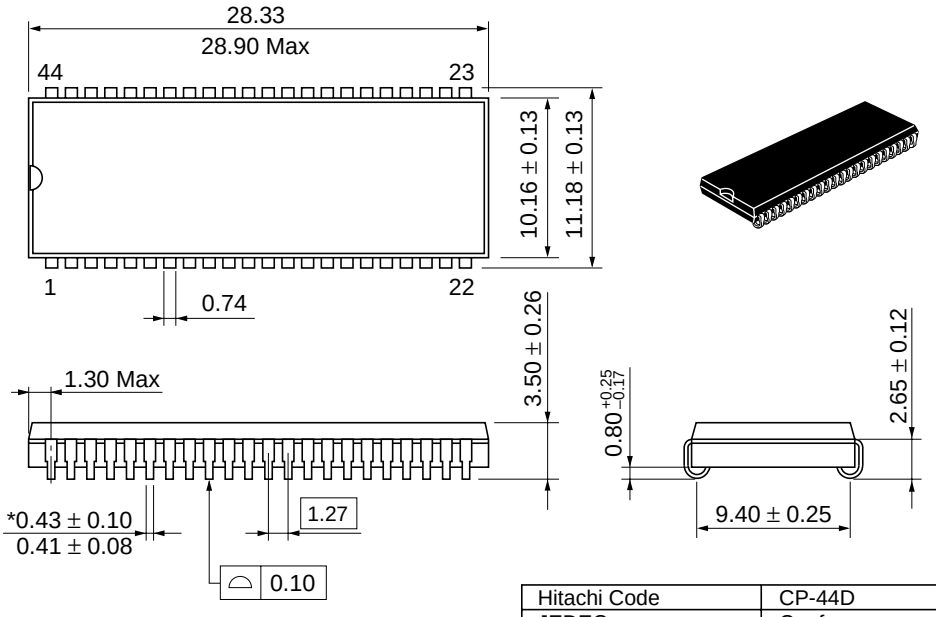
**Write Timing Waveform (3)** ($\overline{CS}$ Controlled)



## Package Dimensions

**HM62W16255HJPI Series** (CP-44D)

Unit: mm

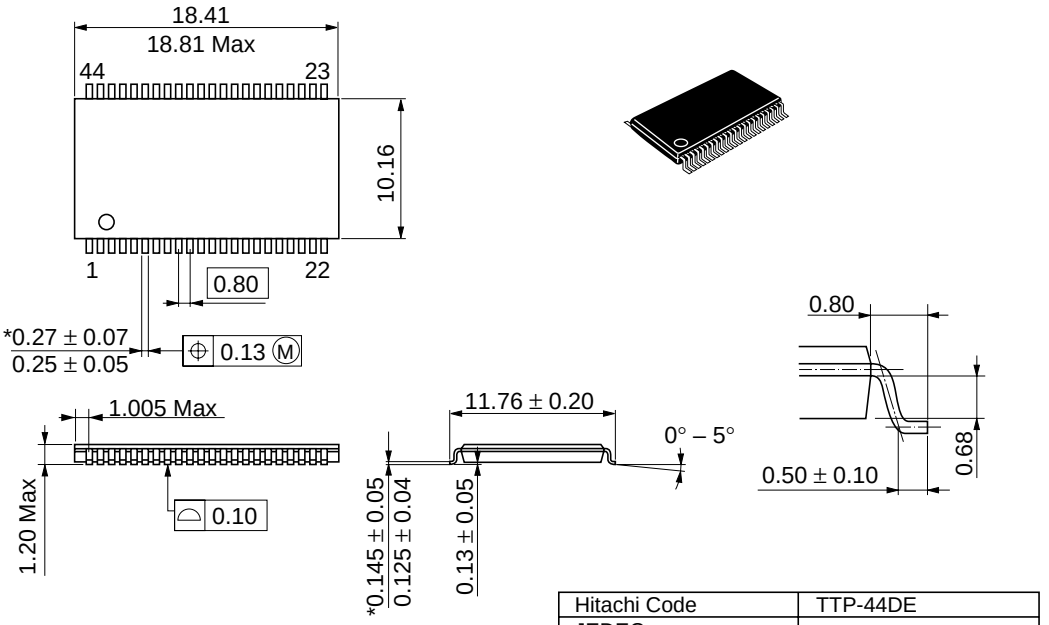



| | |
|---|---|
| Hitachi Code | CP-44D |
| JEDEC | Conforms |
| EIAJ | — |
| Weight (reference value) | 1.8 g |

*Dimension including the plating thickness
Base material dimension

**HM62W16255HTTI Series** (TTP-44DE)

Unit: mm




*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | TTP-44DE |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.43 g |

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/index.htm

**For further information write to:**

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

## Revision Record

| Rev. | Date | Contents of Modification | Drawn by | Approved by |
|---|---|---|---|---|
| 1.0 | Apr. 15, 1999 | Initial issue | T. Fukazawa | K. Makuta |
| 2.0 | Jan. 20, 2000 | Ordering information: Correct error | | |