
HM5212325F-B60

128M LVTTL interface SDRAM

100 MHz

1-Mword $\times$ 32-bit $\times$ 4-bank

PC/100 SDRAM

HITACHI

ADE-203-1053A (Z)

Rev. 1.0

Oct. 18, 1999

Description

The Hitachi HM5212325F is a 128-Mbit SDRAM organized as 1048576-word $\times$ 32-bit $\times$ 4-bank. All inputs and outputs are referred to the rising edge of the clock input. It is packaged in standard 108 bump BGA.

Features

- Single chip wide bit solution ($\times$ 32)
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTL interface
- Extremely small foot print: 1.27 mm pitch
 - Package: BGA (BP-108)
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 4/8/full page
- 2 variations of burst sequence
 - Sequential (BL = 4/8/full page)
 - Interleave (BL = 4/8)
- Programmable $\overline{\text{CAS}}$ latency: 2/3
- Byte control by DQMB
- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
 - Auto refresh
 - Self refresh

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- Full page burst length capability
 - Sequential burst
 - Burst stop capability

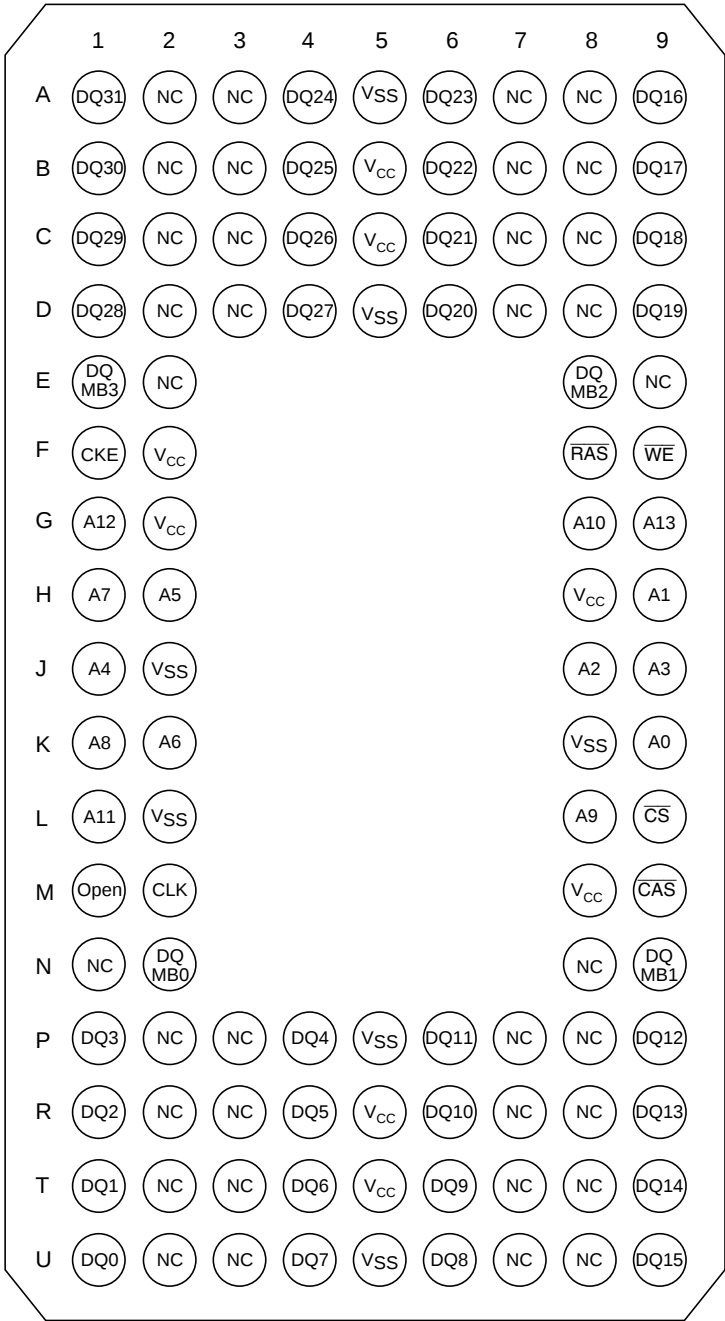
Ordering Information

Type No.	Frequency	CAS latency	Package
HM5212325FBP-B60*	100 MHz	3	14 mm × 22 mm 108 bump BGA (BP-108)

Note: 66 MHz operation at CAS latency = 2.

Pin Arrangement

108-bump BGA



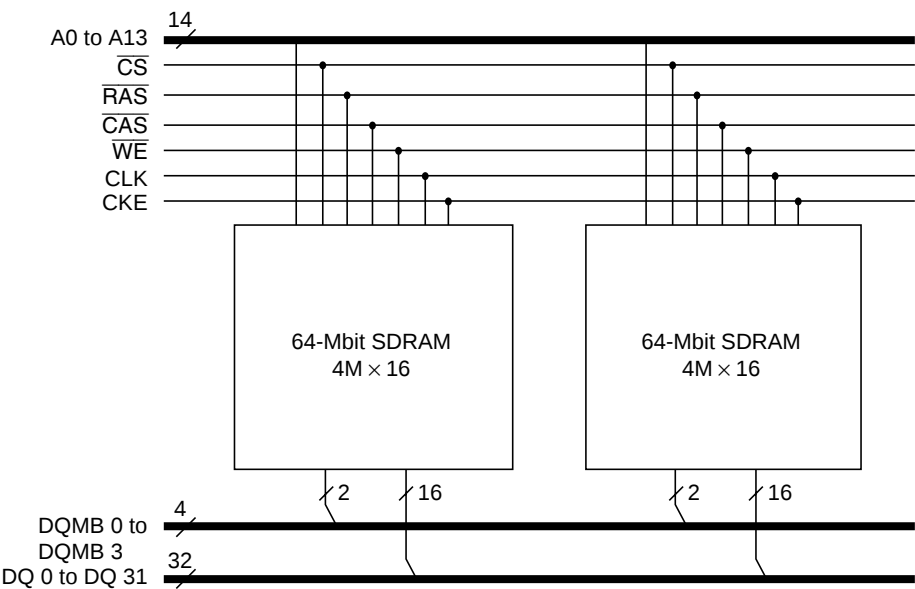
(Top view)

Pin Description

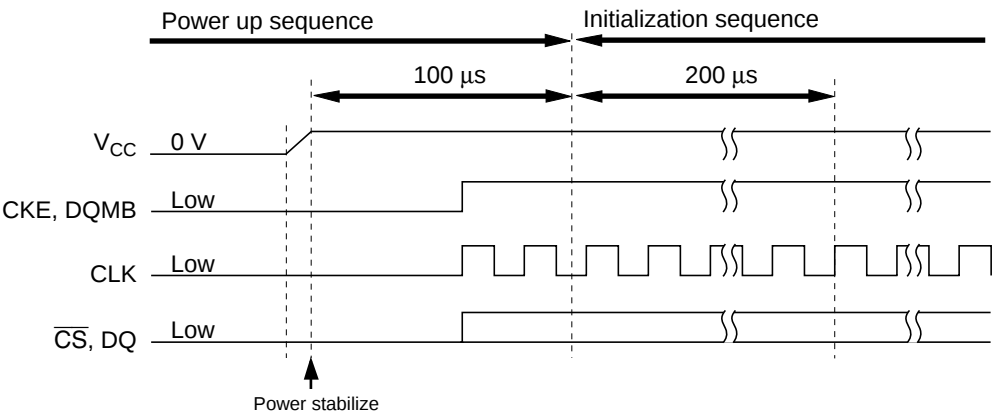
Pin name	Function
A0 to A13	Address input Row address A0 to A11 Column address A0 to A7 Bank select address A12/A13 (BS)
DQ0 to DQ31	Data-input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{RAS}}$	Row address strobe command
$\overline{\text{CAS}}$	Column address strobe command
$\overline{\text{WE}}$	Write enable
DQMB0 to DQMB3	Byte data mask* ¹
CLK	Clock input
CKE	Clock enable
V_{cc}	Power supply
V_{ss}	Ground
Open	Open* ²

Note: 1. DQMB0: DQ0 to DQ7
 DQMB1: DQ8 to DQ15
 DQMB2: DQ16 to DQ23
 DQMB3: DQ24 to DQ31
 2. Don't connect. Internally connected with die.

Block Diagram



Power-up Sequence and Initialization Sequence



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V _{SS}	V _T	−0.5 to V _{CC} + 0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to V _{SS}	V _{CC}	−0.5 to +4.6	V	1
Short circuit output current	I _{out}	50	mA	
Operating temperature	T _{opr}	0 to +70 (T _j max = 110)	°C	
Storage temperature	T _{stg}	−55 to +125	°C	

Note: 1. Respect to V_{SS}.

DC Operating Conditions (T_{case} = 0 to +70°C [T_j max = 110°C])

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V _{CC}	3.0	3.6	V	1, 2
	V _{SS}	0	0	V	3
Input high voltage	V _{IH}	2.0	V _{CC} + 0.3	V	1, 4
Input low voltage	V _{IL}	−0.3	0.8	V	1, 5

- Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.
4. V_{IH} (max) = V_{CC} + 2.0 V for pulse width ≤ 3 ns at V_{CC}.
5. V_{IL} (min) = V_{SS} − 2.0 V for pulse width ≤ 3 ns at V_{SS}.

DC Characteristics

(T_{case} = 0 to +70°C [T_j max = 110°C]), V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HM5212325F				
		-B60				
Parameter	Symbol	Min	Max	Unit	Test conditions	Notes
Operating current (CAS latency = 2)	I _{CC1}	—	100	mA	Burst length = 1 t _{RC} = min	1, 2, 3
($\overline{\text{CAS}}$ latency = 3)	I _{CC1}	—	110	mA		
Standby current in power down	I _{CC2P}	—	6	mA	CKE = V _{IL} , t _{CK} = 12 ns	6
Standby current in power down (input signal stable)	I _{CC2PS}	—	4	mA	CKE = V _{IL} , t _{CK} = ∞	7
Standby current in non power down	I _{CC2N}	—	32	mA	CKE, $\overline{\text{CS}}$ = V _{IH} , t _{CK} = 12 ns	4
Standby current in non power down (input signal stable)	I _{CC2NS}	—	18	mA	CKE = V _{IH} , t _{CK} = ∞	9
Active standby current in power down	I _{CC3P}	—	8	mA	CKE = V _{IL} , t _{CK} = 12 ns	1, 2, 6
Active standby current in power down (input signal stable)	I _{CC3PS}	—	6	mA	CKE = V _{IL} , t _{CK} = ∞	2, 7
Active standby current in non power down	I _{CC3N}	—	40	mA	CKE, $\overline{\text{CS}}$ = V _{IH} , t _{CK} = 12 ns	1, 2, 4
Active standby current in non power down (input signal stable)	I _{CC3NS}	—	30	mA	CKE = V _{IH} , t _{CK} = ∞	2, 9
Burst operating current (CAS latency = 2)	I _{CC4}	—	110	mA	t _{CK} = min, BL = 4	1, 2, 5
($\overline{\text{CAS}}$ latency = 3)	I _{CC4}	—	135	mA		
Refresh current	I _{CC5}	—	190	mA	t _{RC} = min	3
Self refresh current	I _{CC6}	—	2	mA	V _{IH} ≥ V _{CC} − 0.2 V V _{IL} ≤ 0.2 V	8
Self refresh current (L-version)	I _{CC6}	—	0.8	mA		
Input leakage current	I _{LI}	−4	4	μA	0 ≤ Vin ≤ V _{CC}	
Output leakage current	I _{LO}	−6	6	μA	0 ≤ Vout ≤ V _{CC} DQ = disable	
Output high voltage	V _{OH}	2.4	—	V	I _{OH} = −4 mA	
Output low voltage	V _{OL}	—	0.4	V	I _{OL} = 4 mA	

- Notes:
- 1. I_{cc} depends on output load condition when the device is selected. I_{cc} (max) is specified at the output open condition.
 - 2. One bank operation.
 - 3. Input signals are changed once per one clock.
 - 4. Input signals are changed once per two clocks.
 - 5. Input signals are changed once per four clocks.
 - 6. After power down mode, CLK operating current.
 - 7. After power down mode, no CLK operating current.
 - 8. After self refresh mode set, self refresh current.
 - 9. Input signals are V_{IH} or V_{IL} fixed.

Capacitance ($T_a = 25^{\circ}C$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (CLK)	C_{i1}	5	8	pF	1, 2, 4
Input capacitance (Input except DQM)	C_{i2}	5	8	pF	1, 2, 4
Input capacitance (DQM)	C_{i3}	2.5	5	pF	1, 2, 4
Output capacitance (DQ)	C_o	3	5	pF	1, 2, 3, 4

- Notes:
- 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 - 2. Measurement condition: $f = 1\text{ MHz}$, 1.4 V bias, 200 mV swing.
 - 3. $DQMB = V_{IH}$ to disable Dout.
 - 4. This parameter is sampled and not 100% tested.

AC Characteristics

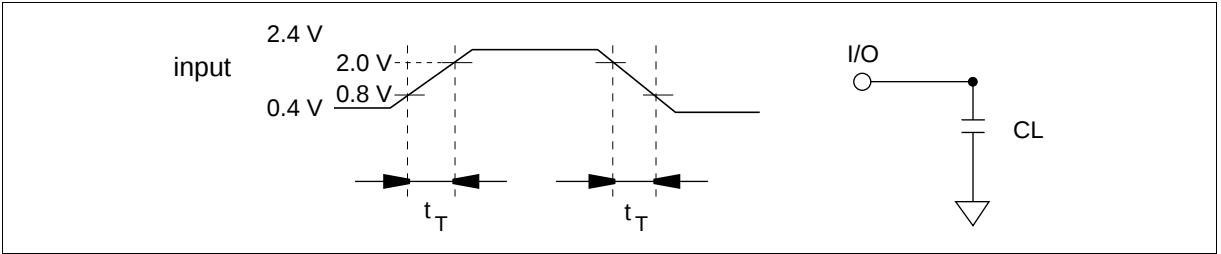
(Tcase = 0 to +70°C [Tj max = 110°C]), VCC = 3.3 V ± 0.3 V, VSS = 0 V)

HM5212325F						
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Parameter	HITACHI Symbol	PC/100 Symbol	Min	Max	Unit	Notes
System clock cycle time (CAS latency = 2)	t _{CK}	Tclk	15	—	ns	1
(CAS latency = 3)	t _{CK}	Tclk	10	—	ns	
CLK high pulse width	t _{CKH}	Tch	3	—	ns	1
CLK low pulse width	t _{CKL}	Tcl	3	—	ns	1
Access time from CLK (CAS latency = 2)	t _{AC}	Tac	—	8	ns	1, 2
(CAS latency = 3)	t _{AC}	Tac	—	6	ns	
Data-out hold time	t _{OH}	Toh	3	—	ns	1, 2
CLK to Data-out low impedance	t _{LZ}		2	—	ns	1, 2, 3
CLK to Data-out high impedance	t _{HZ}		—	6	ns	1, 4
Input setup time	t _{AS} , t _{CS} , t _{DS} , t _{CES}	Tsi	2	—	ns	1, 5, 6
CKE setup time for power down exit	t _{CESP}	Tpde	2	—	ns	1
Input hold time	t _{AH} , t _{CH} , t _{DH} , t _{CEH}	Thi	1	—	ns	1, 5
Ref/Active to Ref/Active command period	t _{RC}	Trc	70	—	ns	1
Active to Precharge command period	t _{RAS}	Tras	50	120000	ns	1
Active command to column command (same bank)	t _{RCD}	Trcd	20	—	ns	1
Precharge to active command period	t _{RP}	Trp	20	—	ns	1
Write recovery or data-in to precharge lead time	t _{DPL}	Tdpl	10	—	ns	1
Active (a) to Active (b) command period	t _{RRD}	Trrd	20	—	ns	1
Transition time (rise and fall)	t _T		1	5	ns	
Refresh period	t _{REF}		—	64	ms	

- Notes:
- 1. AC measurement assumes $t_T = 1\text{ ns}$. Reference level for timing of input signals is 1.5 V.
 - 2. Access time is measured at 1.5 V. Load condition is $CL = 50\text{ pF}$.
 - 3. $t_{LZ}(\text{min})$ defines the time at which the outputs achieves the low impedance state.
 - 4. $t_{HZ}(\text{max})$ defines the time at which the outputs achieves the high impedance state.
 - 5. t_{CES} define CKE setup time to CLK rising edge except power down exit command.
 - 6. t_{AS}/t_{AH} : Address, t_{CS}/t_{CH} : $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{DQM}$.
 t_{DS}/t_{DH} : Data-in, t_{CES}/t_{CEH} : CKE

Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures

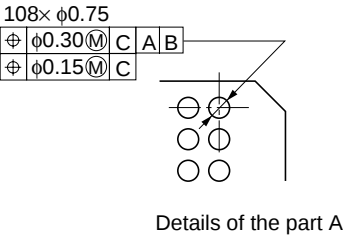
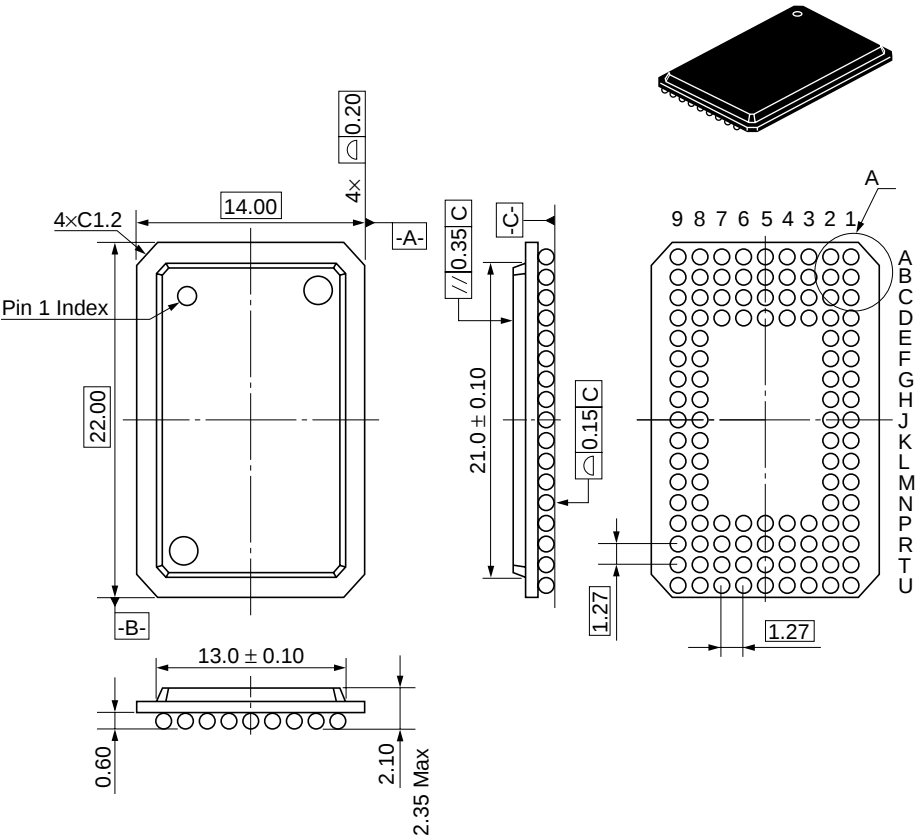


Package Dimensions

HM5212325FBP Series (BP-108)

Preliminary

Unit: mm



Hitachi Code	BP-108
JEDEC	—
EIAJ	—
Weight (reference value)	1.2 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	May. 12, 1999	Initial issue	S. Hatano	S. Hatano
1.0	Oct. 18, 1999	Programmable $\overline{\text{CAS}}$ latency: 3 to 2/3 Ordering information Addition of note Pin description Addition of note 1 DC Characteristics I_{CC1} max (CL = 3): 150 mA to 110 mA I_{CC4} max (CL = 3): 180 mA to 135 mA I_{CC5} max: 230 mA to 190 mA Addition of I_{CC1} max (CL = 2): 100 mA Addition of I_{CC4} max (CL = 2): 110 mA Capacitance C_{I2} max: 10 pF to 8 pF C_{I3} max: 6 pF to 5 pF C_{O} min: 4 pF to 3 pF C_{O} max: 6.5 pF to 5 pF AC Characteristics Addition of t_{CK} min (CL = 2): 15 ns Addition of t_{AC} max (CL = 2): 8 ns Package dimension Change tolerance of height		