
HM51W16405 Series HM51W17405 Series

16 M EDO DRAM (4-Mword $\times$ 4-bit)
4 k Refresh/2 k Refresh

ELPIDA

E0152H10 (Ver. 1.0)
(Previous ADE-203-647D (Z))
Jul. 6, 2001 (K)

Description

The HM51W16405 Series, HM51W17405 Series are CMOS dynamic RAMs organized 4,194,304-word $\times$ 4-bit. They employ the most advanced CMOS technology for high performance and low power. The HM51W16405 Series, HM51W17405 Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have package variations of standard 300-mil 26-pin plastic SOJ and 300-mil 26-pin plastic TSOP.

Features

- Single 3.3 V (± 0.3 V)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation
 - Active mode : 324 mW /288 mW /252 mW (max) (HM51W16405 Series)
: 360mW/324 mW/288 mW (max) (HM51W17405 Series)
 - Standby mode : 7.2 mW (max)
: 0.36 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
 - 4096 refresh cycles : 64 ms (HM51W16405 Series)
: 128 ms (L-version)
 - 2048 refresh cycles : 32 ms (HM51W17405 Series)
: 128 ms (L-version)
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)

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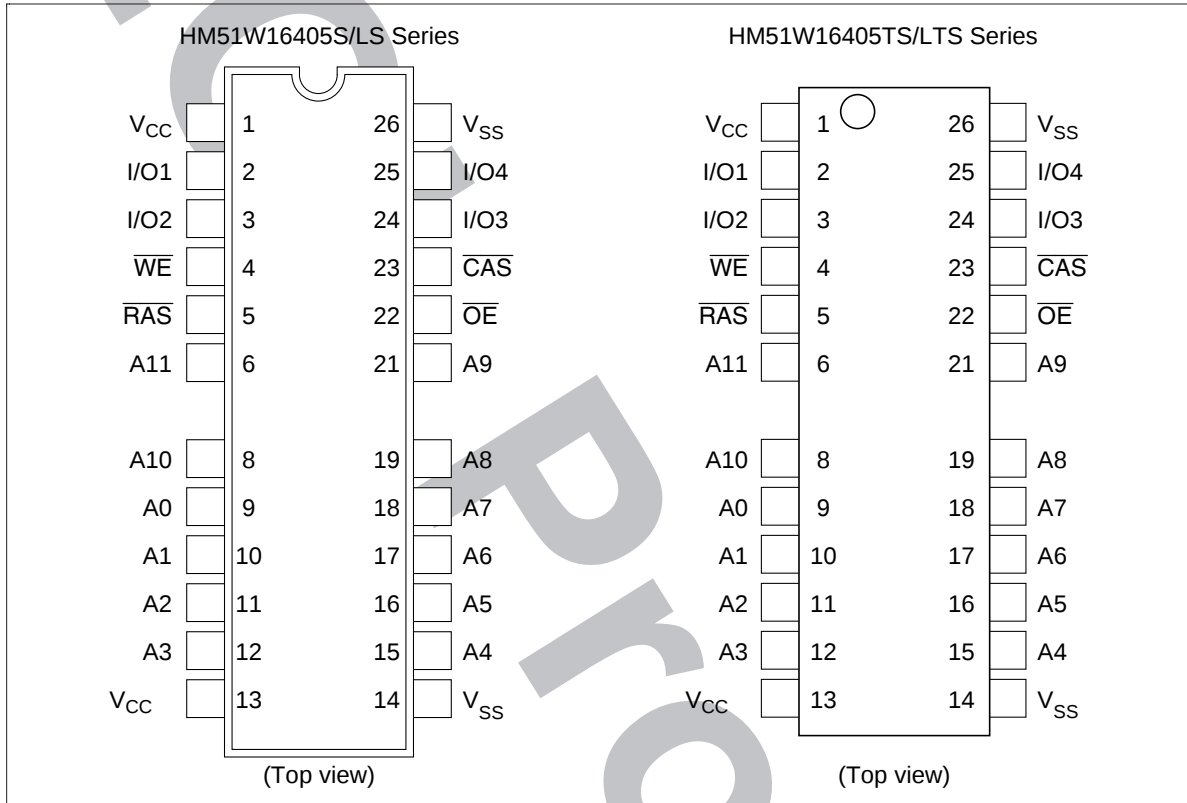
- Battery backup operation (L-version)
- Test function
 - 16-bit parallel test mode

Ordering Information

Type No.	Access time	Package
HM51W16405S-5	50 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM51W16405S-6	60 ns	
HM51W16405S-7	70 ns	
HM51W16405LS-5	50 ns	
HM51W16405LS-6	60 ns	
HM51W16405LS-7	70 ns	
HM51W17405S-5	50 ns	
HM51W17405S-6	60 ns	
HM51W17405S-7	70 ns	
HM51W17405LS-5	50 ns	
HM51W17405LS-6	60 ns	
HM51W17405LS-7	70 ns	
HM51W16405TS-5	50 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM51W16405TS-6	60 ns	
HM51W16405TS-7	70 ns	
HM51W16405LTS-5	50 ns	
HM51W16405LTS-6	60 ns	
HM51W16405LTS-7	70 ns	
HM51W17405TS-5	50 ns	
HM51W17405TS-6	60 ns	
HM51W17405TS-7	70 ns	
HM51W17405LTS-5	50 ns	
HM51W17405LTS-6	60 ns	
HM51W17405LTS-7	70 ns	

HM51W16405 Series, HM51W17405 Series

Pin Arrangement

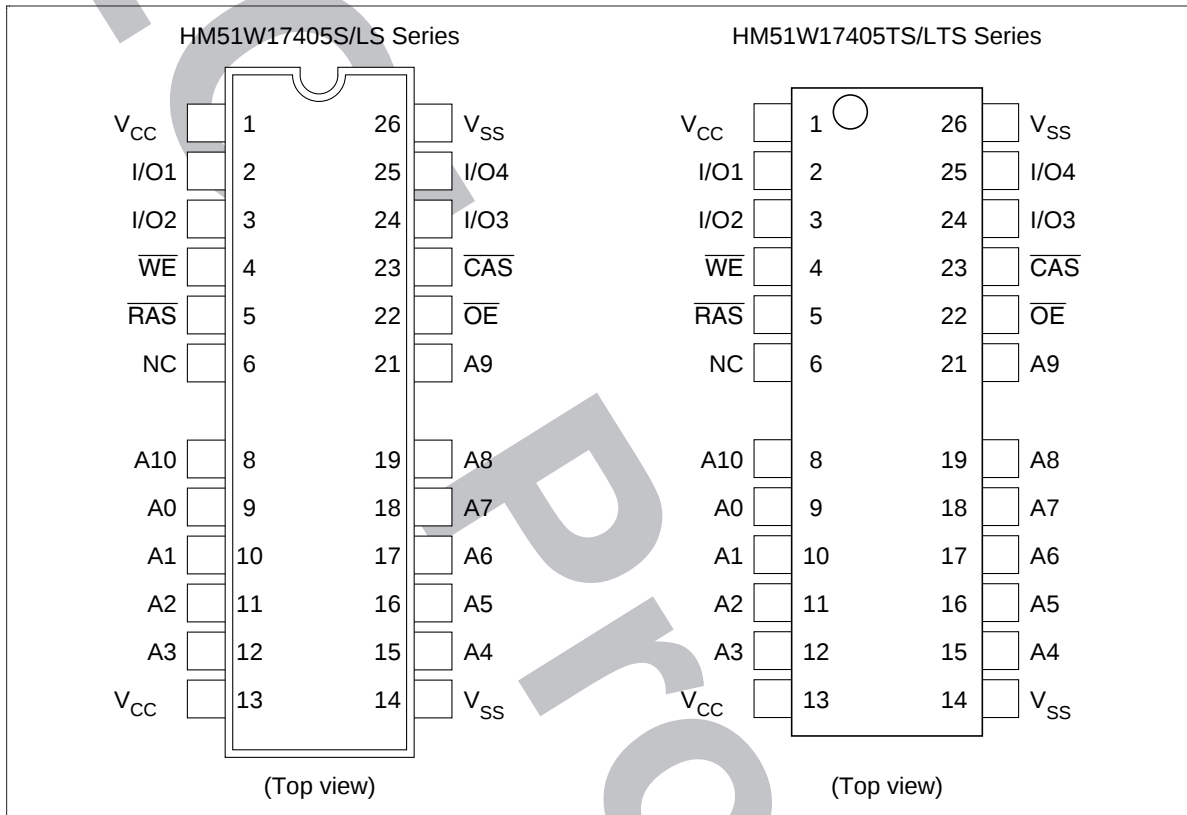


Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A9
I/O1 to I/O4	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

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Pin Arrangement

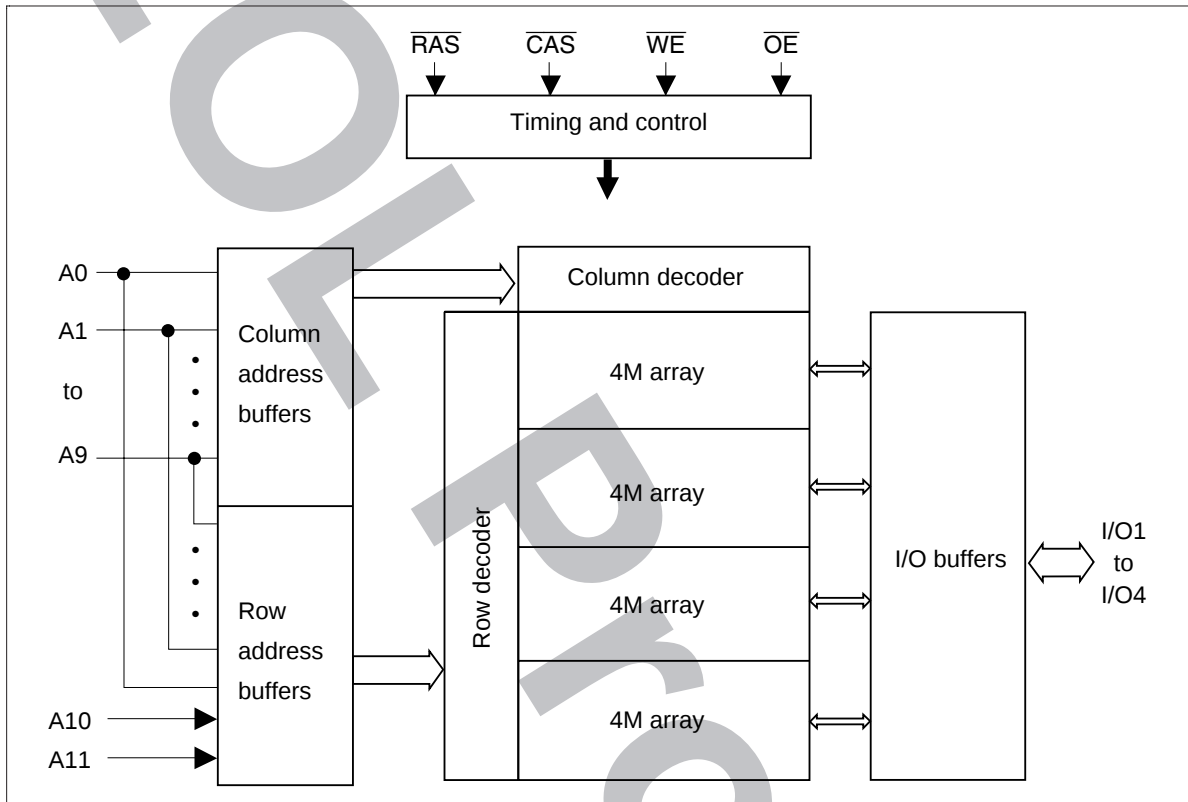


Pin Description

Pin name	Function
A0 to A10	Address input — Row/Refresh address A0 to A10 — Column address A0 to A10
I/O1 to I/O4	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

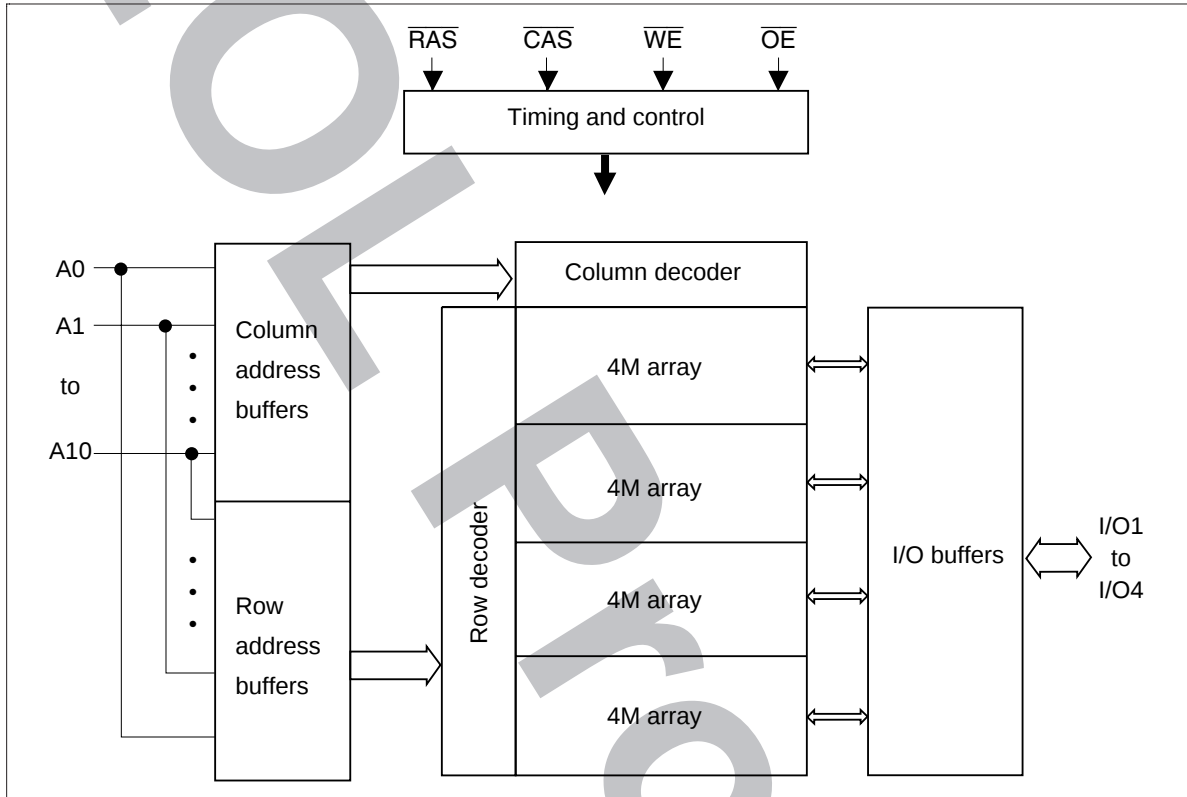
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Block Diagram(HM51W16405 Series)



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Block Diagram(HM51W17405 Series)



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to $V_{CC} + 0.5$ ($\leq +4.6$ V (max))	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to $+4.6$	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to $+70$	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to $+125$	$^{\circ}\text{C}$

Recommended DC Operating Conditions ($T_a = 0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

HM51W16405 Series, HM51W17405 Series

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W16405 Series)

		HM51W16405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I _{CC1}	—	90	—	80	—	70	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	100	—	100	—	100	μA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z
RAS-only refresh current ^{*2}	I _{CC3}	—	90	—	80	—	70	mA	t _{RC} = min
Standby current ^{*1}	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	90	—	80	—	70	mA	t _{RC} = min
EDO page mode current ^{*1, *3}	I _{CC7}	—	80	—	70	—	65	mA	t _{HPC} = min
Battery backup current	I _{CC10}	—	300	—	300	—	300	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	200	—	200	—	200	μA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL}.

3. Address can be changed once or less while CAS = V_{IH}.

HM51W16405 Series, HM51W17405 Series

DC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$) (HM51W17405 Series)

		HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I _{CC1}	—	100	—	90	—	80	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	100	—	100	—	100	μA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current ^{*2}	I _{CC3}	—	100	—	90	—	80	mA	t _{RC} = min
Standby current ^{*1}	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	100	—	90	—	80	mA	t _{RC} = min
EDO page mode current ^{*1, *3}	I _{CC7}	—	90	—	80	—	75	mA	t _{HPC} = min
Battery backup current	I _{CC10}	—	300	—	300	—	300	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 62.5 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	200	—	200	—	200	μA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

HM51W16405 Series, HM51W17405 Series

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

HM51W16405 Series, HM51W17405 Series

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$) *¹, *², *¹⁸

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL} = 0\text{ V}$, $V_{IH} = 3\text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	84	—	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	8	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	8	10000	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	8	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	12	37	14	45	14	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	10	25	12	30	12	35	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	10	—	13	—	13	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{OED}	13	—	15	—	18	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	7

HM51W16405 Series, HM51W17405 Series

Read Cycle

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9, 20
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17, 20
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17, 20
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	—	18	ns	9, 20
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	13	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	22
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	13	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	13	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

HM51W16405 Series, HM51W17405 Series

Write Cycle

Parameter	Symbol	HM51W16405/HM51W17405						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t _{WCH}	8	—	10	—	13	—	ns	
Write command pulse width	t _{WP}	8	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t _{RWL}	8	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t _{CWL}	8	—	10	—	13	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t _{DH}	8	—	10	—	13	—	ns	15

Read-Modify-Write Cycle

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	111	—	135	—	161	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	67	—	79	—	92	—	ns	14
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	30	—	34	—	40	—	ns	14
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	42	—	49	—	57	—	ns	14
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	5	—	ns	
CAS hold time (CBR refresh cycle)	t _{CHR}	8	—	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t _{WRP}	0	—	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t _{WRH}	8	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	5	—	5	—	5	—	ns	

HM51W16405 Series, HM51W17405 Series

EDO Page Mode Cycle

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	20	—	25	—	30	—	ns	21
EDO page mode RAS pulse width	t _{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from CAS precharge	t _{CPA}	—	30	—	35	—	40	ns	9, 17, 20
RAS hold time from CAS precharge	t _{CPRH}	30	—	35	—	40	—	ns	
Output data hold time from CAS low	t _{DOH}	3	—	3	—	3	—	ns	9, 17
CAS hold time referred OE	t _{COL}	8	—	10	—	13	—	ns	
CAS to OE setup time	t _{COP}	5	—	5	—	5	—	ns	
Read command hold time from CAS precharge	t _{RCHC}	30	—	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read- modify-write cycle time	t _{HPRWC}	57	—	68	—	79	—	ns	
WE delay time from $\overline{\text{CAS}}$ precharge	t _{CPW}	45	—	54	—	62	—	ns	14

Test Mode Cycle *19

		HM51W16405/HM51W17405							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WTS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WTH}	8	—	10	—	10	—	ns	

Refresh (HM51W16405 Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

HM51W16405 Series, HM51W17405 Series

Refresh (HM51W17405 Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	32	ms	2048 cycles
Refresh period (L-version)	t_{REF}	128	ms	2048 cycles

Self Refresh Mode (L-version)

		HM51W16405L/HM51W17405L							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
RAS pulse width (self refresh)	t_{RASS}	100	—	100	—	100	—	μ s	
RAS precharge time (self refresh)	t_{RPS}	90	—	110	—	130	—	ns	
CAS hold time (self refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	

Notes: 1. AC measurements assume $t_r = 2$ ns.

- An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
- Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
- Either t_{OED} or t_{CDD} must be satisfied.
- Either t_{DZO} or t_{DZC} must be satisfied.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
- Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
- Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
- Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
- t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

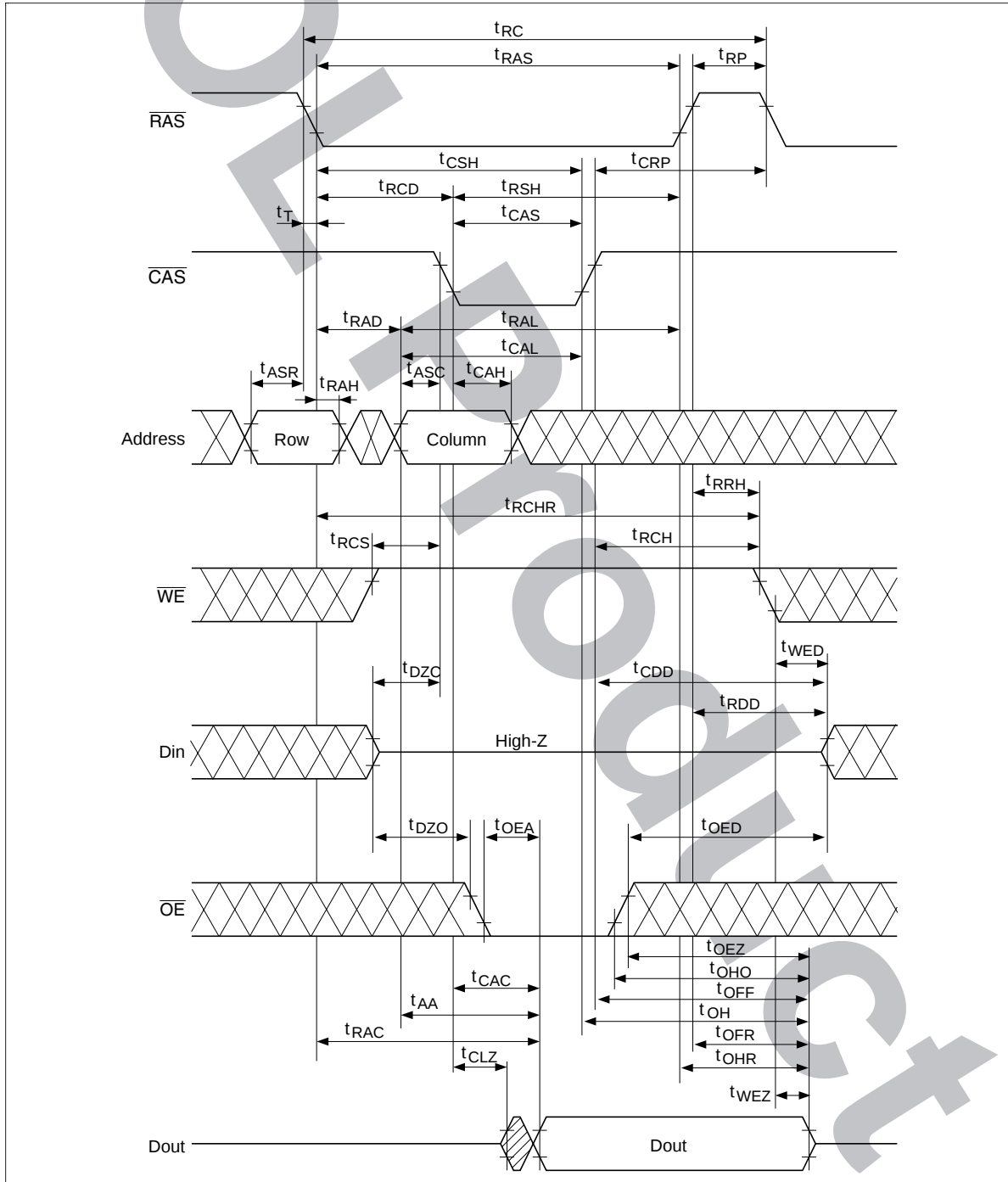
HM51W16405 Series, HM51W17405 Series

15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to device.
19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M $\times$ 4 are don't care during test mode. Test mode is set by performing a $\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.
If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.
Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.
To get out of test mode and enter a normal operation mode, perform either a regular $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or $\overline{\text{RAS}}$ -only refresh cycle.
20. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
21. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2 t_r$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
22. Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
23. Please do not use t_{RASS} timing, $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} > 100 \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .
24. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 2048 cycles (4096 cycles: HM51W16405 Series, 2048 cycles: HM51W17405 Series) of distributed CBR refresh with 15.6 μs interval should be executed within 64 or 32 ms (64 ms: HM51W16405 Series, 32 ms: HM51W17405 Series) immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H: V_{IH} (min) $\leq V_{\text{IN}} \leq V_{\text{IH}}$ (max), L: V_{IL} (min) $\leq V_{\text{IN}} \leq V_{\text{IL}}$ (max))
/////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

HM51W16405 Series, HM51W17405 Series

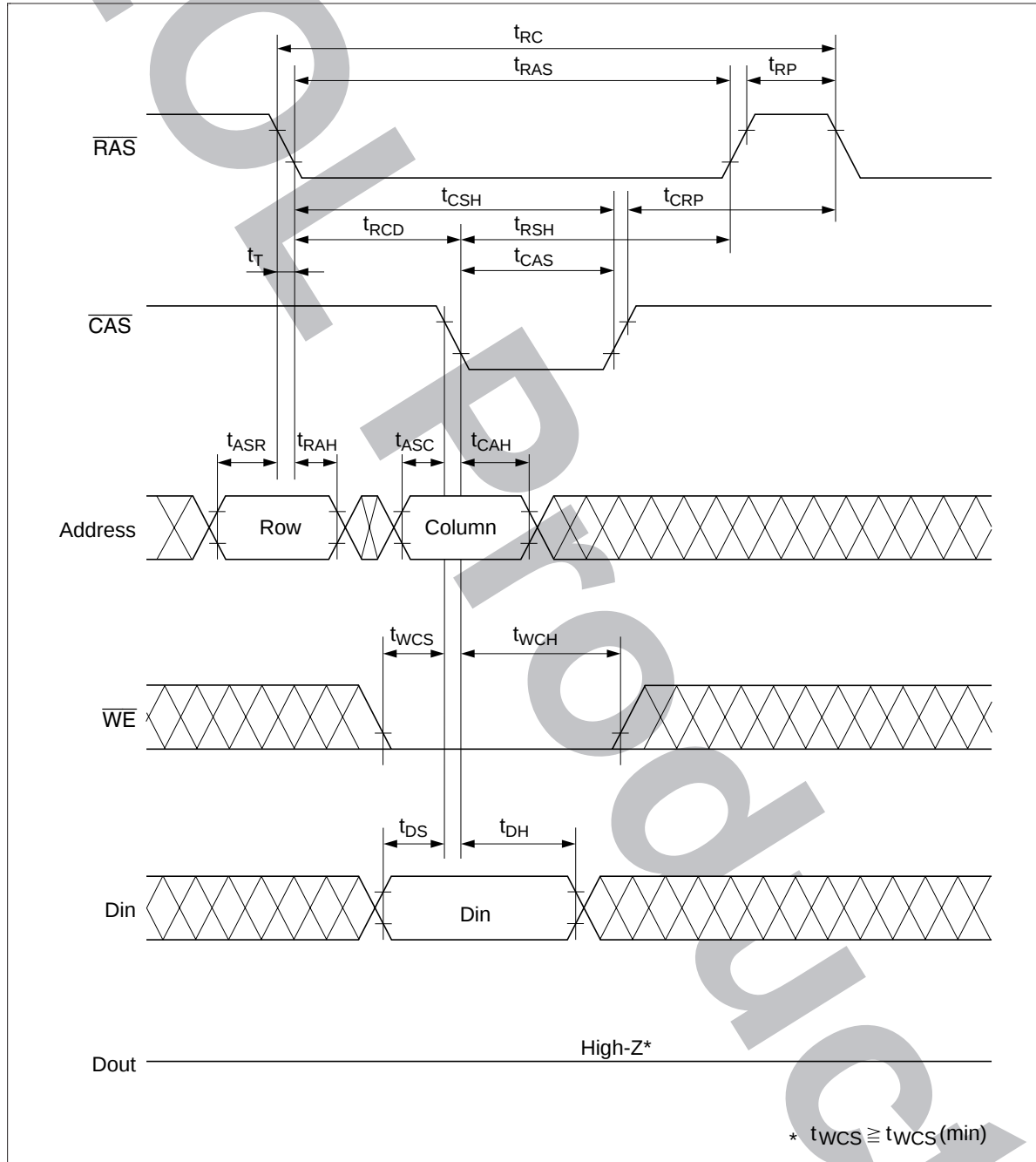
Timing Waveforms*27

Read Cycle



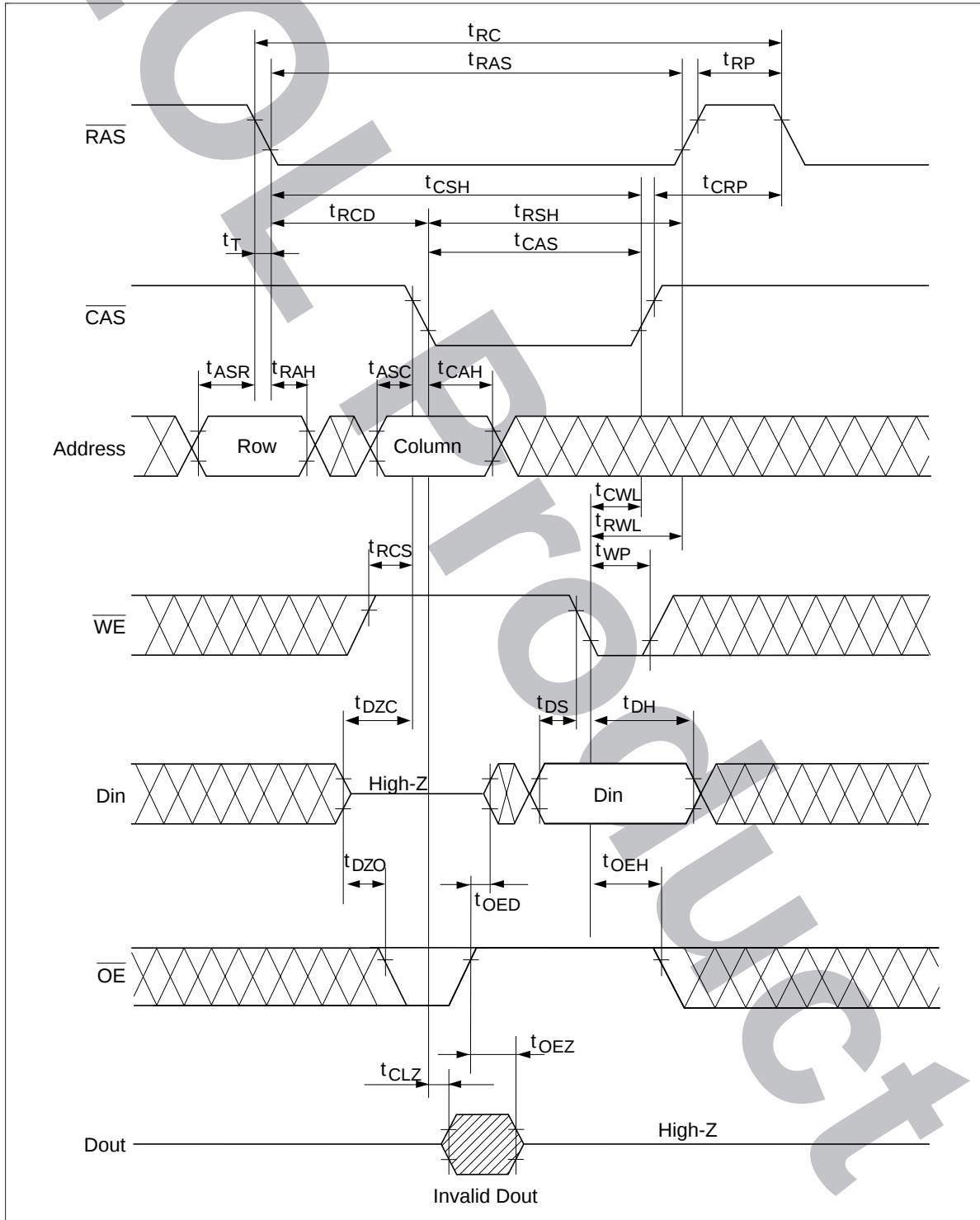
HM51W16405 Series, HM51W17405 Series

Early Write Cycle



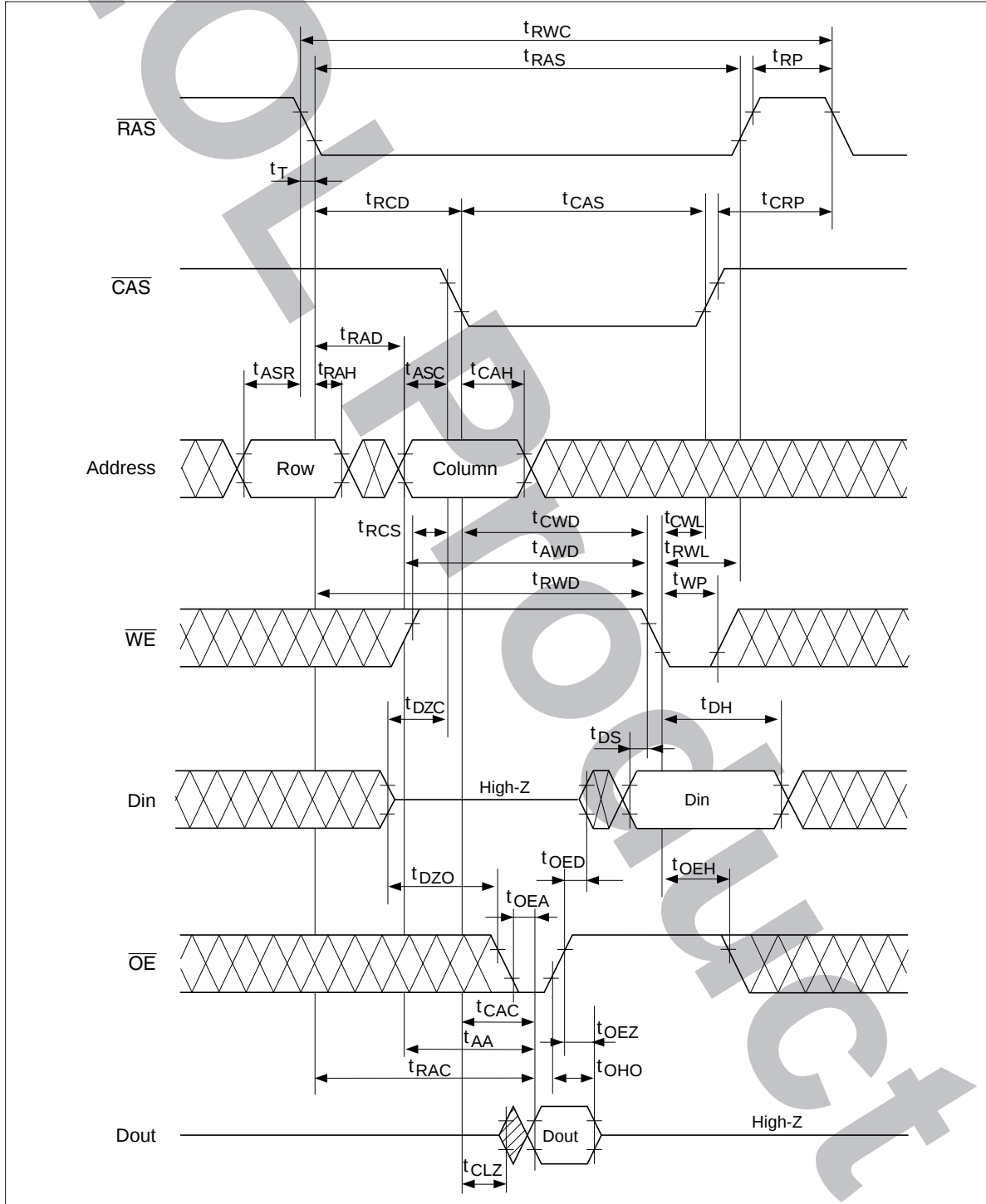
HM51W16405 Series, HM51W17405 Series

Delayed Write Cycle*¹⁸



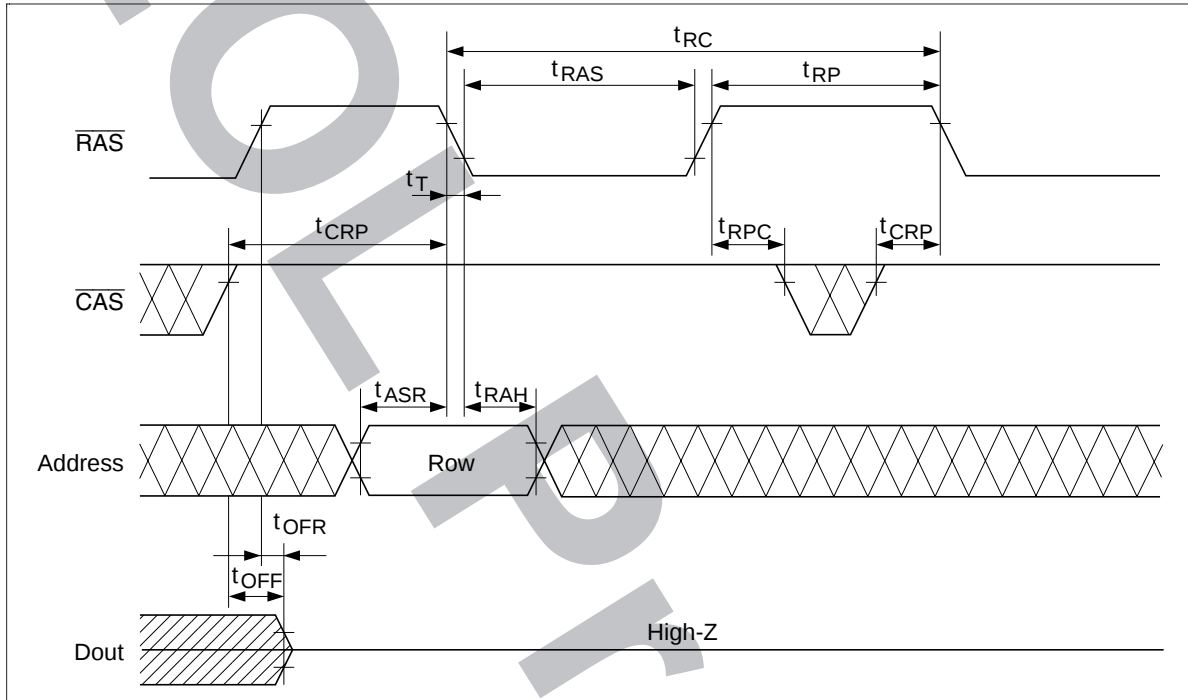
HM51W16405 Series, HM51W17405 Series

Read-Modify-Write Cycle *18



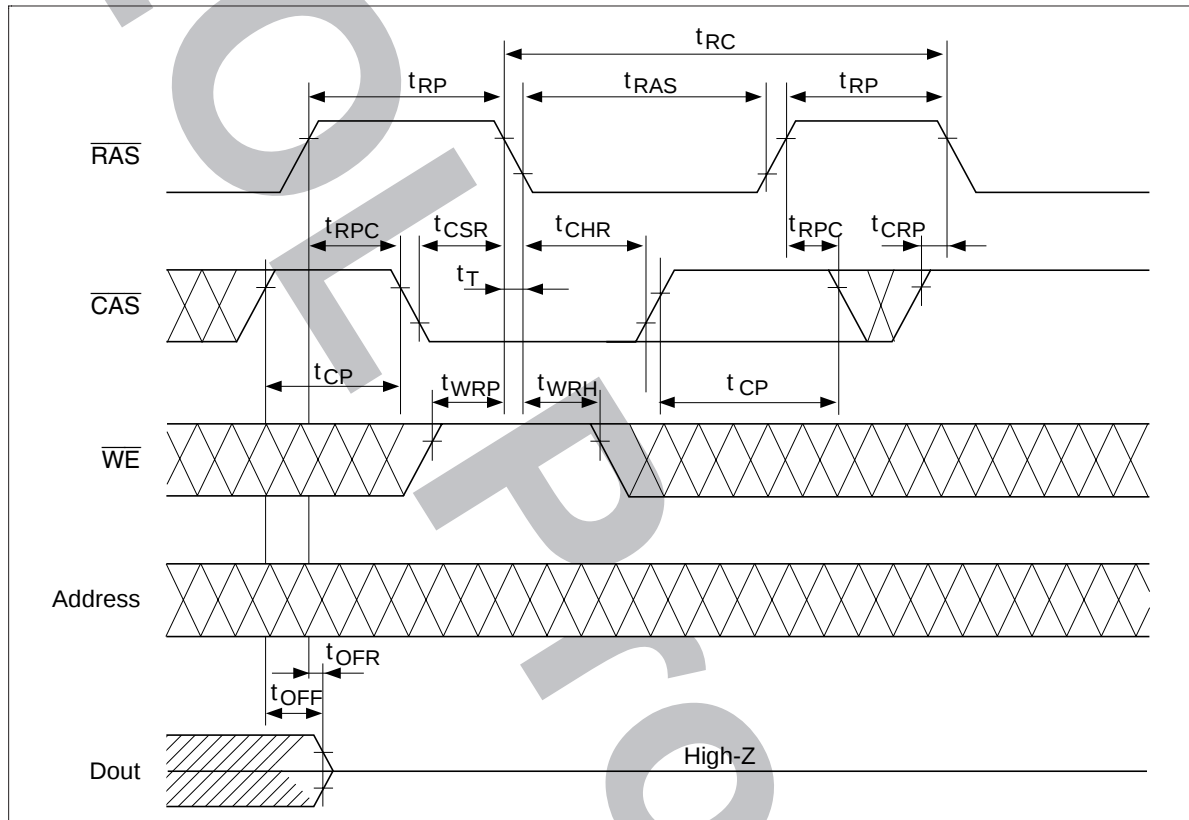
HM51W16405 Series, HM51W17405 Series

$\overline{\text{RAS}}$ -Only Refresh Cycle



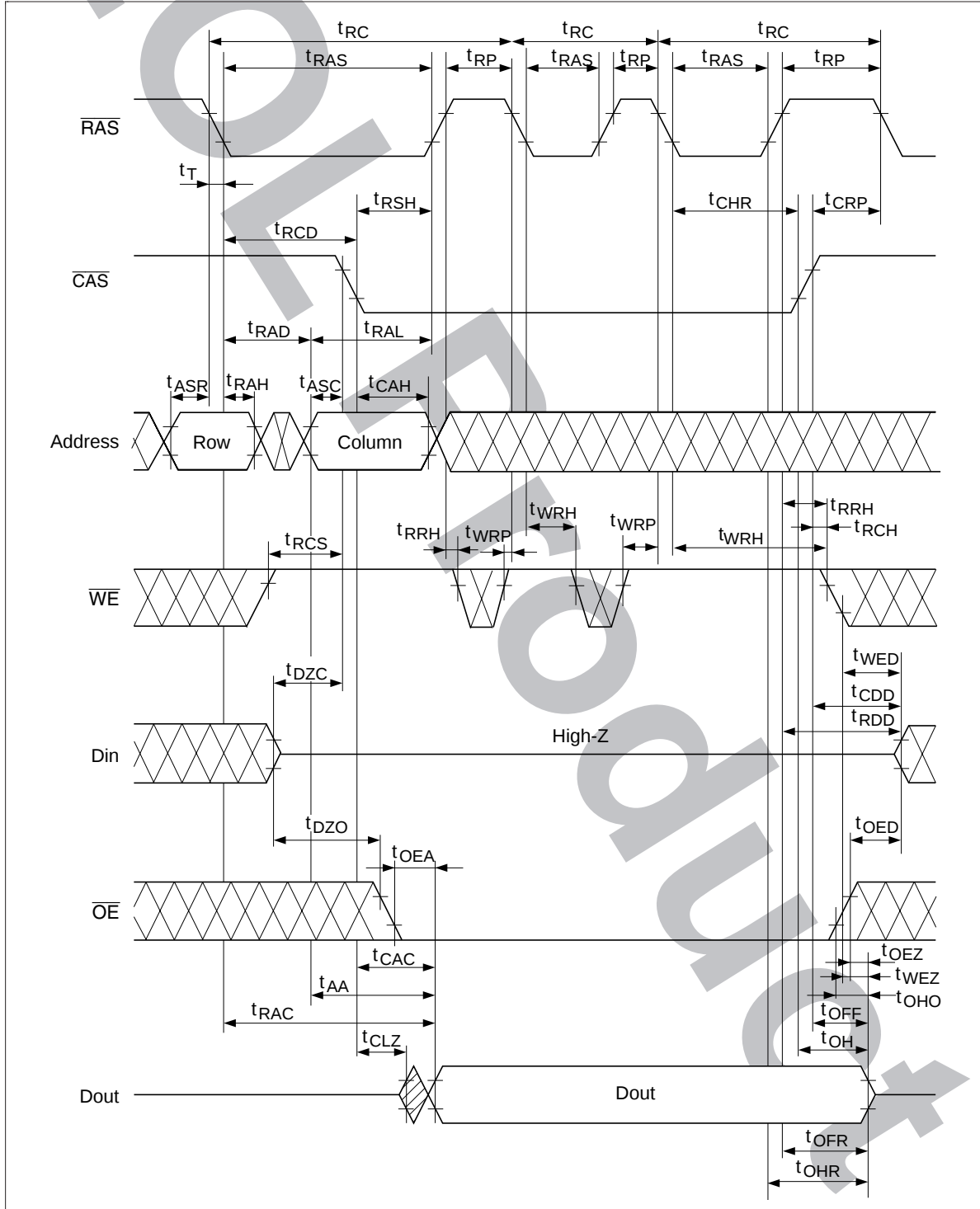
HM51W16405 Series, HM51W17405 Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

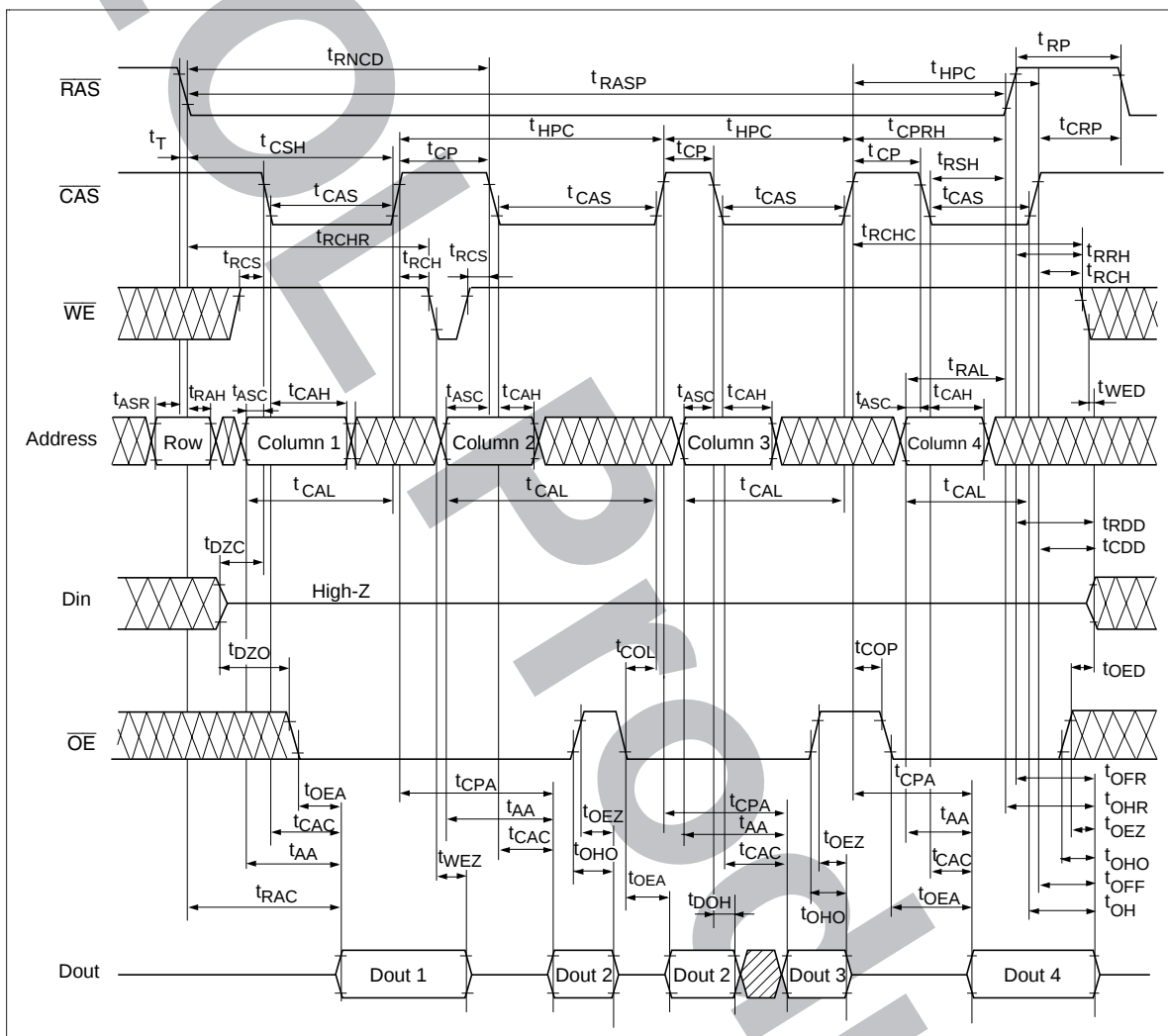


HM51W16405 Series, HM51W17405 Series

Hidden Refresh Cycle

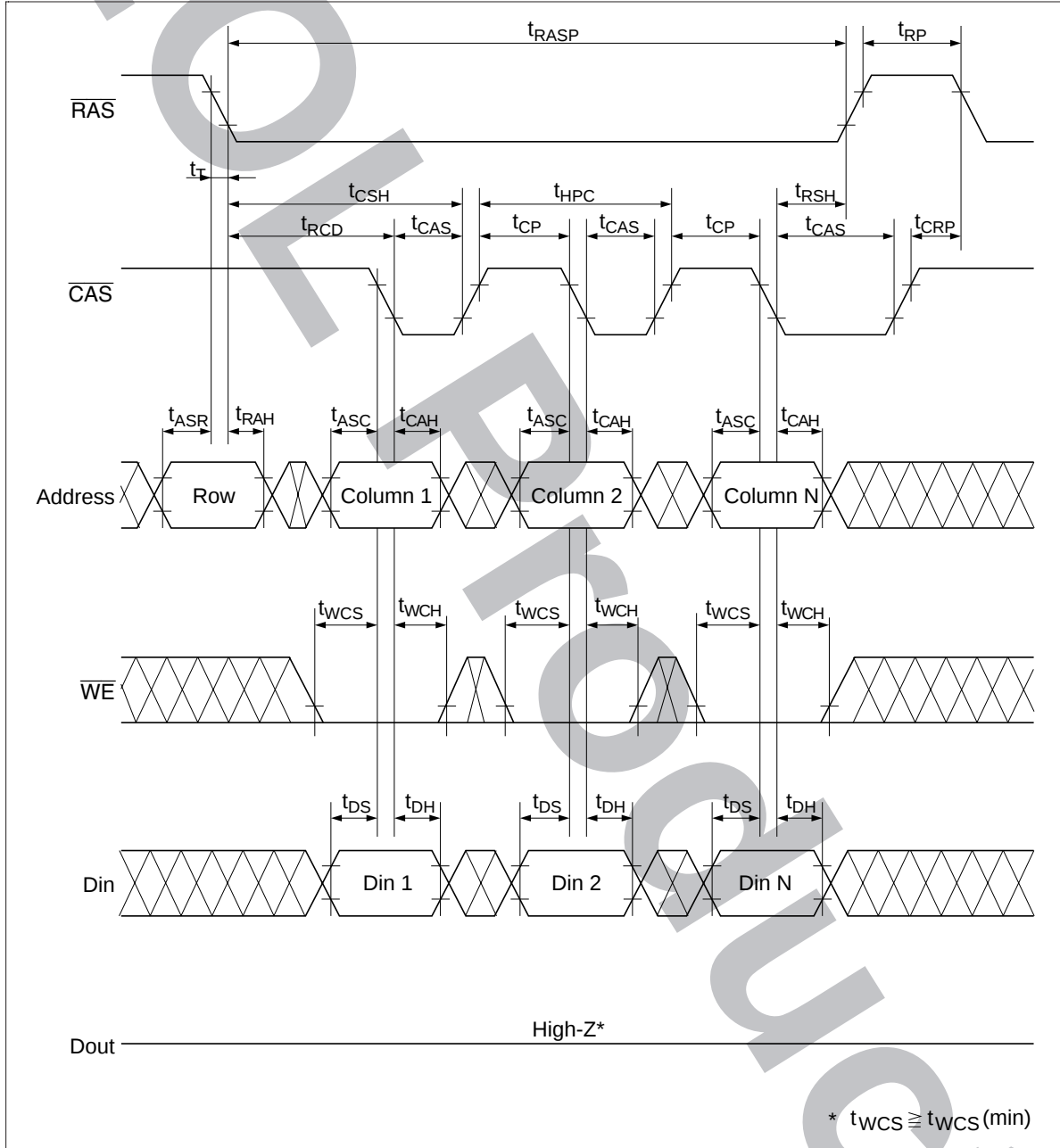


EDO Page Mode Read Cycle



HM51W16405 Series, HM51W17405 Series

EDO Page Mode Early Write Cycle



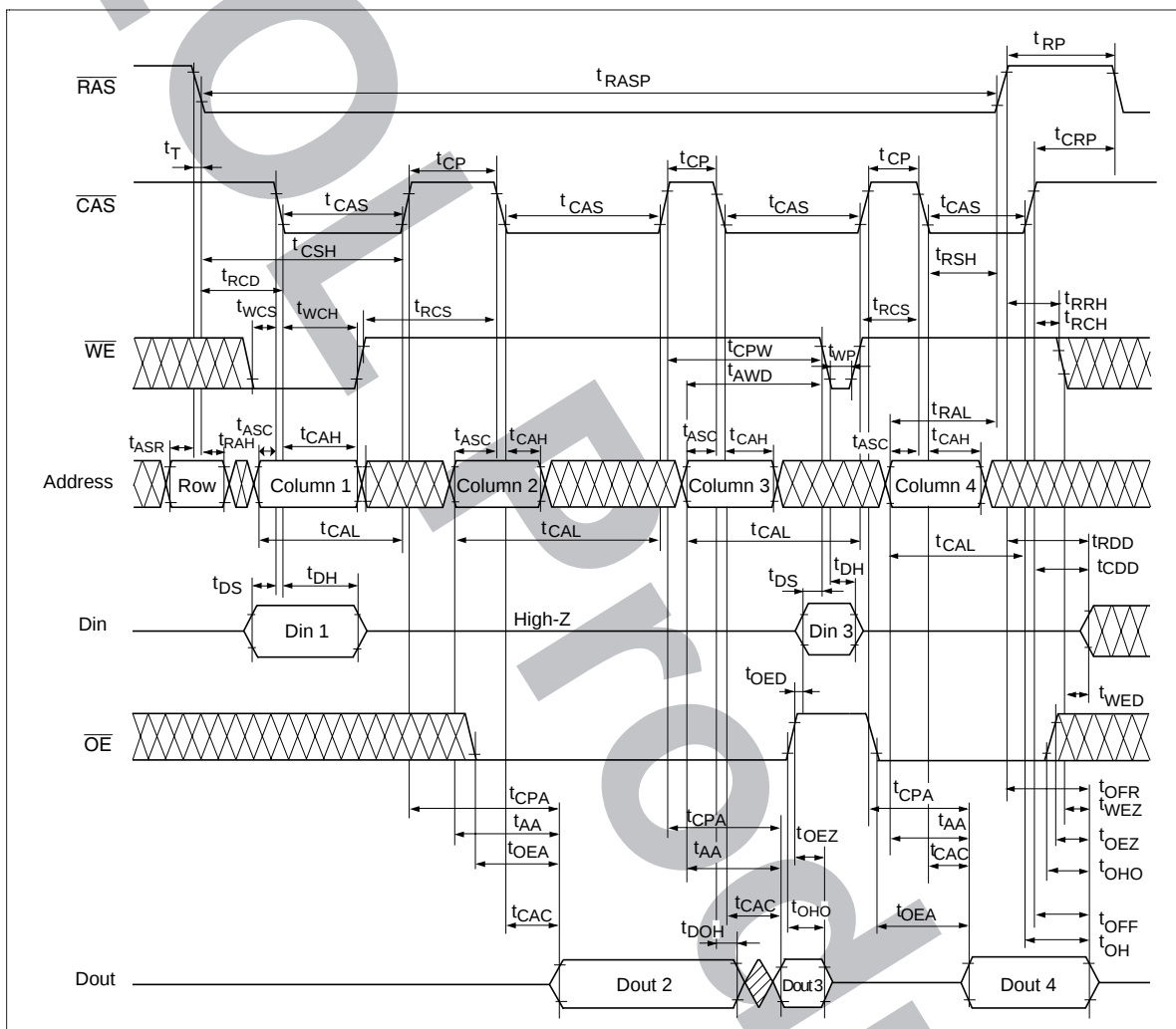
EDO Page Mode Delayed Write Cycle ^{*18}



EDO Page Mode Read-Modify-Write Cycle *¹⁸

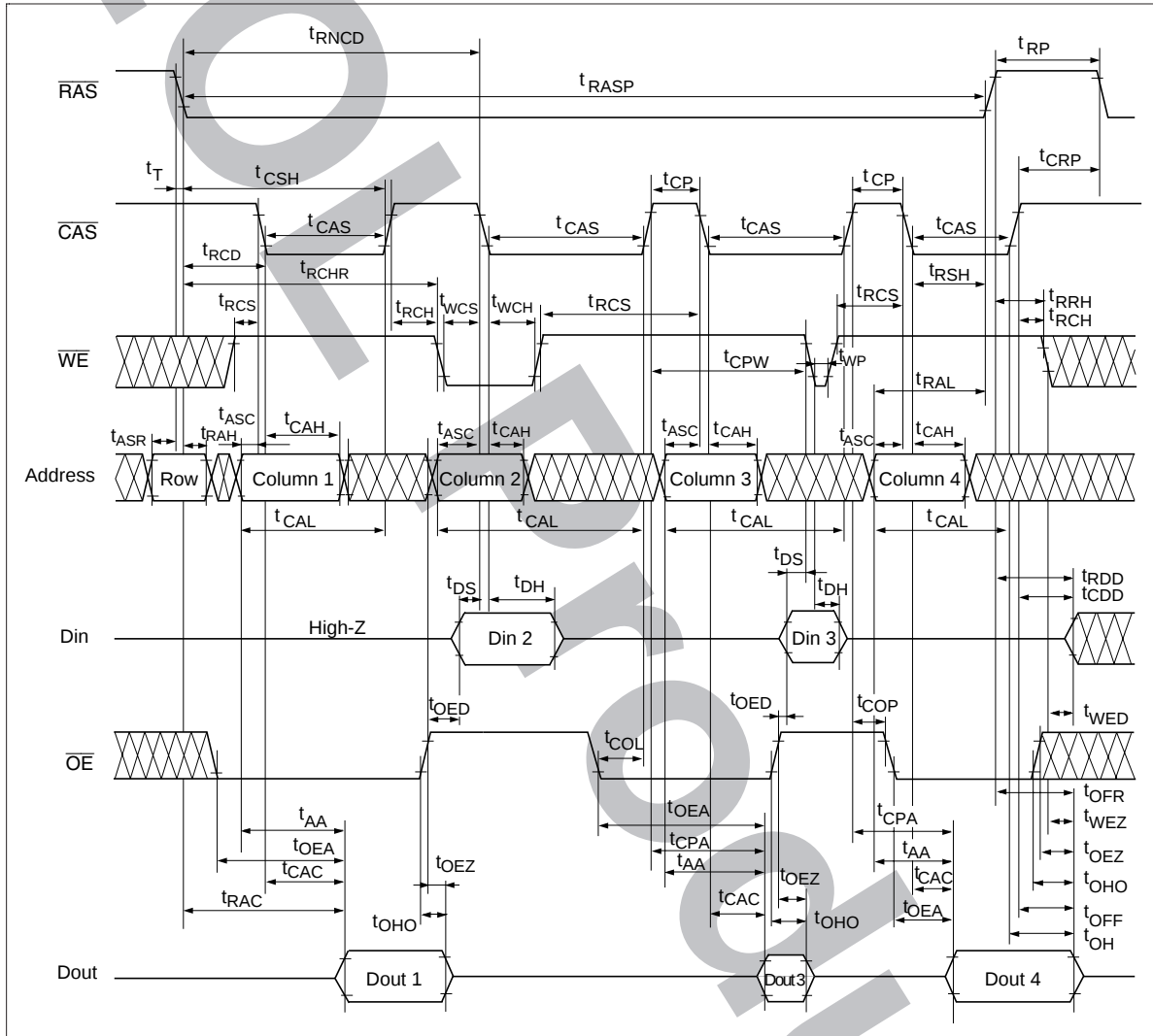


EDO Page Mode Mix Cycle (1)



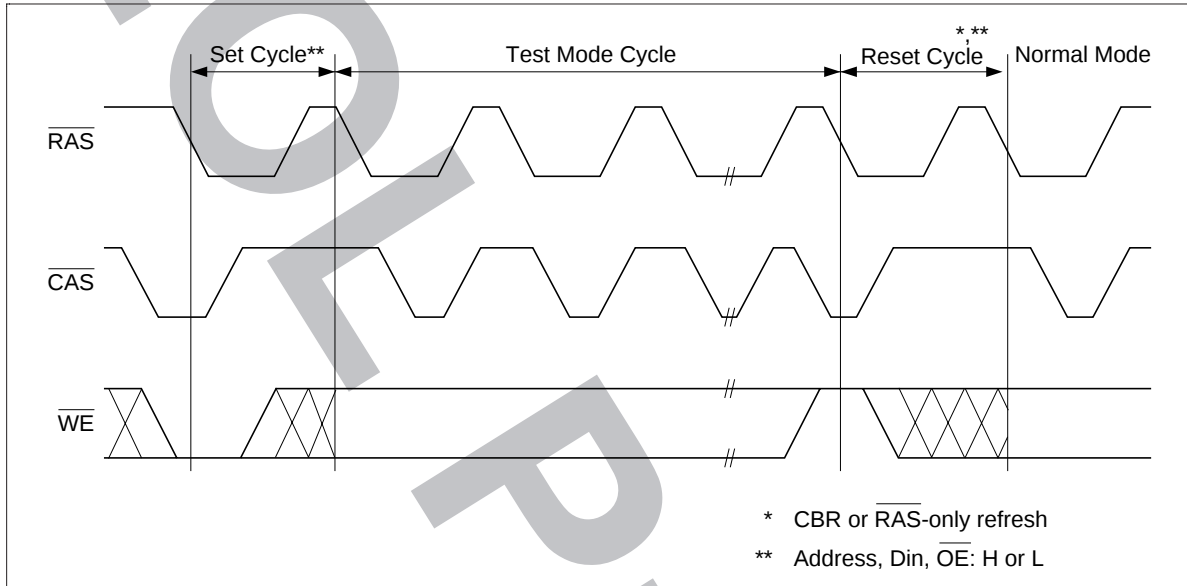
HM51W16405 Series, HM51W17405 Series

EDO Page Mode Mix Cycle (2)



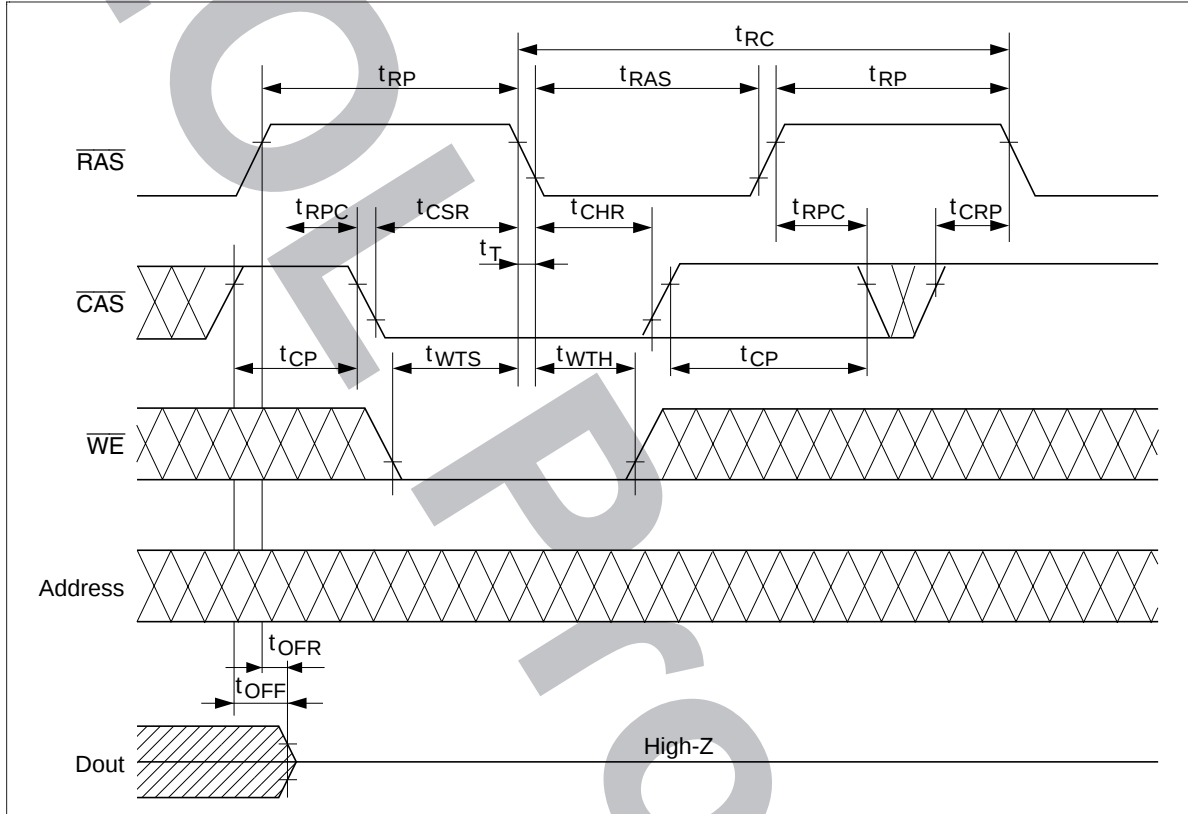
HM51W16405 Series, HM51W17405 Series

Test Mode Cycle ^{*19}



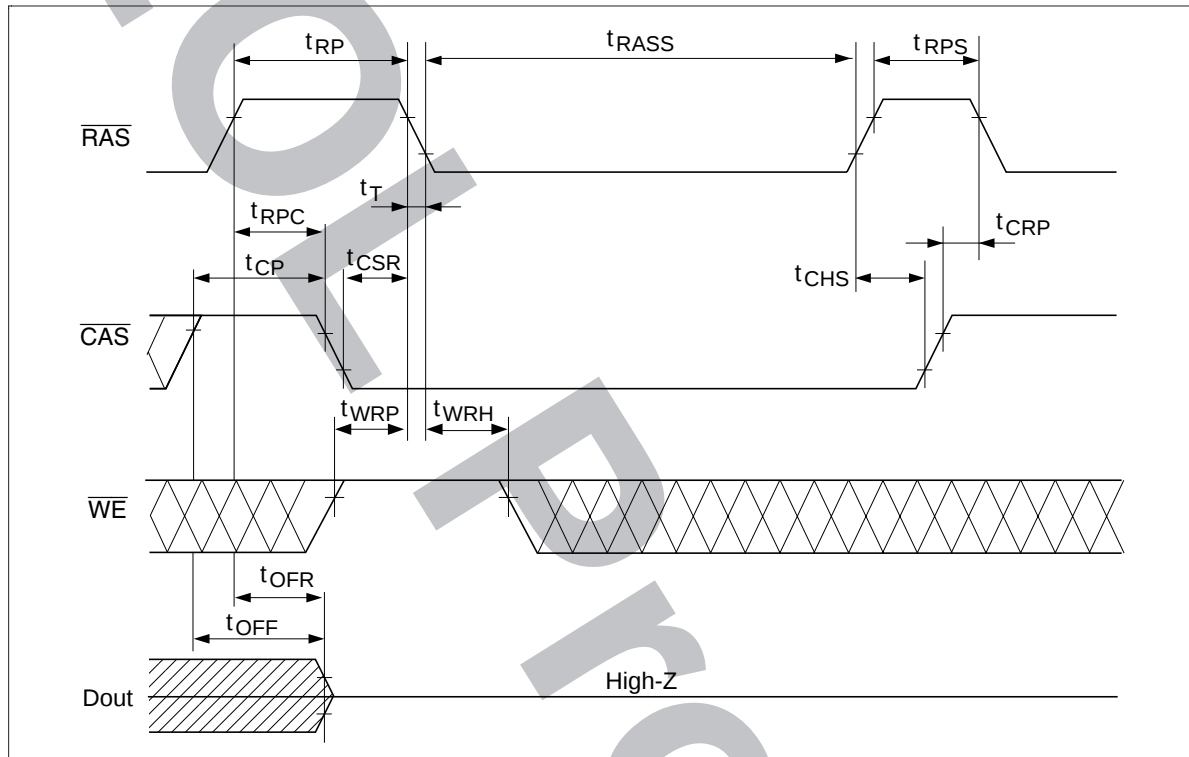
HM51W16405 Series, HM51W17405 Series

Test Mode Set Cycle



HM51W16405 Series, HM51W17405 Series

Self Refresh Cycle (L-version)*^{23, *24, *25, *26}



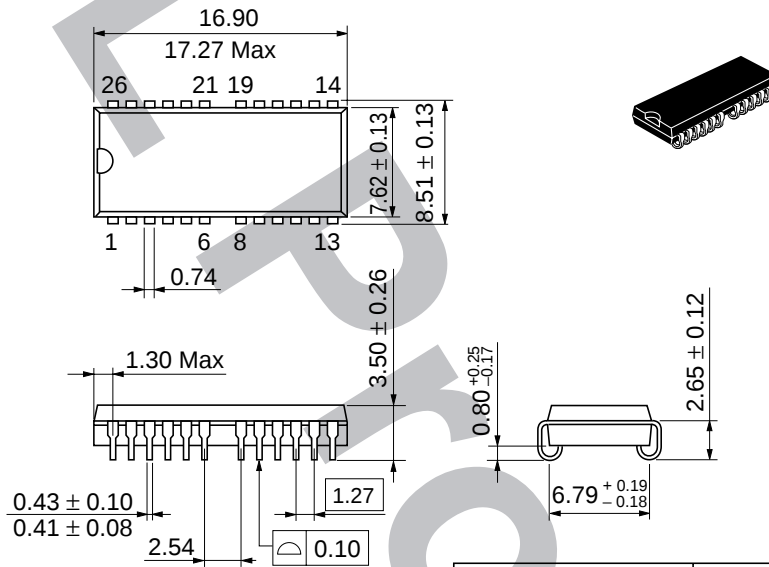
HM51W16405 Series, HM51W17405 Series

Package Dimensions

HM51W16405S/LS Series

HM51W17405S/LS Series (CP-26/24DB)

Unit: mm



Dimension including the plating thickness
Base material dimension

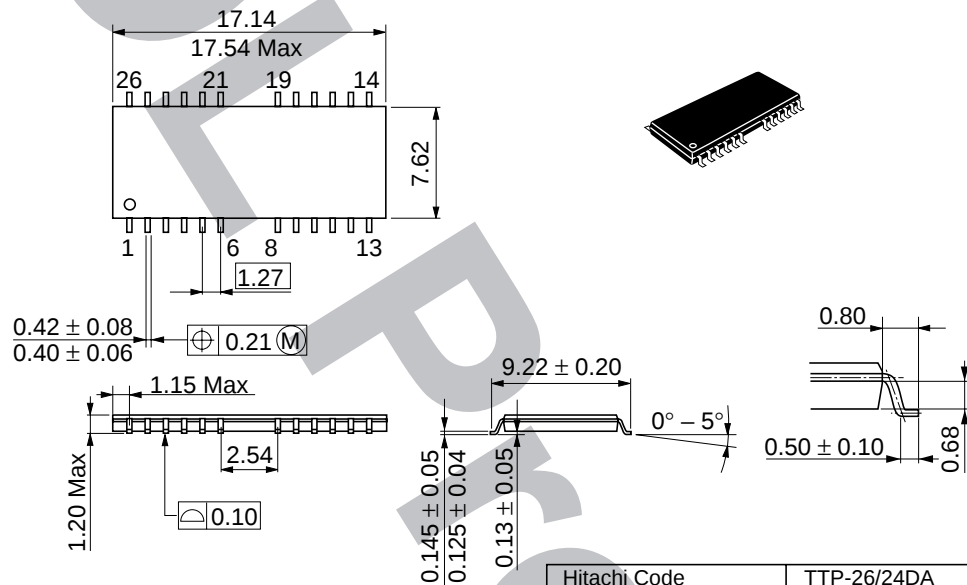
Hitachi Code	CP-26/24DB
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.8 g

HM51W16405 Series, HM51W17405 Series

HM51W16405TS/LTS Series

HM51W17405TS/LTS Series (TTP-26/24DA)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-26/24DA
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.30 g

HM51W16405 Series, HM51W17405 Series

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