

P-Channel Enhancement Mode Power MOSFET

Description

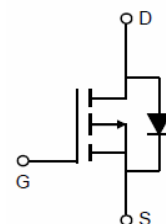
The HM45P02Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

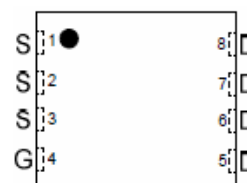
- $V_{DS} = -20V, I_D = -45A$
 $R_{DS(ON)} < 7m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} < 9m\Omega @ V_{GS} = -2.5V$
 $R_{DS(ON)} < 12m\Omega @ V_{GS} = -1.8V$
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Load switch
- Battery protection



Schematic diagram



Pin Assignment



DFN 3.3x3.3 EP top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM45P02Q	HM45P02Q	DFN 3.3x3.3 EP	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	-45	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	-35	A
Pulsed Drain Current	I_{DM}	-200	A
Maximum Power Dissipation	P_D	80	W
Derating factor		0.64	W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.6	$^\circ C/W$
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.6	-1.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-20A	-	5.8	7	mΩ
		V _{GS} =-2.5V, I _D =-20A	-	7.2	9	
		V _{GS} =-1.8V, I _D =-20A		9	12	
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-20A	80	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, F=1.0MHz	-	3500	-	PF
Output Capacitance	C _{oss}		-	577	-	PF
Reverse Transfer Capacitance	C _{rss}		-	445	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-10V, R _{GEN} =3Ω V _{GS} =-4.5V, R _L =0.5Ω	-	18	-	nS
Turn-on Rise Time	t _r		-	42	-	nS
Turn-Off Delay Time	t _{d(off)}		-	85	-	nS
Turn-Off Fall Time	t _f		-	23	-	nS
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-20A, V _{GS} =-4.5V	-	55	-	nC
Gate-Source Charge	Q _{gs}		-	10	-	nC
Gate-Drain Charge	Q _{gd}		-	15	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =-20A	-	-	-1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	-45	A
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = -10A	-	47	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	53	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics (Curves)

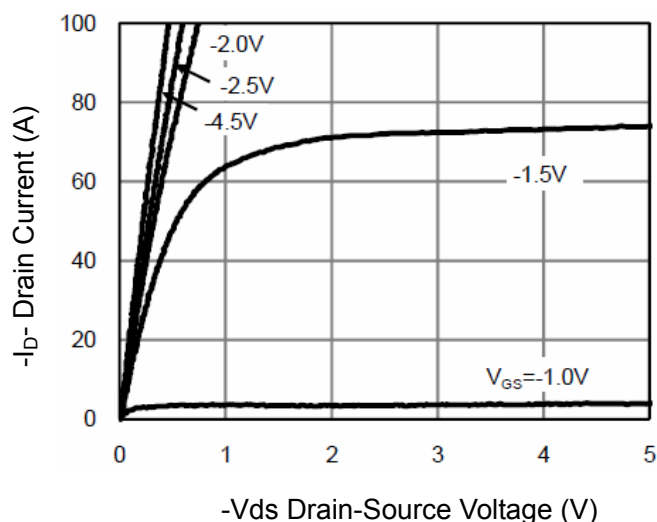


Figure 1 Output Characteristics

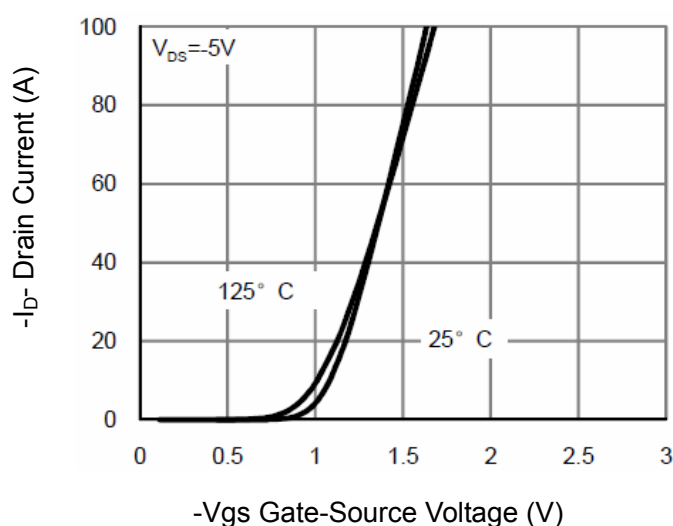


Figure 2 Transfer Characteristics

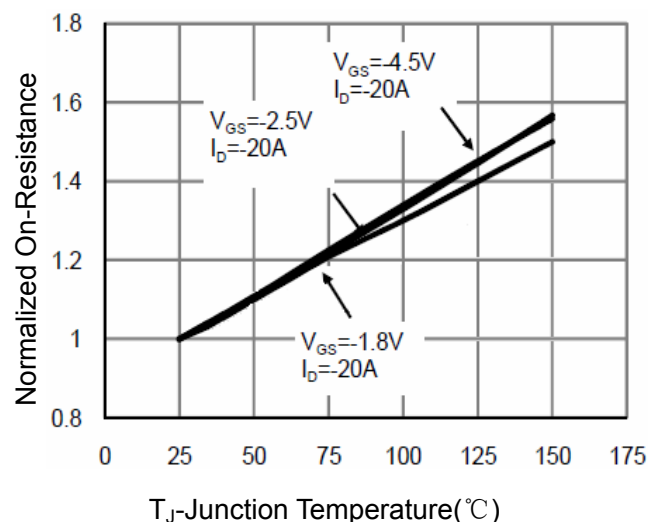


Figure 4 R_{DS(on)}-Junction Temperature

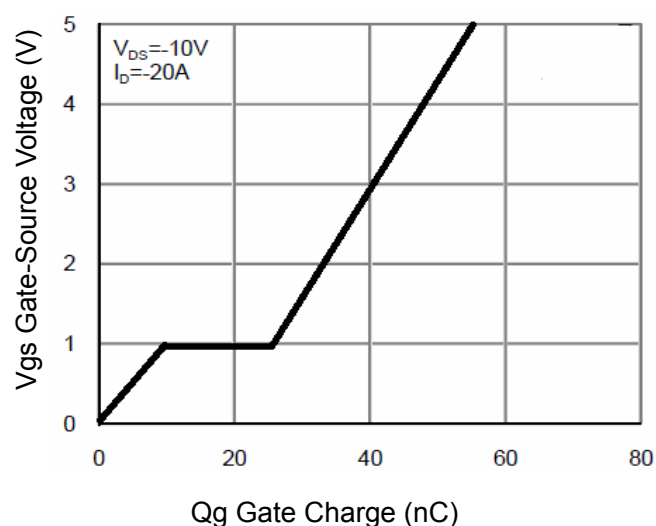


Figure 5 Gate Charge

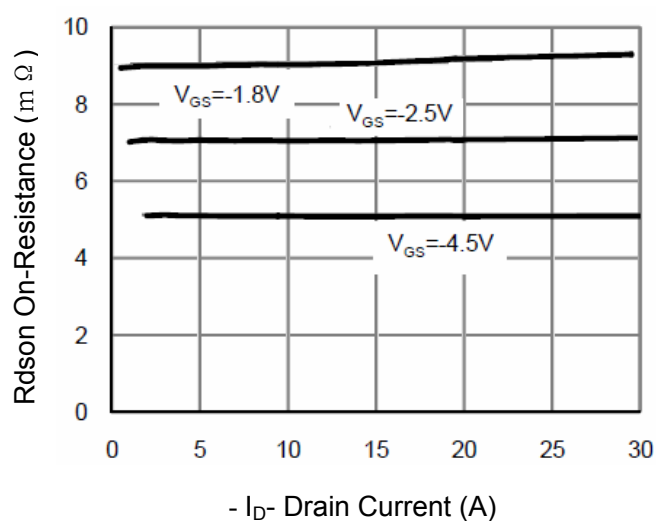


Figure 3 R_{DS(on)}- Drain Current

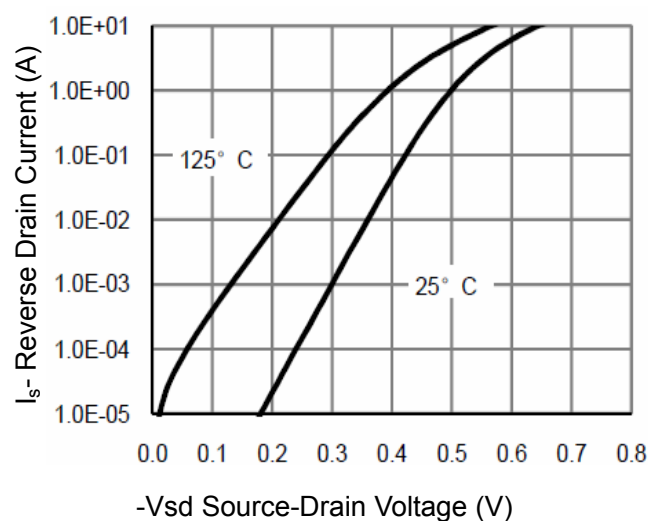
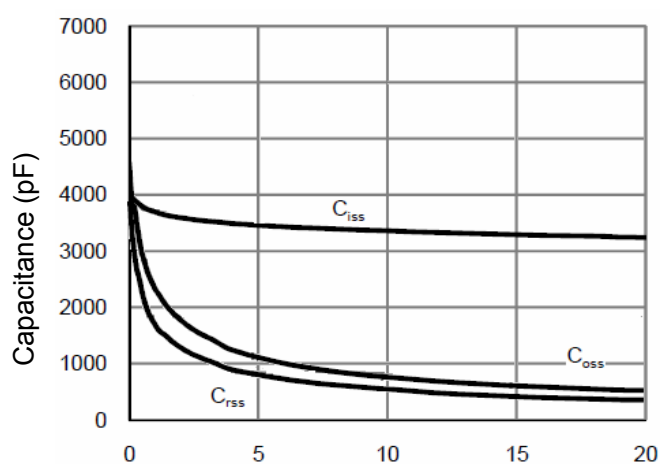
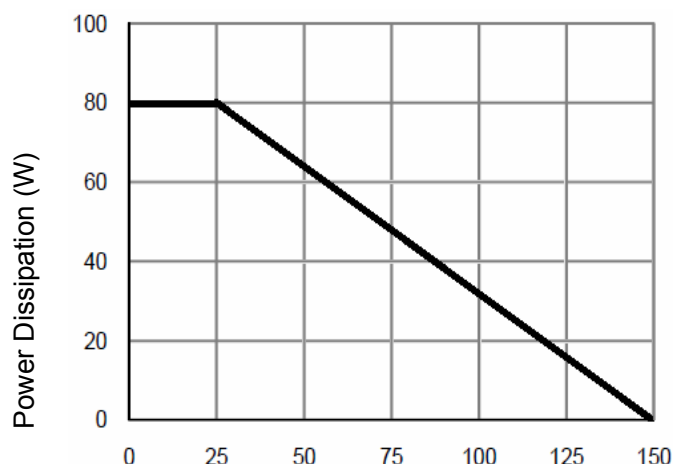


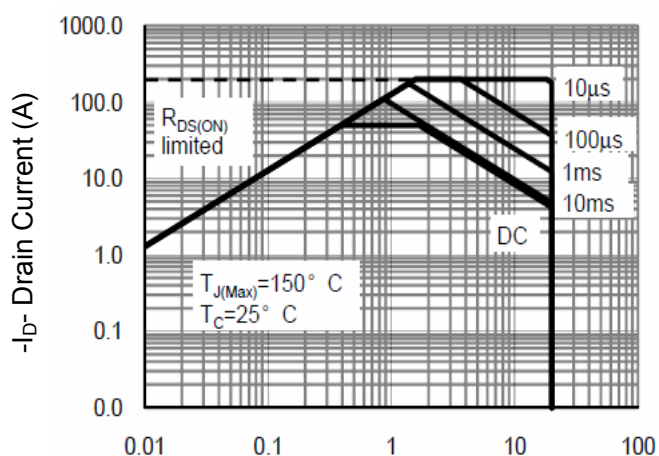
Figure 6 Source- Drain Diode Forward



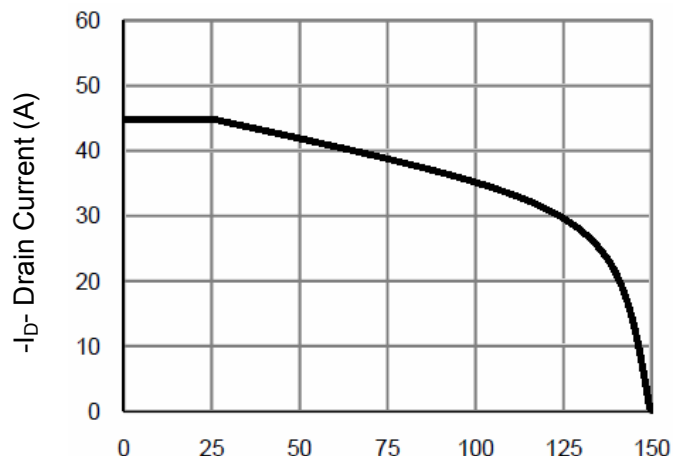
-Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 Power De-rating



-Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 -Current De-rating

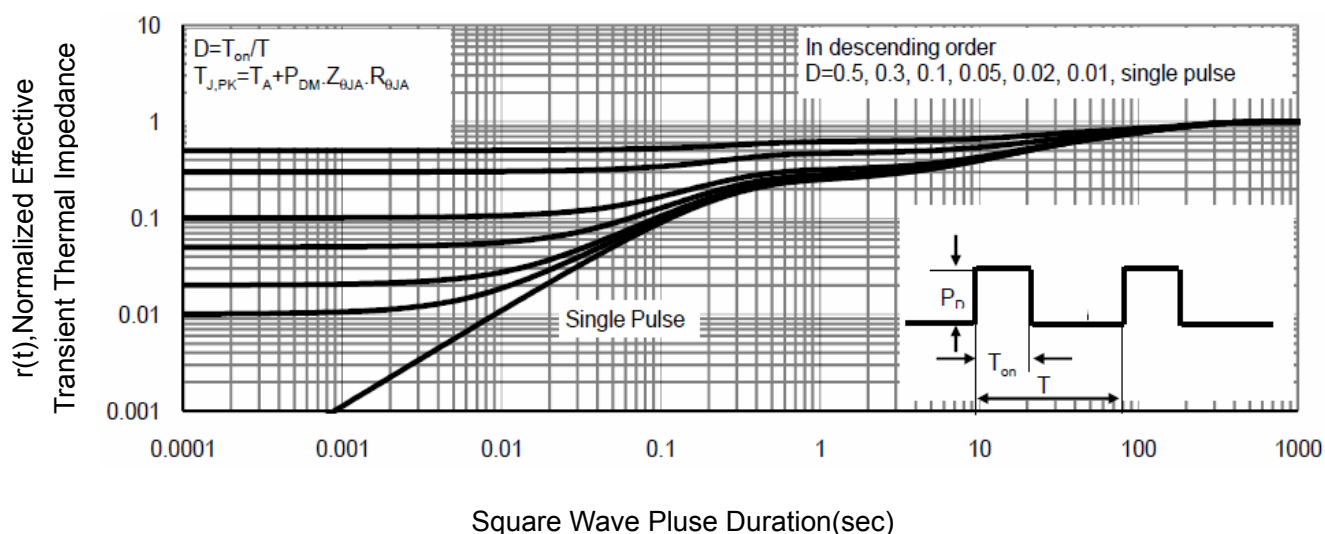
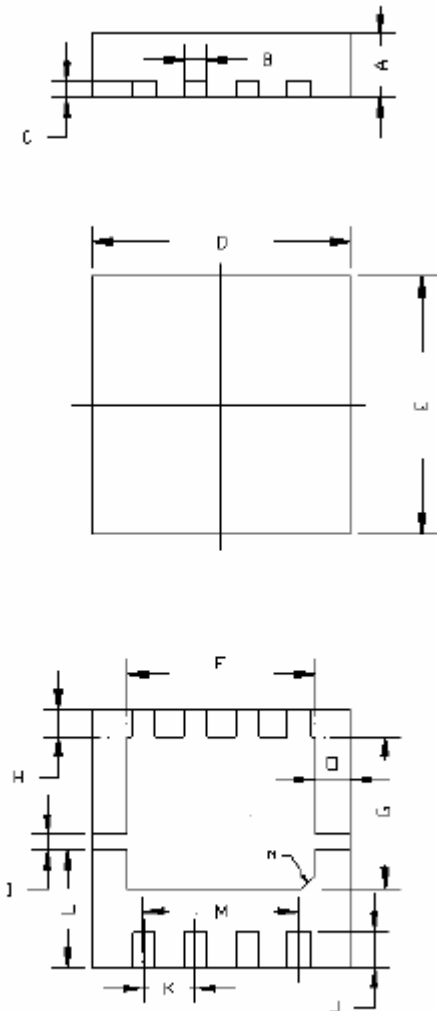


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3 EP Package Information

封装外形尺寸图				
	符号	单位: mm		
		MIN	MAX	TYP
	A	0.75	0.85	0.8
	B	0.25	0.35	0.3
	C	0.18	0.22	0.2
	D	3.2	3.3	3.25
	E	3.2	3.3	3.25
	F	2.2	2.5	2.35
	G	1.8	2.0	1.9
	H	0.3	0.4	0.35
	I	0.15	0.25	0.2
	J	0.4	0.5	0.45
	K	0.6	0.7	0.65
	L	1.38	1.58	1.48
	M	1.8	2.1	1.95
	N	0.15*45°		
	O	0.4	0.5	0.45